R&S®RTO-K81, R&S®RTO6-K81, R&S®RTP-K81/-K83
PCIe Compliance Test
User Manual

1333229902
Version 08

ROHDE&SCHWARZ
Make ideas real

This manual describes the PCIe compliance test procedures with the following options:

- R&S®RTO-K81 (1326.0920.02) - PCIe 1.1
- R&S®RTO6-K81 (1801.6964.02) - PCIe 1.1 / 2.0
- R&S®RTP-K81 (1337.8885.02) - PCIe 1.1 / 2.0
- R&S®RTP-K83 (1800.6954.02) - PCIe 1.1 / 2.0 / 3.0

The tests require the R&S ScopeSuite software.

The software contained in this product uses several valuable open source software packages. For information, see the "Open Source Acknowledgment" document, which is available for download from the R&S RTO/RTO6/RTP product page at http://www.rohde-schwarz.com/product/rto.html > "Software".
Rohde & Schwarz would like to thank the open source community for their valuable contribution to embedded computing.

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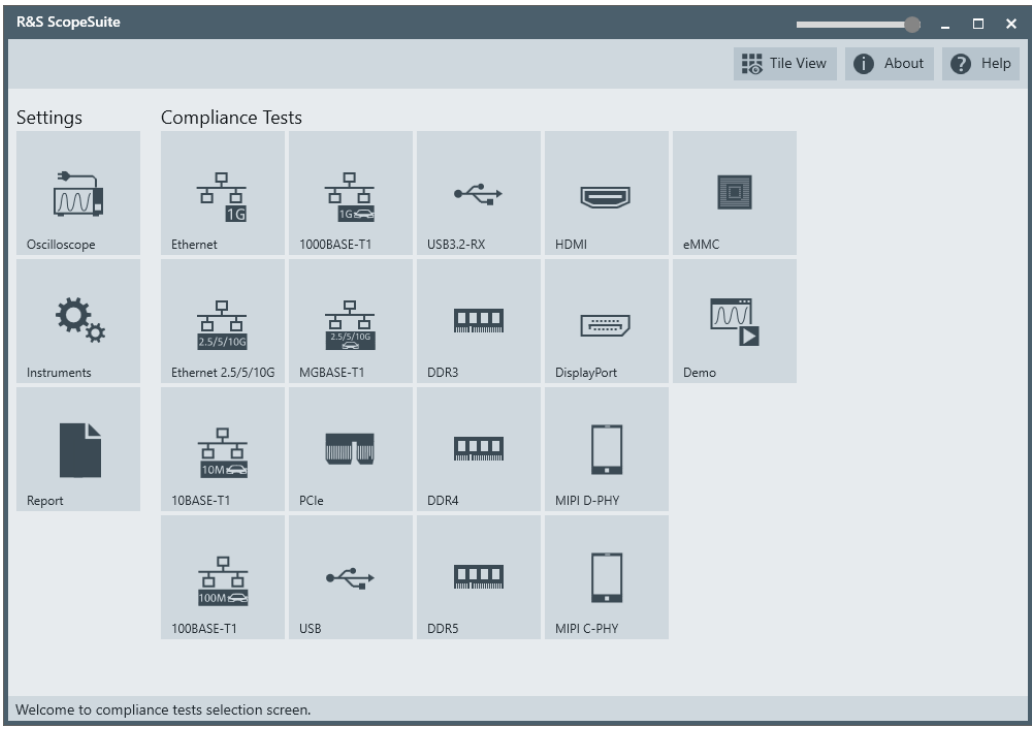
1333.2299.02 | Version 08 | R&S®RTO-K81, R&S®RTO6-K81, R&S®RTP-K81/-K83

Throughout this manual, products from Rohde & Schwarz are indicated without the ® symbol.

Contents

1 R&S ScopeSuite overview

The R&S ScopeSuite software is used with R&S RTO/RTO6/RTP oscilloscopes. It can be installed on a test computer or directly on the oscilloscope. For system requirements, refer to the Release Notes.



The R&S ScopeSuite main panel has several areas:

- "Settings": connection settings to oscilloscope and other instruments also default report settings
- "Compliance Tests": selection of the compliance test
- "Demo": accesses demo test cases that can be used for trying out the software without having a connection to an oscilloscope
- : shift sideways to change the transparency of the dialog box
- "Help": opens the help file, containing information about the R&S ScopeSuite configuration
- "About": gives information about the R&S ScopeSuite software
- "Tile View": allows a personalization of the compliance test selection
  You can configure which tests are visible in the compliance test section and which are hidden, so that only the ones you use are displayed.

► To hide a test from the "Compliance Tests" view, do one of the following:

a) Right-click on the compliance test that you want to hide.
The icon of the test changes, see Figure 1-1. Now with a left click you can hide the test.

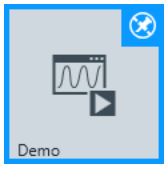


Figure 1-1: Unpin icon

b) Click on "Title View" to show a list of the available test cases. By clicking a test case in the show list, you can pin/unpin it from the main panel.

2 Preparing the measurements

2.1 Test equipment

PCIe 1.1 / PCIe 2.0 Test Equipment

For PCIe compliance tests, the following test equipment is needed:

- R&S RTO/RTO6/RTP oscilloscope with at least 6 GHz bandwidth, 2 channels and 20 GS/s available
- Probes/cables:
  - Two SMP to SMA cables or
  - Two single-ended probes with at least 6GHz bandwidth bandwidth or
  - One differential probe with at least 6GHz bandwidth bandwidth
- R&S RTO/RTO6/RTP-K81 PCIe compliance test option (required option, installed on the oscilloscope)
- Recommended test fixture:
  - For Add-In card testing: PCI Express Compliance Base Board (CBB2.0) from PCI-SIG
  - For System Board testing: PCI Express Compliance Load Board (CLB2.0) from PCI-SIG
- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the oscilloscope.

PCIe 3.0 Test Equipment

For PCIe compliance tests, the following test equipment is needed:

- R&S RTP oscilloscope with at least 16 GHz bandwidth, 2 channels and 40 GS/s available
- Probes/cables:
  - Two SMP to SMA cables or
  - Two single-ended probes with at least 6GHz bandwidth bandwidth or
  - One differential probe with at least 6GHz bandwidth bandwidth
  - Two R&S RTP-ZMA40 Amplifier probe tips.
- R&S RTP -K83 PCIe compliance test option (required option, installed on the oscilloscope)
- Recommended test fixture:
  - For Add-In card testing: PCI Express Compliance Base Board (CBB3.0) from PCI-SIG
  - For System Board testing: PCI Express Compliance Load Board (CLB3.0) from PCI-SIG

- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the oscilloscope.

2.2 Installing software and license

The preparation steps are performed only once for each computer and instrument that are used for testing.

Uninstall older versions of the R&S ScopeSuite

If an older version of the R&S ScopeSuite is installed, make sure to uninstall the old version before you install the new one. You can find the version number of the current installation in "Help" menu > "About". To uninstall the R&S ScopeSuite, use the Windows " Control Panel" > "Programs".

For best operation results, we recommend that the installed firmware versions of the R&S ScopeSuite and the oscilloscope are the same.

To install the R&S ScopeSuite

1. Download the latest R&S ScopeSuite software from the "Software" section on the Rohde & Schwarz R&S RTO/RTO6/RTP website:
   www.rohde-schwarz.com/product/rtp.html
   www.rohde-schwarz.com/product/rto.html
2. Install the R&S ScopeSuite software:
   - On the computer that is used for testing, or
   - On the R&S RTO/RTO6/RTP.

   For system requirements, refer to the Release Notes.

To install the license key on the R&S RTO/RTO6/RTP

► When you got the license key of the compliance test option, enable it on the oscilloscope using [Setup] > "SW Options".
For a detailed description, refer to the R&S RTO/RTO6/RTP user manual, chapter "Installing Options", or to the online help on the instrument.

2.3 Setting up the network

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection.

There are two ways of connection:

- LAN (local area network): It is recommended that you connect to a LAN with DHCP server. This server uses the Dynamic Host Configuration Protocol (DHCP) to assign all address information automatically.

If no DHCP server is available, assign fixed IP addresses to all devices.

- Direct connection of the instruments and the computer or connection to a switch using LAN cables: Assign fixed IP addresses to the computer and the instruments and reboot all devices.

To set up and test the LAN connection

1. Connect the computer and the instruments to the same LAN.
2. Start all devices.
3. If no DHCP server is available, assign fixed IP addresses to all devices.
4. Ping the instruments to make sure that the connection is established.
5. If VISA is installed, check if VISA can access the instruments.
   a) Start VISA on the test computer.
   b) Validate the VISA address string of each device.

See also:

- Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

2.4 Starting the R&S ScopeSuite

To start the R&S ScopeSuite on the test computer or on the oscilloscope:

► Double-click the R&S ScopeSuite program icon.

To start the R&S ScopeSuite on the instrument, in the R&S RTO/RTO6/RTP firmware:

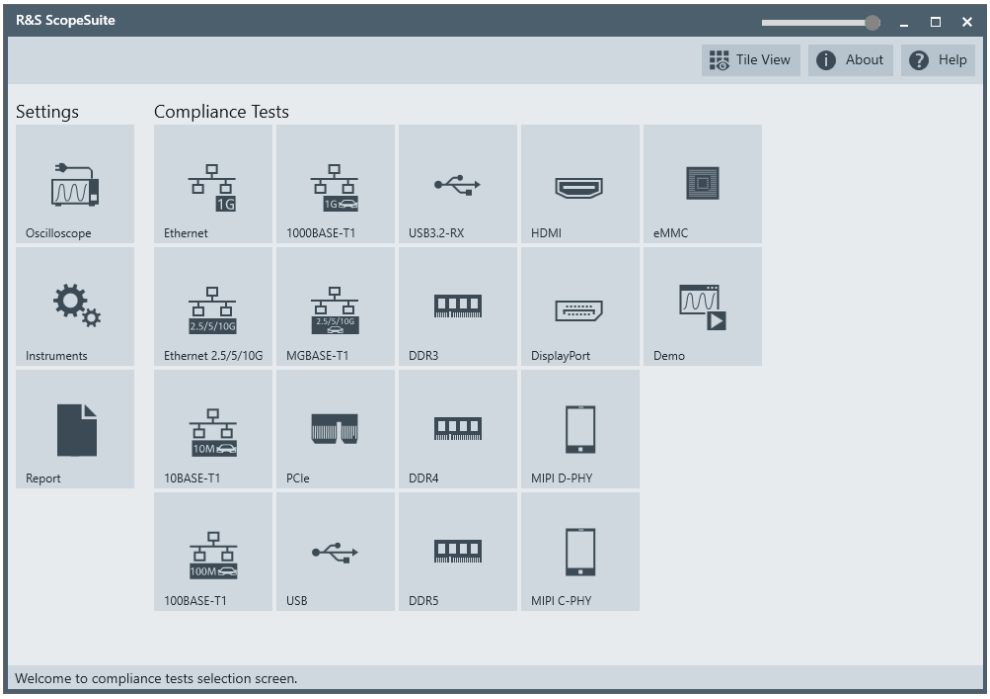
► In the "Apps" dialog, open the "Compliance" tab.

2.5 Connecting the R&S RTO/RTO6/RTP

If the R&S ScopeSuite is installed directly on the instrument, the software detects the R&S RTO/RTO6/RTP firmware automatically, and the "Oscilloscope" button is not available in the R&S ScopeSuite.

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection, see Chapter 2.3, "Setting up the network", on page 8. The R&S ScopeSuite software needs the IP address of the oscilloscope to establish connection.

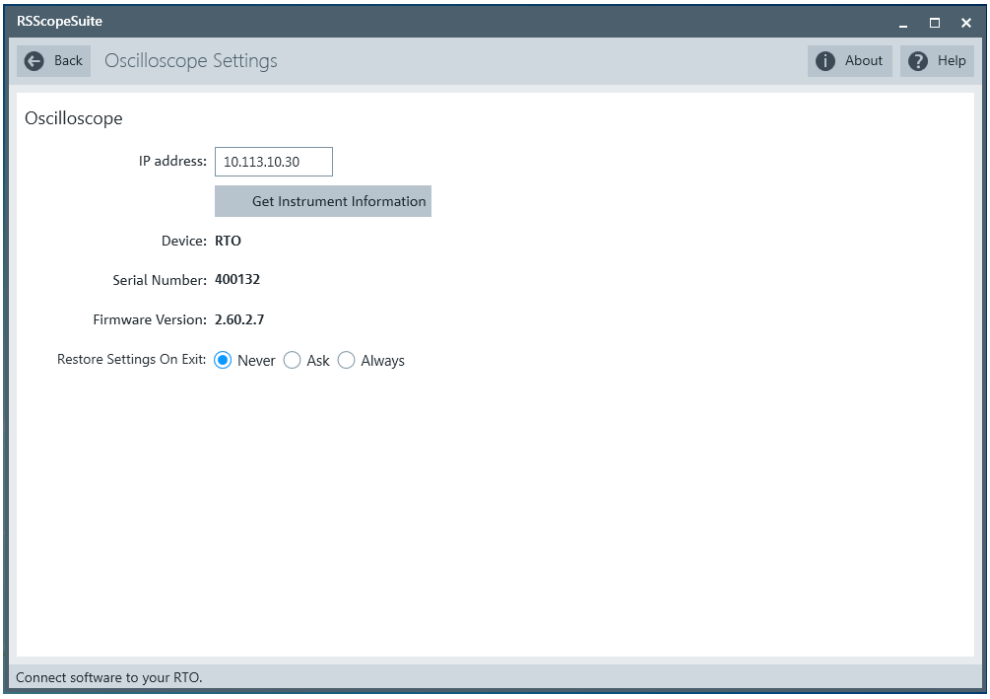
1. Start the R&S RTO/RTO6/RTP.
2. Start the R&S ScopeSuite software.
3. Click "Settings" > "Oscilloscope".



4. Enter the IP address of the oscilloscope.
   To obtain the IP address: press the Rohde & Schwarz logo at the top-right corner of the oscilloscope's display.

5. Click "Get Instrument Information".

   The computer connects with the instrument and gets the instrument data.



If the connection fails, an error message is shown.

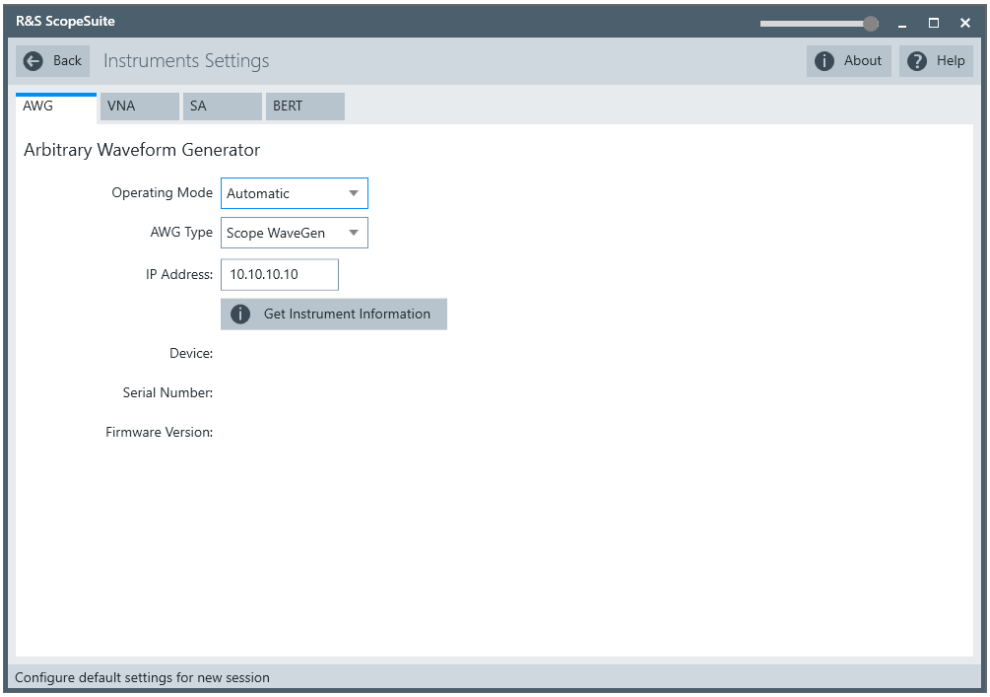
2.6 Connecting the arbitrary waveform generator

Automatic test execution is possible with all instruments that are listed in the R&S ScopeSuite, in the "Instrument Settings" dialog box. In automatic mode, the R&S ScopeSuite configures the instrument and ensures that the AWG sends the required waveforms. Automatic mode requires a LAN connection and the installation of a VISA implementation (R&S VISA, see www.rohde-schwarz.com/rsvisa) on the computer that is running the R&S ScopeSuite. If the R&S ScopeSuite is installed on the R&S RTO/RTO6/RTP, no installation is needed because VISA is already installed on the instrument. If the Tabor WX2182B / WX2182C or Hameg HMF2550 is used for automatic testing, fixed IP addresses are required.

For manual test execution, it is recommended to use one of the listed AWGs, but you can also use another AWG. In manual mode, you connect the AWG to the test board and configure the instrument manually. VISA is not required. The R&S ScopeSuite uses VISA if it is installed, otherwise it uses the VXI-11 protocol.

To configure the arbitrary waveform generator for automatic testing

1. Connect the computer and the AWG.
2. Set up the LAN connection. See Chapter 2.3, "Setting up the network", on page 8.
3. In the R&S ScopeSuite, click "Instruments".
   Alternatively, you can select the "Instrument" tab in the test case configuration dialog.
4. Click the "AWG" tab.
5. Select "Operating mode" = "Automatic".
6. Select a supported "AWG Type" and enter its IP address.
   For a list of the supported AWGs, see chapter "Test Equipment".



7. Click "Get Instrument Information".

   The computer or R&S RTO/RTO6/RTP connects with the instrument and retrieves the instrument data.

8. If the connection to the arbitrary waveform generator failed, check if the IP address is assigned correctly.

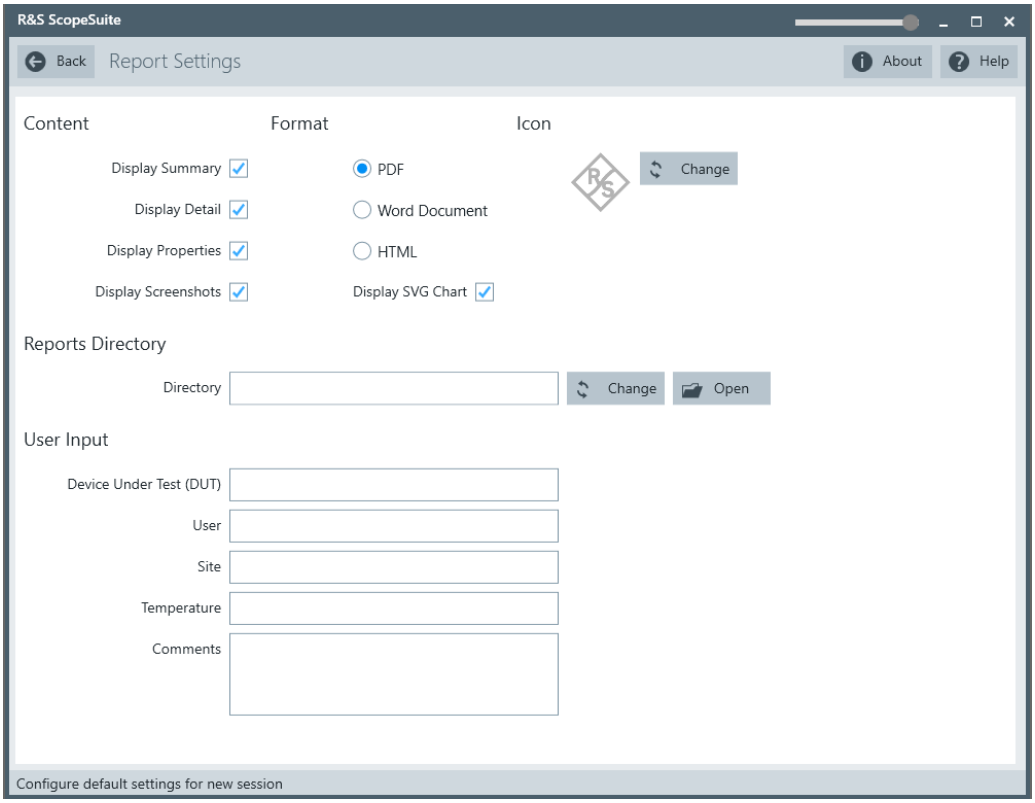
To configure the AWG for manual testing

► In the "AWG" tab, enable the "Manual" operating mode.

2.7 Report configuration

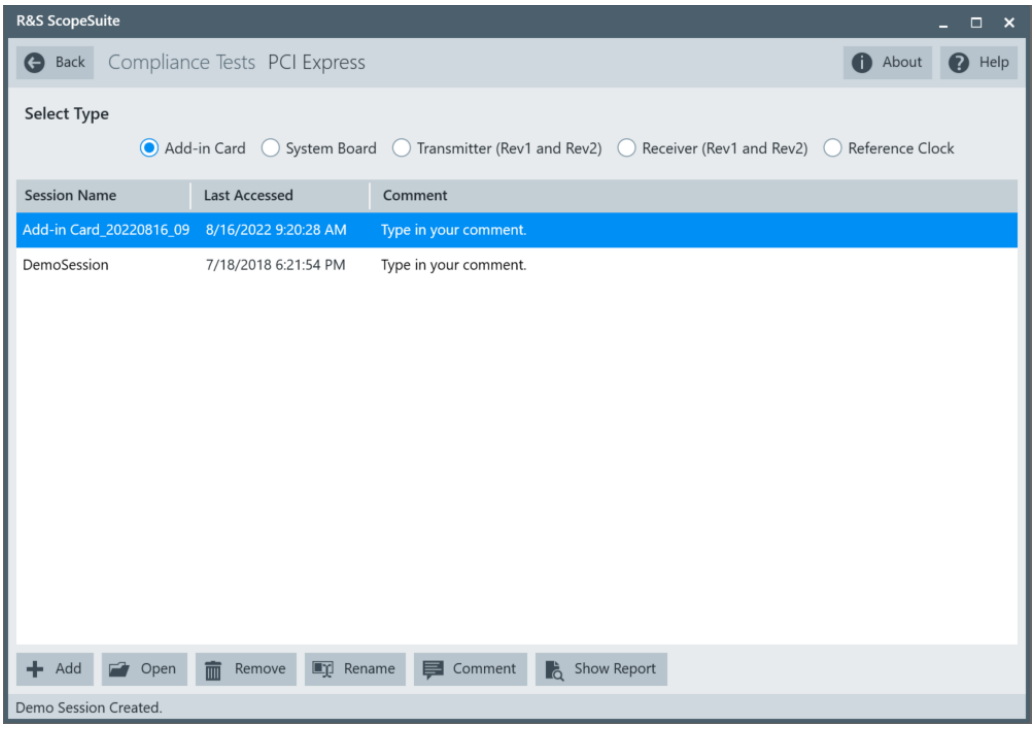
In the "Report Configuration" menu, you can select the format of the report and the details to be included in the report. You can also select an icon that is displayed in the upper left corner of the report.

Also, you can enter common information on the test that is written in the "General Information" section of the test report.


R&S ScopeSuite
Back
Report Settings
About
Help
Content
Format
Icon
Display Summary
Display Detail
Display Properties
Display Screenshots
PDF
Word Document
HTML
Display SVG Chart
Change
Reports Directory
Directory
Change
Open
User Input
Device Under Test (DUT)
User
Site
Temperature
Comments
Configure default settings for new session

3 Performing tests

3.1 Starting a test session



After you open a compliance test, the "Session Selection" dialog appears. In this dialog, you can create new sessions, open or view existing report.

The following functions are available for handling test sessions:

Function	Description
"Add"	Adds a new session
"Open"	Opens the selected session
"Remove"	Removes the selected session
"Rename"	Changes the "Session Name"
"Comment"	Adds a comment
"Show report"	Generates a report for the selected session

To add a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog press "Add".
3. If necessary change the "Session Name"

To open a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog, select the session you want to open and double click on it.
   Alternatively, select the session and press "Open".

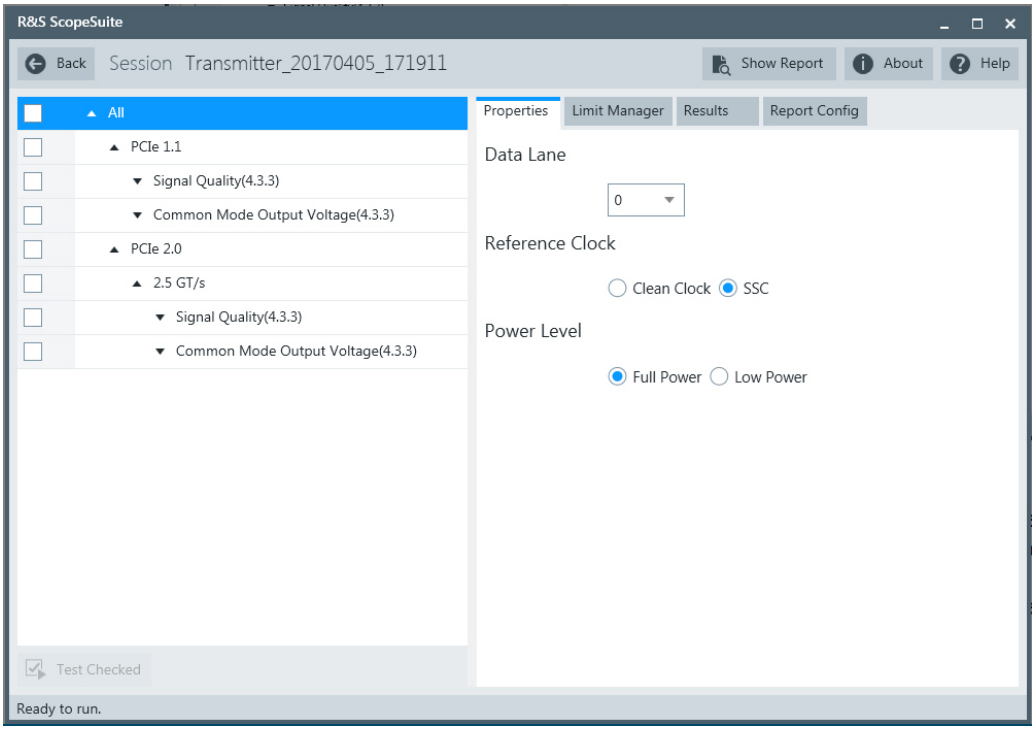
To show a report for a test session

1. In the R&S ScopeSuite window, select the compliance test.
2. In the "Session Selection" dialog, select the session you want the report for and press "Show report".

3.2 Configuring the test

1. In the R&S ScopeSuite window, select the compliance test to be performed:
   - "PCIe"
2. Open a test session, see Chapter 3.1, "Starting a test session", on page 14.
3. Adjust the "Properties" settings for the test cases you want to perform.
4. Click "Limit Manager" and edit the limit criteria, see Chapter 3.2.1.1, "Limit manager", on page 17.
5. If you want to use special report settings the "Report Config" tab to define the format and contents of the report. Otherwise the settings defined in "RSScopeSuite" > "Settings" > "Report" are used. See Chapter 2.7, "Report configuration", on page 12.
6. Click "Test Checked"/"Test Single" and proceed as described in the relevant test case chapter.

3.2.1 General test settings



Each session dialog is divided into several sections:

- "Properties": shows the settings that can be made for the test case selected on the left side of the dialog. You can differentiate between the "All" and the sub test properties
  In the "All" > "Properties" tab you can configure the settings for all test cases in the current session. Once you change and save a setting in this tab, the changes will be done for all test in the sessions. At the same time, there will be a special marking for the functions that have different settings for different sub tests.
- "Limit Manager": sets the measurement limits that are used for compliance testing, see Chapter 3.2.1.1, "Limit manager", on page 17.
- "Results": shows an overview of the available test results for this session.
- "Instruments": defines instruments settings for connecting to external devices, that are specific for this test session.
  When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Instruments") are copied to the session. This "Instruments" tab can be used to change those copied defaults.
- "Report Config": defines the format and contents of the report for this session.
  When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Report") are copied to the session. This "Report Config" tab can be used to change those copied defaults.
- "Test Checked"/ "Test Single": starts the selected test group.

3.2.1.1 Limit manager

The "Limit Manager" shows the measurement limits that are used for compliance testing.

Each limit comprises the comparison criterion, the unit, the limit value A, and a second limit value B if the criterion requires two limits.

You can set the values to defaults, change the values in the table, export the table in xml format, or import xml files with limit settings.

You can also return the values to the original limits with "Reset to default".

► Check and adjust the measurement limits.

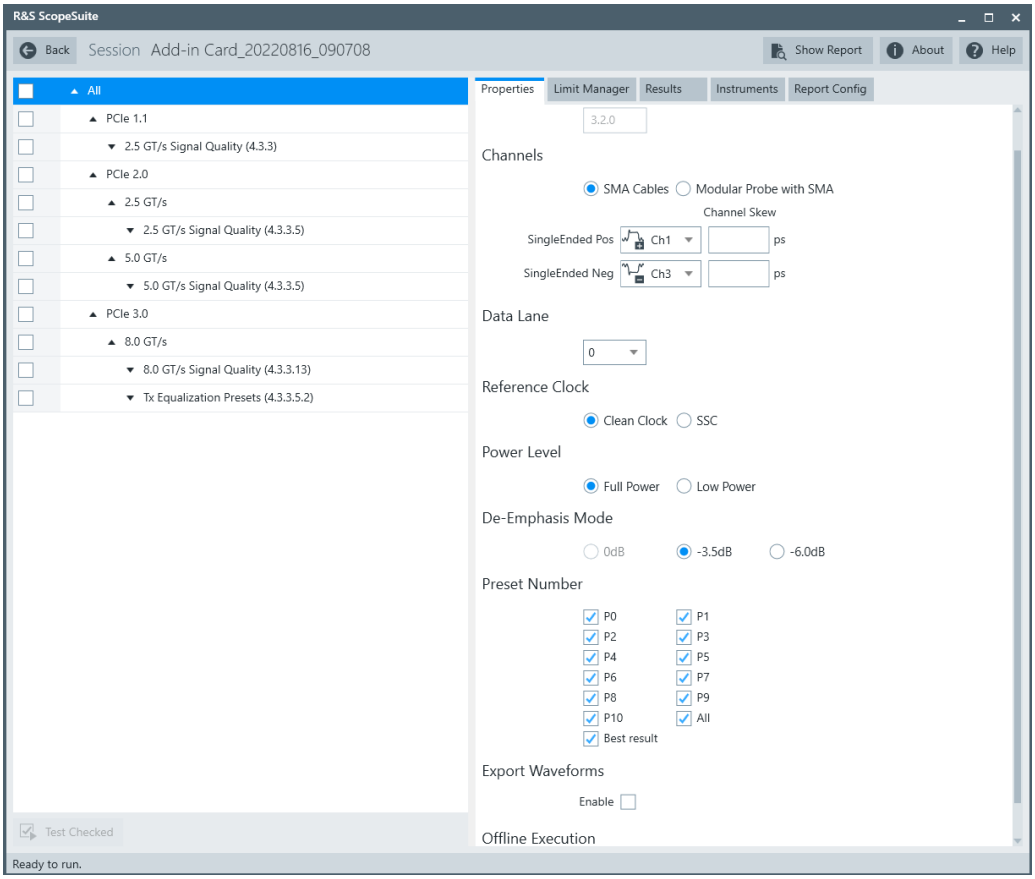
Properties | Limit Manager | Results | Report Config

Measurement	Criteria	Unit	A	B
Generation 1 Unit Interval	A<x<B	s	3.9988E-10	4.0212E-10
Generation 1 Data Rate (SSC Clock)	A<x<B	Bits	2.48675E+09	2.50075E+09
Generation 1 Data Rate (Clean Clock)	A<x<B	Bits	2.49925E+09	2.50075E+09
Generation 2 Unit Interval	A<x<B	s	1.9994E-10	2.0006E-10
Generation 2 Data Rate (SSC Clock)	A<x<B	Bits	4.9735E+09	5.0015E+09
Generation 2 Data Rate (Clean Clock)	A<x<B	Bits	4.9985E+09	5.0015E+09
3.5dB De-Emphasized Differential Voltage Ratio	A<x<B	dB	3	4
6.0dB De-Emphasized Differential Voltage Ratio	A<x<B	dB	5.5	6.5
(Full Power) Differential Output Voltage	A<x<B	V	0.8	1.2
(Low Power) Differential Output Voltage	A<x<B	V	0.4	1.2
Generation 1 (Full Power) Min Non Transition Eye Height	A<x<B	V	0.505	1.2
Generation 1 (Full Power) Min Transition Eye Height	A<x<B	V	0.8	1.2
Generation 1 (Full Power) Min Eye Width	x>=A	s	3E-10	
(Full Power) Median To Max Jitter	x<=A	s	5E-11	
Generation 1 (Full Power) Composite Eye Height	x>=A	V	0.566	
Generation 1 (Low Power) Min Non Transition Eye Height	A<x<B	V	0.4	1.2
Generation 1 (Low Power) Min Transition Eye Height	A<x<B	V	0.4	1.2
Generation 1 (Low Power) Min Eye Width	x>=A	s	2.8E-10	
(Low Power) Median To Max Jitter	x<=A	s	5E-11	
Generation 1 (Low Power) Composite Eye Height	x>=A	V	0.4	
Generation 1 Rise/Fall Time	x>=A	s	5E-11	
RMS AC Peak Common Mode Output Voltage	x<A	V	0.02	
Avg DC Common Mode Output Voltage	A<=x<=B	V	0	3.6
DC Common Mode Line Delta	0<x<=A	V	0.025	
DC Common Mode Output Voltage Variation	x<=A	V	0.1	
Generation 2 Rise/Fall Time	x>=A	s	3E-11	

Reset to Default | Export | Import

3.2.2 PCIe test configuration

The test configuration consists of some test-specific configuration settings.



SigTest

Displays the version of the SigTest software that is used for the test.

Included in the installation is 3.2.0. The following table gives an overview of the compatibility with the SigTest versions:

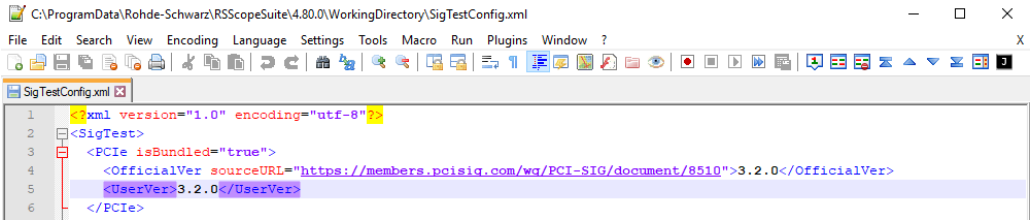
Table 3-1: Supported SigTest versions

Version	Standard	Installed with ScopeSuite	Notes
3.2.0	PCIe 3	Yes	Tested on Windows 10 version 1809. Older Windows 10 versions (e.g. Windows 10 version 1703) may show a crash popup on exit.
3.2.0.3	PCIe 3	No	Does not work
4.0.23.2	PCIe 3	No	Supported
4.0.52	PCIe 4	No	Supported

You are able to select a custom SigTest by editing the `SigTestConfig.xml` file in:

`C:\ProgramData\Rohde-Schwarz\RSScopeSuite\4.80.0\WorkingDirectory`.

You can set the required version in the PCIe *<UserVer>...</UserVer>* field.



Channels
In the "Channels" section you can select the probes used for the test setup and set the skew for each channel.

The availble probes are " SMA cables" and "Modular Probe with SMA".

Skew ← Channels
The skew compensates signal propagation differences between channels caused by the different length of cables, probes, and other sources.

When creating a new session, the skew values are read from the oscilloscope and the skew fields are updated. You can also enter the skew value for each channel. Measure the deskew of each channel before you start the compliance test.

Retrieve skew ← Channels
The skew values are read from the oscilloscope and updated.

Data Lane
Selects the data lane under test.

Reference Clock
Selects the type of reference clock of the DUT. You can select between a clean clock or a spread-spectrum clocking (SSC).

De-Emphasis Mode
Selects between the "-3.5 dB" and "-6 dB" de-emphasis mode of the DUT.This setting is available for 5.0 GT/s Signal quality tests.

Power Level
Selects between the "Full Power" and "Low Power" mode of the DUT.

Preset numbers
Selects the preset numbers for the "System Board "> "Tx Equalization Presets (4.3.3.5.2)". They give a coarser control over the Tx equalization resolution.

Export Waveforms
Enables you to export a waveform. You can later load the waveforms to run the tests in the offline mode, see "Offline Execution" on page 21.

You can define an export directory, or use the default one:

`MyDocuments\Rohde-Schwarz\RSScopeSuite\<Version>\Waveforms\<ComplianceTest>\<SessionType>\<SessionName>`

For example:

```
MyDocuments\Rohde-Schwarz\RSScopeSuite\4.80.0\Waveforms\PCIe\
Add-in Card(Tx)_20201030_144116
```

Offline Execution
If enabled, allows you to use exported waveforms as a source for the execution of the compliance test.

You can select one waveform for each needed signal.

3.3 Getting test results

For each test, the test data - report, diagrams and waveform files - is saved in the following folder:

```
%ProgramData%\Rohde-Schwarz\RSScopeSuite2\Sessions\PCIe\
<Session_Name>
```

If you resume an existing session, new measurements are appended to the report, new diagrams and waveform files are added to the session folder. Existing files are not deleted or replaced. Sessions data remain until you delete them in the "Results" tab of the session.

The report format can be defined in "RSScopeSuite" > "Settings" > "Report" for all compliance tests (see also Chapter 2.7, "Report configuration", on page 12). If you want to use special report settings for a session, you can define the format and contents of the report in the "Report Config" tab of the session.

All test results are listed in the "Results" tab. Reports can be provided in PDF, MSWord, or HTML format. To view and print PDF reports, you need a PDF viewer, for example, the Acrobat Reader.

The test report file can be created at the end of the test, or later in the "Session Selection" dialog.

To show a test report

1. In the R&S ScopeSuite window, select the compliance test to be performed.
2. Select the session name in the "Session Selection" dialog and click "Show report".

   The report opens in a separate application window, depending on the file format. You can check the test results and print the report.

To delete the results, diagrams and waveform files of a session

1. In the "Session Selection" dialog select the session and open it.
2. In the "Results" tab, select the result to be deleted.
3. Click "Remove".

4 Add-in Card tests

4.1 Starting Add-in Card tests

Before you run the test, complete the following actions:

- Initial setup of the equipment, see Chapter 2.2, "Installing software and license", on page 8
- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

1. Select "PCIe" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, set "Select Type" > "Add-in Card (Tx)".
3. Add a new test session and open it, see Chapter 3.1, "Starting a test session", on page 14.
4. Check the test configuration settings and adjust, if necessary. See:
   - Chapter 3.2.2, "PCIe test configuration", on page 18
   - Chapter 3.2.1.1, "Limit manager", on page 17
5. Select/check the test cases you want to run and click "Test Single"/"Test checked".
6. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

4.2 PCIe 1.1 / PCIe 2.0

4.2.1 Signal Quality test

4.2.1.1 Test equipment

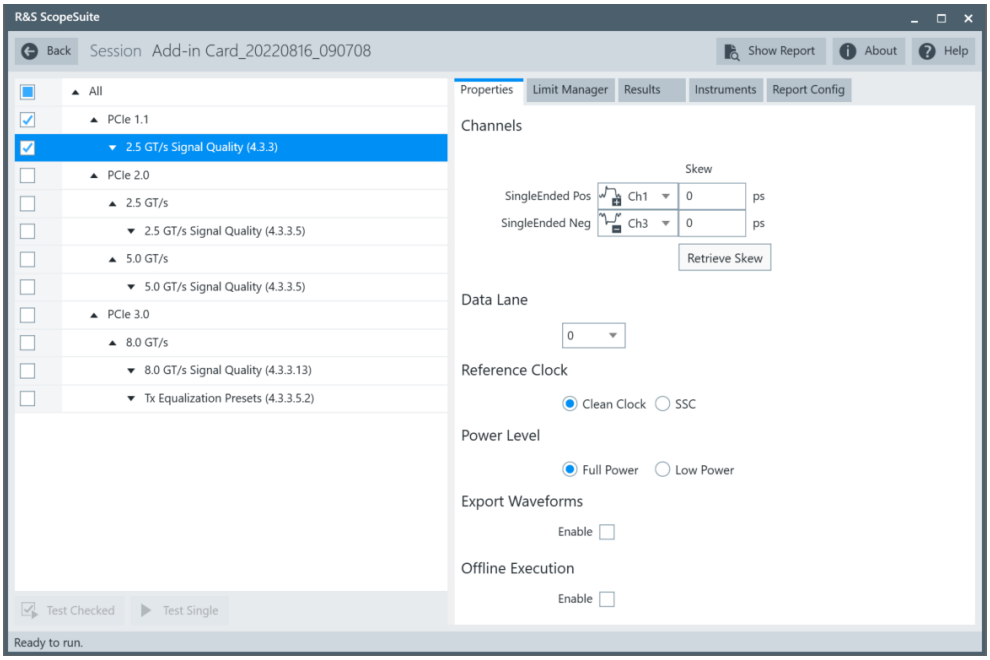
Table 4-1: Equipment for Signal Quality add-in card tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
Compliance Base Board[1]	PCISIG Gen 2.0 Compliance Base Board (CBB)	1
SMP to SMA cables	Connected to SMP probing points on CBB	2

Item	Description, model	Quantity
DUT	Add-In Card	1
We recommend PCI Express Compliance Base Board (CBB2.0) from PCI-SIG.		

4.2.1.2 Performing the tests

1. Start the test as described in Chapter 4.1, "Starting Add-in Card tests", on page 22.
2. Select the "Signal Quality (4.3.3)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

4.2.1.3 Purpose

This test verifies that the transmitter signal complies with the quality specifications in section 4.3.3 of the PCI Express Base Specification, REV. 1.1.

4.2.1.4 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

These tests use PCI Express Compliance Base Board (CBB2.0) from PCI-SIG. The CBB test fixture provides SMP Probing Points for data lanes that are used to connect to the oscilloscope.

4.2.1.5 Measurements

This test does the following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 1.1 and Section 4.7.1 of the Card Electromechanical Specification, REV 1.1.

- Mean Unit Interval (UI)
- Data Rate
- Template Tests
- Min Eye Width (T_{TX-EYE})
- Median To Max Jitter ($T_{TX-EYEMEDIAN-to-MAXJITTER}$)
- Differential Output Voltage ($V_{TX-DIFFp-p}$)
- Total Jitter at BER-12 (PCIe 2.0 only)
- Deterministic jitter (PCIe 2.0 only)
- RMS jitter (PCIe 2.0 only)

4.3 PCIe 3.0

PCIe 3.0 compliance tests require option R&S RTP- K83.

4.3.1 Signal Quality test

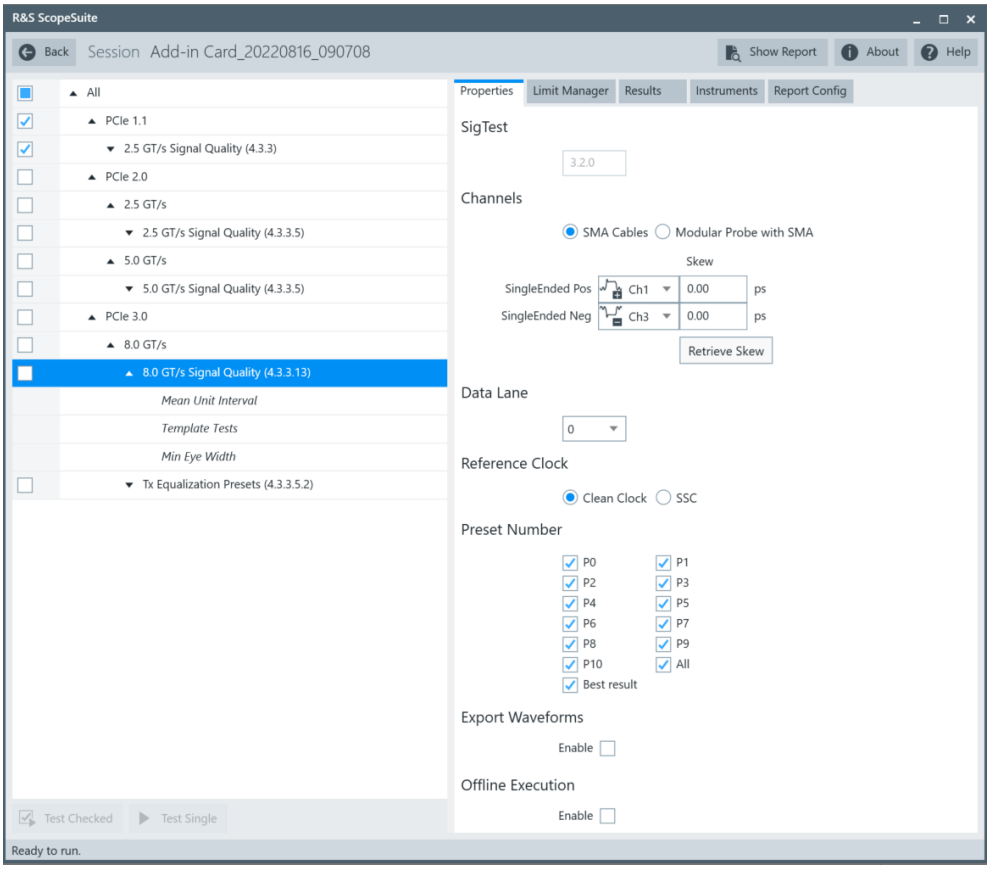
4.3.1.1 Test equipment

Table 4-2: Equipment for Signal Quality add-in card tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S R&S RTP with at least 16 GHz bandwidth and (40 GS/s available)	1
Compliance Base Board[1]	PCISIG Gen 3.0 Compliance Base Board (CBB)	1
SMP to SMA cables	Connected to SMP probing points on CBB	2
DUT	Add-In Card	1
DC block (optional)	DC Block, BLK-222+, 50 Ohm, 0.01-2.2 GHz	
We recommend PCI Express Compliance Base Board (CBB3.0) from PCI-SIG.		

4.3.1.2 Performing the tests

1. Start the test as described in Chapter 4.1, "Starting Add-in Card tests", on page 22.
2. Select the "Signal Quality (4.3.3.13/ 4.3.3.13.1)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

4.3.1.3 Purpose

This test verifies that the transmitter signal complies with the quality specifications in section 4.3.3.13/ 4.3.3.13.1 of the PCI Express Base Specification, REV. 3.0.

4.3.1.4 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

If the preset test mode is unable to trigger properly, a DC block needs to be attached to the WaveGen (B6).

These tests use PCI Express Compliance Base Board (CBB3.0) from PCI-SIG. The CBB test fixture provides SMP Probing Points for data lanes that are used to connect to the oscilloscope.

4.3.1.5 Measurements

This test does the following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 3.0 and Section 4.7.1 of the Card Electromechanical Specification, REV 3.0.

- Mean Unit Interval (UI)
- Data Rate
- Template Tests
- Min Eye Width

4.3.2 Tx Equalization presets

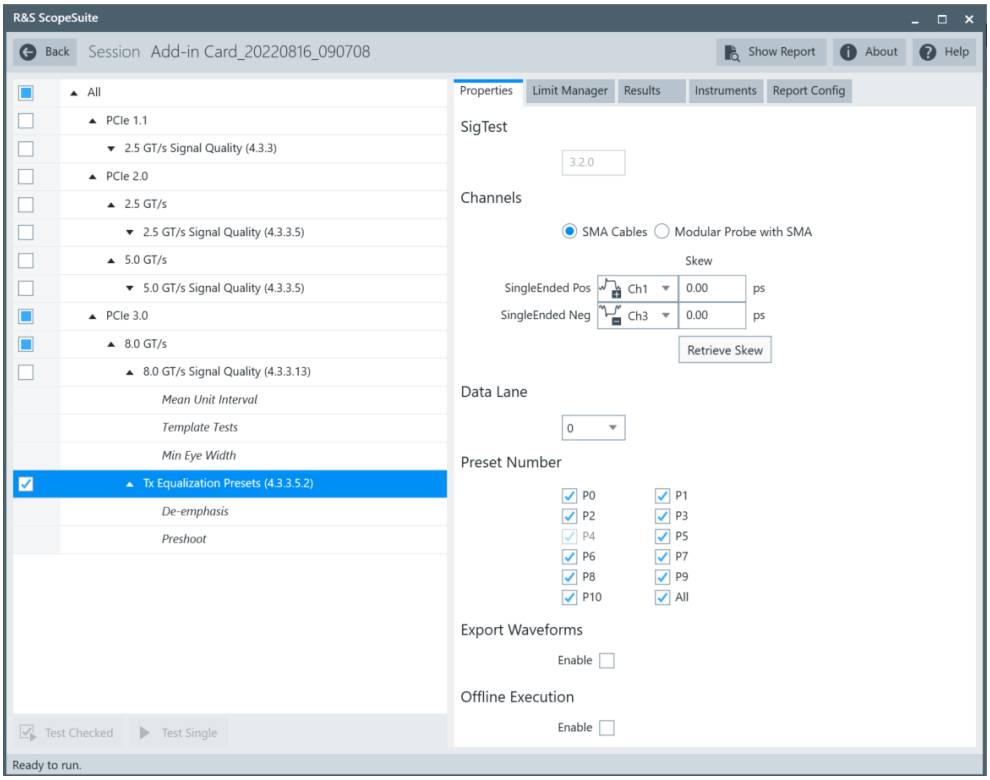
4.3.2.1 Test equipment

Table 4-3: Equipment for signal quality add-in card tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S R&S RTP with at least 16 GHz bandwidth and (40 GS/s available)	1
Compliance Base Board[1]	PCISIG Gen 3.0 Compliance Base Board (CBB)	1
SMP to SMA cables	Connected to SMP probing points on CBB	2
DUT	Add-In Card	1
Signal generator (optional)	R&S R&S RTP -B6 Option SMP to SMA cable	1
DC block (optional)	DC Block, BLK-222+, 50 Ohm, 0.01-2.2 GHz	1
We recommend PCI Express Compliance Base Board (CBB3.0) from PCI-SIG.		

4.3.2.2 Performing the tests

1. Start the test as described in Chapter 4.1, "Starting Add-in Card tests", on page 22.
2. Select the "Tx Equalization Presets (4.3.3.5.2)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

4.3.2.3 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

These tests use PCI Express Compliance Base Board (CBB3.0) from PCI-SIG. The CBB test fixture provides SMP Probing Points for data lanes that are used to connect to the oscilloscope.

4.3.2.4 Measurements

This test does the following measurements described in table 4-16 of section 4.3.3.5.2 of PCI Express Base Specification, REV. 3.0 and Section 4.7.1 of the Card Electromechanical Specification, REV 3.0.

- P0-P10 De-emphasis
- P0-P10 Preshoot

5 System board tests

5.1 Starting system board tests

Before you run the test, complete the following actions:

- Initial setup of the equipment, see Chapter 2.2, "Installing software and license", on page 8
- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

1. Select "PCIe" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, set "Select Type" > "System Board".
3. Add a new test session and open it, see Chapter 3.1, "Starting a test session", on page 14.
4. Check the test configuration settings and adjust, if necessary. See:
   - Chapter 3.2.2, "PCIe test configuration", on page 18
   - Chapter 3.2.1.1, "Limit manager", on page 17
5. Select/check the test cases you want to run and click "Test Single"/"Test checked".
6. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

5.2 PCIe 1.1 / PCIe 2.0

5.2.1 Signal Quality test

5.2.1.1 Test equipment

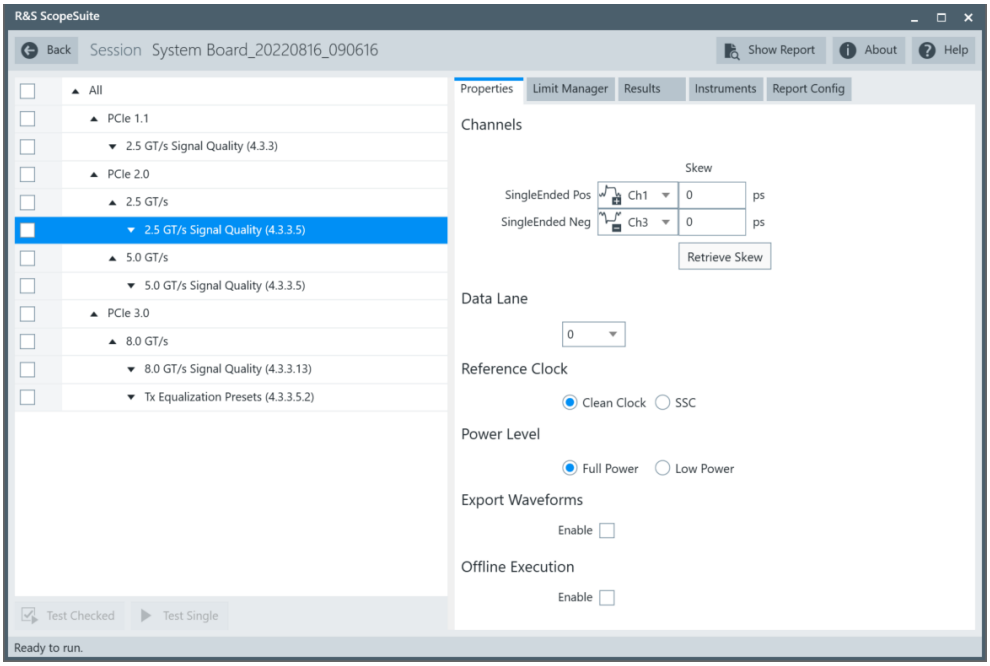
Table 5-1: Equipment for Signal Quality system board tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
Compliance load board[1]	PCISIG Gen 2.0 Compliance Load Board (CLB)	1
SMP to SMA cables	Connected to SMP probing points on CLB	2

Item	Description, model	Quantity
DUT	System board	1
We recommend PCI Express Compliance Load Board (CLB2.0) from PCI-SIG. For details, refer to http://pcisig.com/pci-express-compliance-load-board-clb		

5.2.1.2 Performing the tests

1. Start the test as described in Chapter 5.1, "Starting system board tests", on page 28.
2. Select the "Signal Quality (4.3.3)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

5.2.1.3 Purpose

This test verifies that the transmitter signal complies with the quality requirements in section 4.3.3 of PCI Express Base Specification, REV. 1.1.

This group of test cases is typically performed on PCI Express motherboard.

5.2.1.4 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640 bit Jitter test pattern designed to maximize data dependent jitter.

These tests use PCI Express Compliance Load Board (CLB2.0) from PCI-SIG. The CLB test fixture provides SMP Probing Points for data lanes that are used to connect to the oscilloscope.

Refer to Compliance Load Board (CLB2.0) Test Fixture User's Document for details.

5.2.1.5 Measurements

This test does following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 1.1 and Section 4.7.3 of the Card Electromechanical Specification, REV 1.1.

- Mean Unit Interval (UI)
- Data Rate
- Template Tests
- Min Eye Width ($T_{TX\text{-}EYE}$)
- Median To Max Jitter ($T_{TX\text{-}EYEMEDIAN\text{-}to\text{-}MAXJITTER}$)
- Differential Output Voltage ($V_{TX\text{-}DIFFp\text{-}p}$)

5.3 PCIe 3.0

PCIe 3.0 compliance tests require option R&S RTP- K83.

5.3.1 Signal Quality test

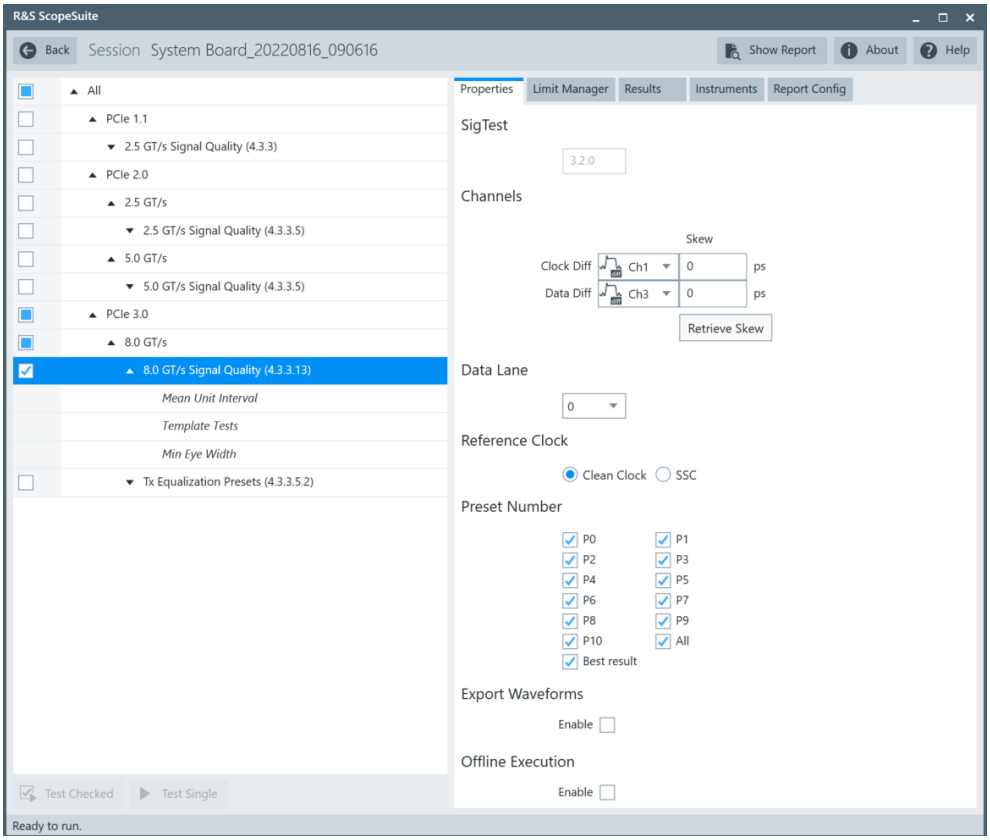
5.3.1.1 Test equipment

Table 5-2: Equipment for Signal Quality system board tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S R&S RTP with at least 16 GHz bandwidth and (40 GS/s available)	1
Compliance load board[1]	PCISIG Gen 3.0 Compliance Load Board (CLB)	1
Probe and probe tip	R&S RTP-ZM160 Modular probe R&S RTP-ZMA140 amplifier probe tip	
SMP to SMA cables	Connected to SMP probing points on CLB	4
DUT	System board	1
DC block (optional)	DC Block, BLK-222+, 50 Ohm, 0.01-2.2 GHz	1
We recommend PCI Express Compliance Load Board (CLB 3.0) from PCI-SIG.		

5.3.1.2 Performing the tests

1. Start the test as described in Chapter 5.1, "Starting system board tests", on page 28.
2. Select the "Signal Quality (4.3.3.13)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

5.3.1.3 Purpose

This test verifies that the transmitter signal complies with the quality requirements in section 4.3.3.13 of PCI Express Base Specification, Rev. 3.0.

This group of test cases is typically performed on PCI Express motherboard.

5.3.1.4 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

These tests use PCI Express Compliance Load Board (CLB3.0) from PCI-SIG. The CLB test fixture provides SMP Probing Points for data lanes that are used to connect to the oscilloscope.

For the test setup, a DC block needs to be connected to the WaveGen (B6), if the pre-set test mode is unable to trigger properly.

If the preset test mode is unable to trigger properly, a DC block needs to be attached to the WaveGen (B6).

Refer to Compliance Load Board (CLB3.0) Test Fixture User's Document for details.

5.3.1.5 Measurements

This test does the following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 3.0 and Section 4.7.3 of the Card Electromechanical Specification, REV 3.0.

- Mean Unit Interval (UI)
- Data Rate
- Template Tests
- Min Eye Width

5.3.2 Tx Equalization presets

See Chapter 4.3.2, "Tx Equalization presets", on page 26.

6 Receiver tests

6.1 Starting receiver tests

Before you run the test, complete the following actions:

- Initial setup of the equipment, see Chapter 2.2, "Installing software and license", on page 8
- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

1. Select "PCIe" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, set "Select Type" > "Receiver (Rev1 and Rev2)".
3. Add a new test session and open it, see Chapter 3.1, "Starting a test session", on page 14.
4. Check the test configuration settings and adjust, if necessary. See:
   - Chapter 3.2.2, "PCIe test configuration", on page 18
   - Chapter 3.2.1.1, "Limit manager", on page 17
5. Select/check the test cases you want to run and click "Test Single"/"Test checked".
6. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

6.2 Signal Quality test

6.2.1 Test equipment

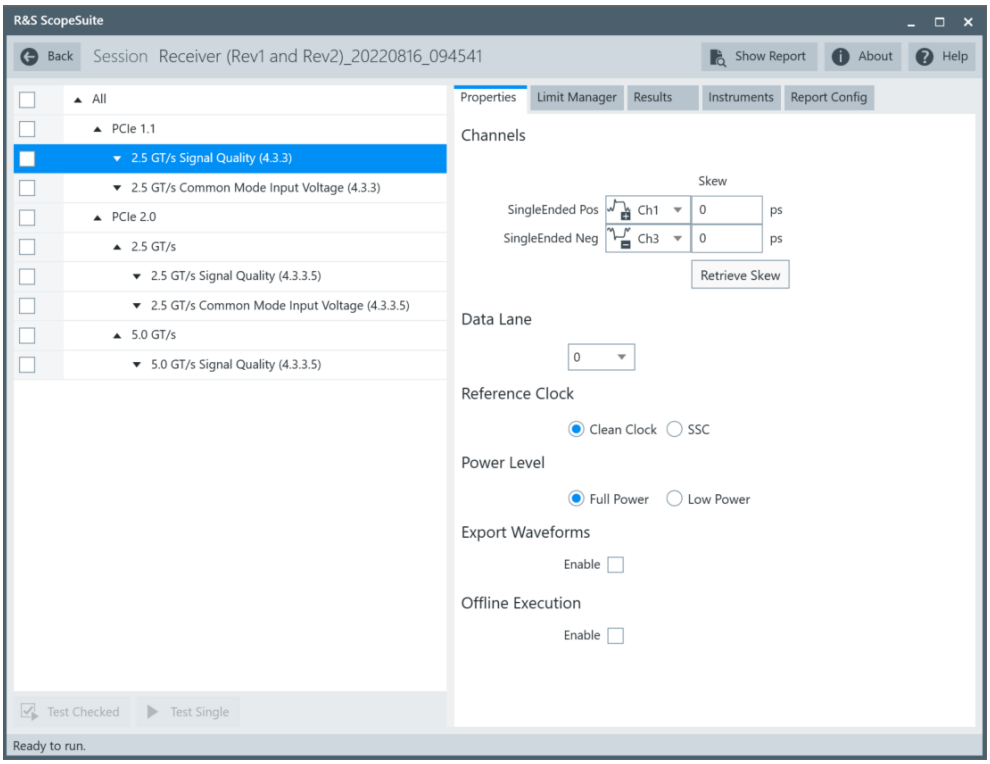
Table 6-1: Equipment for Signal Quality receiver tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
SMP to SMA cable	Connected to SMP probing points on CLB	2
DUT	The evaluation board	1

6.2.2 Performing the tests

1. Start the test as described in Chapter 6.1, "Starting receiver tests", on page 34.

2. Select the "Signal Quality (4.3.3)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.

4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

6.2.3 Purpose

This test verifies that the receiver signal complies with the quality specifications in section 4.3.4 of PCI Express Base Specification, REV. 1.1.

6.2.4 Test setup

The test requires the DUT to receive the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

Receiver tests are done by probing the link as close as possible to the pins of the receiver device. The following figure shows the probing method.

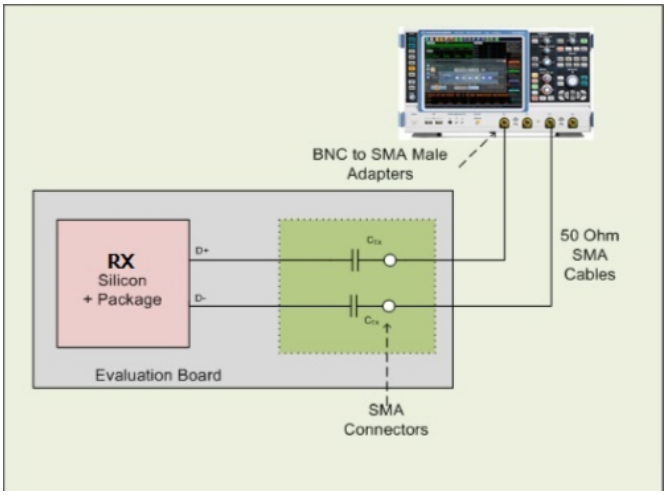


Figure 6-1: Probing with single-ended active probes

6.2.5 Measurements

This test does following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 1.1

- Mean Unit Interval (UI)
- Data Rate
- Template Tests
- Min Eye Width (T_{TX-EYE})
- Median To Max Jitter ($T_{TX-EYEMEDIAN-to-MAXJITTER}$)
- Differential Input Voltage ($V_{RX-DIFFp-p}$)
- AC Peak Common Mode Input Voltage
- Total Jitter at BER-12 (PCIe 2.0 only)
- Deterministic jitter (PCIe 2.0 only)
- RMS jitter (PCIe 2.0 only)

7 Transmitter tests

7.1 Starting transmitter tests

Before you run the test, complete the following actions:

- Initial setup of the equipment, see Chapter 2.2, "Installing software and license", on page 8
- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

1. Select "PCIe" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, set "Select Type" > "Transmitter (Rev1 and Rev2)".
3. Add a new test session and open it, see Chapter 3.1, "Starting a test session", on page 14.
4. Check the test configuration settings and adjust, if necessary. See:
   - Chapter 3.2.2, "PCIe test configuration", on page 18
   - Chapter 3.2.1.1, "Limit manager", on page 17
5. Select/check the test cases you want to run and click "Test Single"/"Test checked".
6. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

7.2 PCIe 1.1 / PCIe 2.0

7.2.1 Signal Quality test

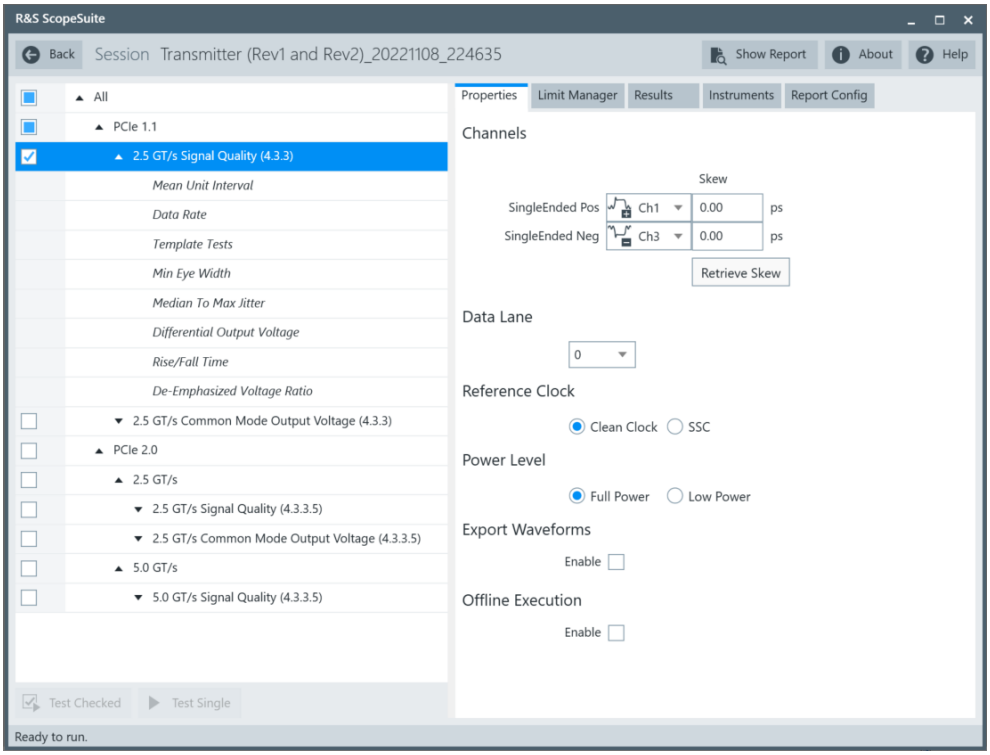
7.2.1.1 Test equipment

Table 7-1: Equipment for Signal Quality transmitter tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
SMP to SMA cable	Connected to SMP probing points on CLB	2
DUT	The evaluation board	1

7.2.1.2 Performing the tests

1. Start the test as described in Chapter 7.1, "Starting transmitter tests", on page 37.
2. Select the "Signal Quality (4.3.3)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

7.2.1.3 Purpose

This test verifies that the transmitter signal complies with the quality specifications in section 4.3.3 of PCI Express Base Specification, REV. 1.1.

7.2.1.4 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

The following figure shows the probing method for transmitter "Signal Quality" tests.

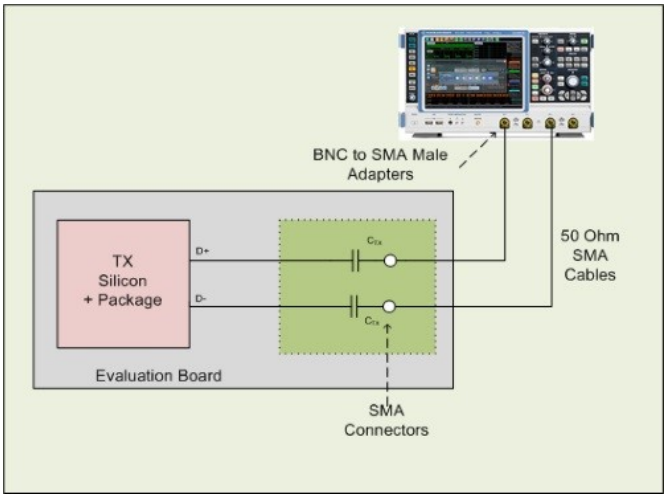


Figure 7-1: Probing with SMA cables

7.2.1.5 Measurements

This test does following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 1.1

- Mean Unit Interval (UI)
- Data Rate
- Template Tests
- Min Eye Width (T_{TX-EYE})
- Median To Max Jitter ($T_{TX-EYEMEDIAN-to-MAXJITTER}$)
- Differential Output Voltage ($V_{TX-DIFFp-p}$)
- Rise/Fall Time ($T_{TX-RISE}$,$T_{TX-FALL}$)
- De-Emphasized Voltage Ratio ($V_{TX-DE-RATIO}$)

7.2.2 Common Mode Output Voltage test

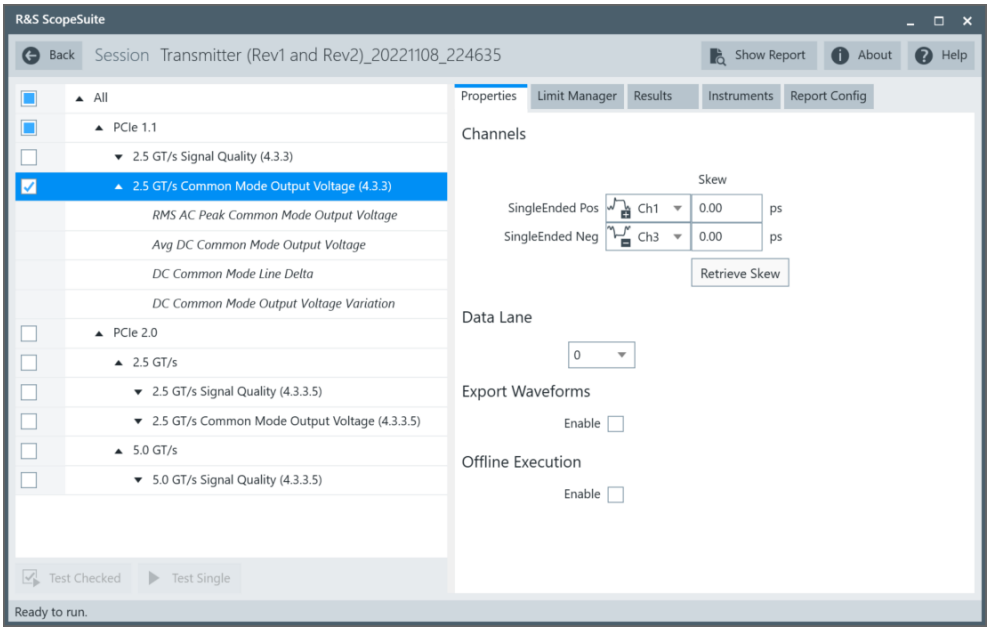
7.2.2.1 Test equipment

Table 7-2: Equipment for Common Mode Output Voltage transmitter tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
SMP to SMA cables	Connected to SMP probing points on CBB	2
DUT	The evaluation board	1

7.2.2.2 Performing the tests

1. Start the test as described in Chapter 7.1, "Starting transmitter tests", on page 37.
2. Select the "Common Mode Output Voltage (4.3.3)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

7.2.2.3 Purpose

This test verifies that the transmitter signal complies with the common mode voltage requirements described in section 4.3.3 of PCI Express Base Specification, REV. 1.1.

7.2.2.4 Test setup

The test requires the DUT to transmit the Compliance Pattern defined in section 4.2.8 (Base Specification). This is 640-bit Jitter test pattern designed to maximize data-dependent jitter.

The following figure shows the probing method for transmitter "Common Mode Output Voltage (4.3.3)" tests.

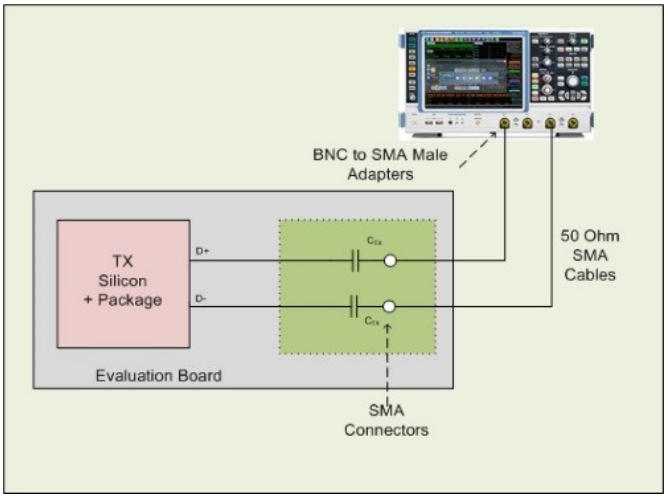


Figure 7-2: Probing with SMA cables

7.2.2.5 Measurements

This test does following measurements described in table 4-5 at section 4.3.3 of PCI Express Base Specification, REV. 1.1

- RMS AC Peak Common Mode Output Voltage ($V_{TX\text{-}CM\text{-}ACp}$)
- Average DC Common Mode Output Voltage ($V_{TX\text{-}DC\text{-}CM}$)
- DC Common Mode Line Delta ($V_{TX\text{-}CM\text{-}DCLINE\text{-}DELTA}$)
- DC Common Mode Output Voltage Variation ($V_{TX\text{-}DC\text{-}CM\text{-}VARIATION}$)

8 Reference clock tests

8.1 Starting reference clock tests

Before you run the test, complete the following actions:

- Initial setup of the equipment, see Chapter 2.2, "Installing software and license", on page 8
- LAN connection of the oscilloscope and the computer running the R&S ScopeSuite, see Chapter 2.5, "Connecting the R&S RTO/RTO6/RTP", on page 9

1. Select "PCIe" in the R&S ScopeSuite start window.
2. In the "Session Selection" dialog, set "Select Type" > "Reference Clock".
3. Add a new test session and open it, see Chapter 3.1, "Starting a test session", on page 14.
4. Check the test configuration settings and adjust, if necessary. See:
   - Chapter 3.2.2, "PCIe test configuration", on page 18
   - Chapter 3.2.1.1, "Limit manager", on page 17
5. Select/check the test cases you want to run and click "Test Single"/"Test checked".
6. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

8.2 PCIe 1.1 Reference clock tests

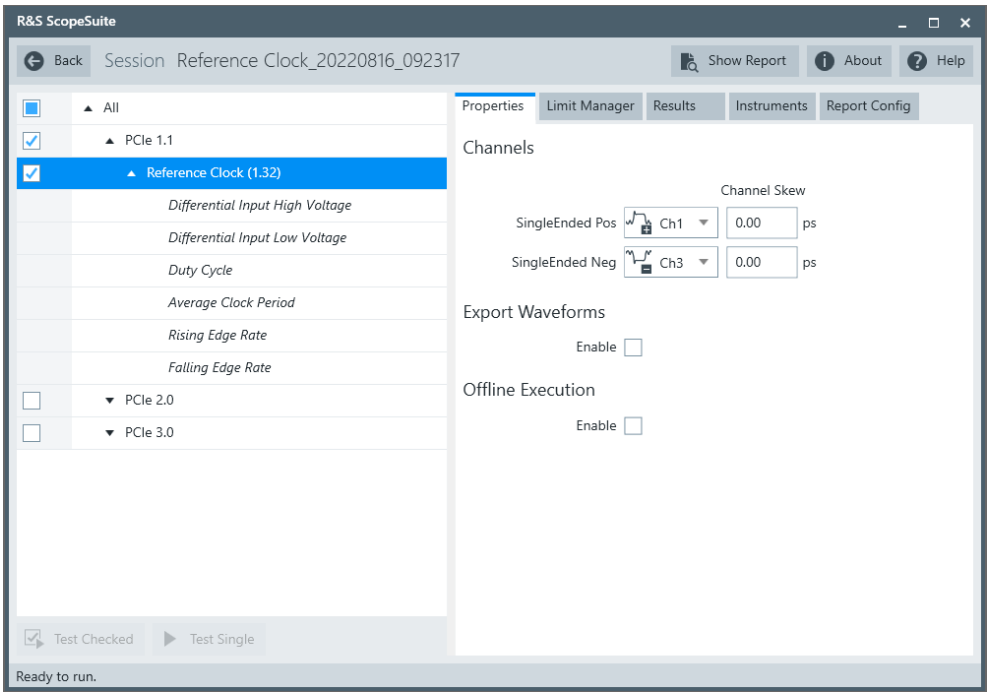
8.2.1 Test equipment

Table 8-1: Equipment for Reference Clock system board tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
Compliance Load Board[1]	PCISIG Gen 2.0 Compliance Load Board (CLB)	1
SMP to SMA cable	Connected to SMP probing points on CLB	2
DUT	System board	1
We recommend PCI Express Compliance Load Board (CLB2.0) from PCI-SIG. For details, refer to http://pcisig.com/pci-express-compliance-load-board-clb		

8.2.2 Performing the tests

1. Start the test as described in Chapter 8.1, "Starting reference clock tests", on page 42.
2. Select "PCIe 1.1" > "Reference Clock (1.3.2)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

8.2.3 Purpose

The purpose of Reference Clock tests is to verify various requirements specific to Reference Clock under Rev 1.1 of the PCI Express Card Electromechanical Specification.

This group of test cases is typically performed on PCI Express motherboard.

8.2.4 Test setup

This group of tests uses PCI Express Compliance Load Board (CLB2.0) from PCI-SIG. The CLB test fixture provides Reference Clock SMP Probing Points that are used to connect the system reference clock to the oscilloscope.

Refer to Compliance Load Board (CLB2.0) Test Fixture User's Document for details.

Channel 1 is connected to Ref Clk P and Channel 2 is connected to Ref Clk N.

8.2.5 Test cases

Reference Clock tests consist of 6 test cases which perform related system reference clock test and measurement defined in Rev 1.1 of the PCI Express Card Electromechanical Specification.

8.2.5.1 Differential input high voltage - VIH

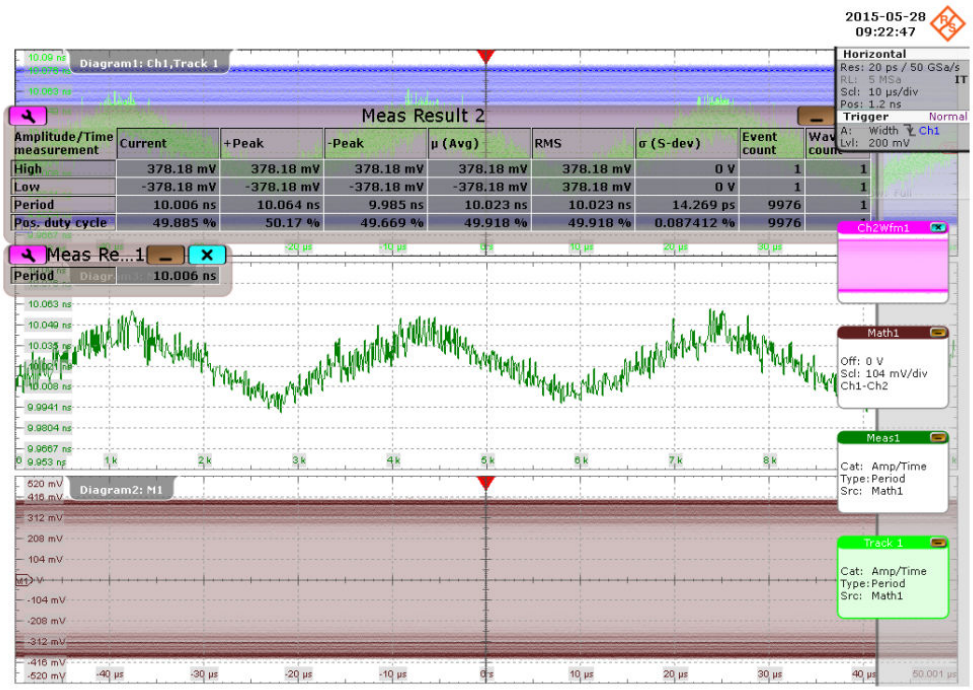
Purpose

The purpose of this test case is to verify the Differential Input High Voltage of reference clock is within the compliance limits. Refer to Section 2.1.3 of the Card Electromechanical Specification Rev. 1.1 for details.

Measurements

The software firstly commands R&S RTO/ RTO6 /RTP to generate a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. Then a statistics measurement of High is performed over the differential clock signal. Avg value is used as test result.

The conformance range for VIH is greater than 150 mV.



8.2.5.2 Differential input low voltage - VIL

Purpose

The purpose of this test case is to verify the Differential Input Low Voltage of reference clock is within the compliance limits. Refer to Section 2.1.3 of the Card Electromechanical Specification Rev. 1.1 for details.

Measurements

The software firstly commands R&S RTO/ RTO6 /RTP to generate a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. Then a statistics measurement of Low is performed over the differential clock signal. Avg value is used as test result.

The conformance range for VIL is less than -150 mV.

8.2.5.3 Duty cycle

Purpose

The purpose of this test case is to verify the Duty Cycle of reference clock is within the compliance limits. Refer to Section 2.1.3 of the Card Electromechanical Specification Rev. 1.1 for details.

Measurements

The software firstly commands R&S RTO/ RTO6 /RTP to generate a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. Then a statistics measurement of Pos. Duty Cycle is performed over the differential clock signal. Avg value is used as test result.

The conformance range for Duty Cycle is greater than or equal to 40% and less than or equal to 60%.

8.2.5.4 Average clock period PPM

Purpose

The purpose of this test case is to verify the Average Clock Period of reference clock is within the compliance limits. Refer to Section 2.1.3 of the Card Electromechanical Specification Rev. 1.1 for details.

Measurements

The software firstly commands R&S RTO/ RTO6 /RTP to generate a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. Then a statistics measurement of Period is performed over the differential clock signal. Avg value is recorded and sent to the software for Average Clock Period PPM calculation.

The conformance range for Average Clock Period is greater than or equal to -300 ppm and less than or equal to 2800 ppm.

8.2.5.5 Rising edge rate

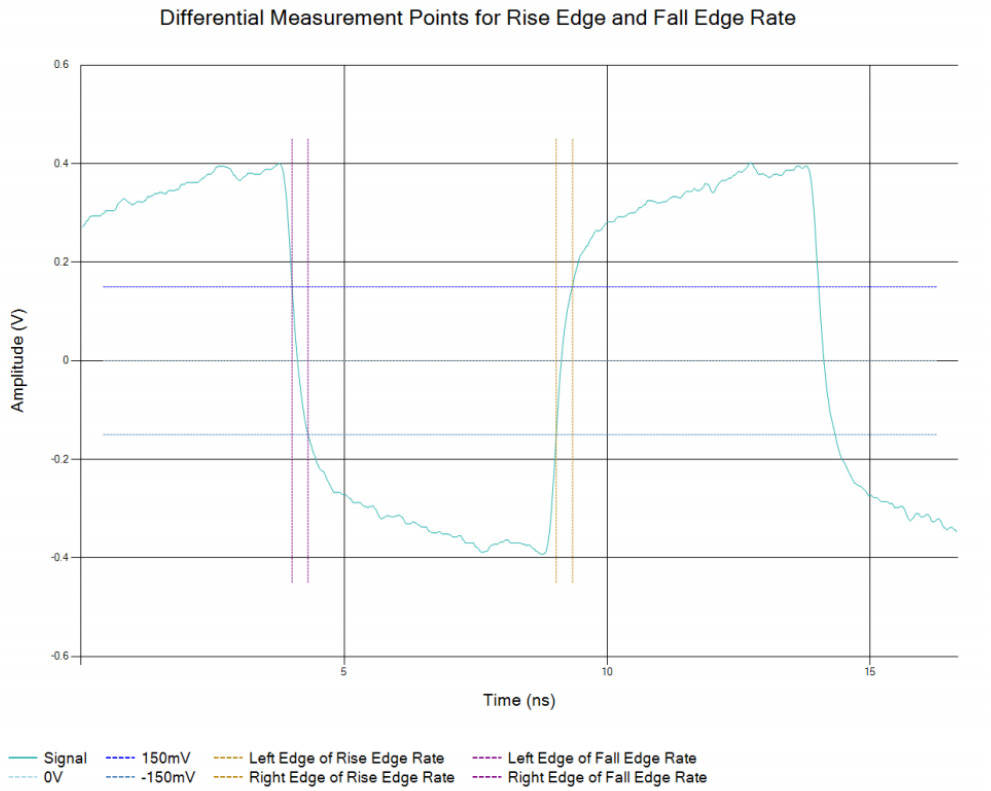
Purpose

The purpose of this test case is to verify the Rising Edge Rate of reference clock is within the compliance limits. Refer to Section 2.1.3 of the Card Electromechanical Specification Rev. 1.1 for details.

Measurements

The software firstly commands R&S RTO/ RTO6 /RTP to generate a differential signal of the reference clock (Refclk+ minus Refclk-) via MATH function. Then the differential clock signal is transferred to the software for post processing. The 300mV measurement window is centered on the differential zero crossing from -150mV to 150mV. Average rising edge rate of all cycles are used as test result.

The conformance range for Rising Edge Rate is greater than or equal to 0.6V/ns and less than or equal to 4.0V/ns.



8.2.5.6 Falling edge rate

Purpose

The purpose of this test case is to verify the Falling Edge Rate of reference clock is within the compliance limits. Refer to Section 2.1.3 of the Card Electromechanical Specification Rev. 1.1 for details.

Measurements

The software firstly commands R&S RTO/ RTO6 /RTP to generate a differential signal of the reference clock (Refclk+ minus Refclk-) via MATH function. Then the differential clock signal is transferred to the software for post processing. The 300mV measurement window is centered on the differential zero crossing from -150mV to 150mV. An average of the falling edge rate of all cycles are used as test result.

The conformance range for Falling Edge Rate is greater than or equal to 0.6V/ns and less than or equal to 4.0V/ns.

8.3 PCIe 2.0 Reference clock tests

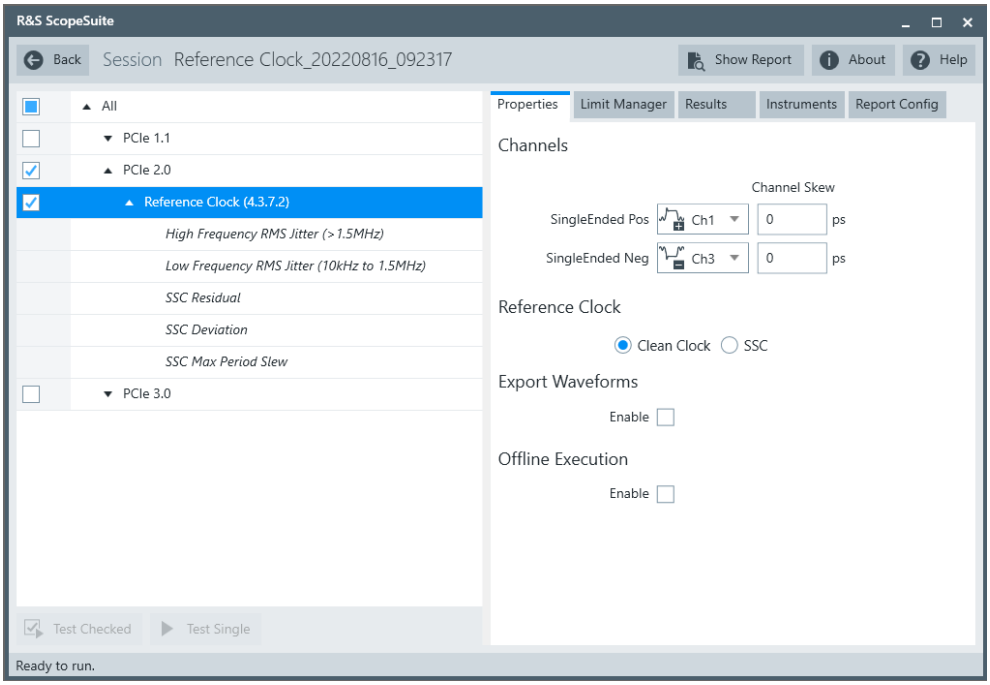
8.3.1 Test equipment

Table 8-2: Equipment for Reference Clock system board tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTO/ RTO6 /RTP with at least 6 GHz bandwidth and (20 GS/s available)	1
Compliance Load Board[1]	PCISIG Gen 2.0 Compliance Load Board (CLB)	1
SMP to SMA cable	Connected to SMP probing points on CLB	2
DUT	System board	1
We recommend PCI Express Compliance Load Board (CLB2.0) from PCI-SIG. For details, refer to http://pcisig.com/pci-express-compliance-load-board-clb		

8.3.2 Performing the tests

1. Start the test as described in Chapter 8.1, "Starting reference clock tests", on page 42.
2. Select "PCIe 2.0" > "Reference Clock (4.3.7.2)" test case:



3. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.

4. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

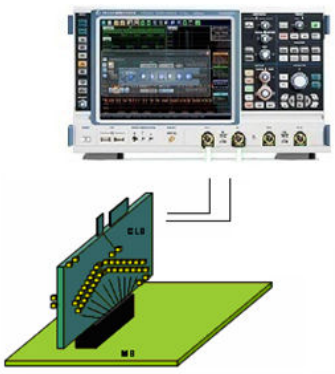
8.3.3 Purpose

The purpose of Reference Clock tests is to verify various requirements specific to Reference Clock of PCI Express Base Specification, Rev. 2.1

This group of test cases is typically performed on PCI Express motherboard.

8.3.4 Test setup

This group of tests uses PCI Express Compliance Load Board (CLB2.0) from PCI-SIG. The CLB test fixture provides Reference Clock SMP Probing Points that are used to connect the system reference clock to the oscilloscope.



Refer to Compliance Load Board (CLB2.0) Test Fixture User's Document for details.

Channel 1 is connected to Ref Clk P and Channel 2 is connected to Ref Clk N.

8.3.5 Test cases

Reference Clock tests consist of 5 test cases which perform related system reference clock test and measurement defined in Rev 1.1 of the PCI Express Card Electromechanical Specification.

8.3.5.1 High Frequency RMS Jitter (>1.5MHz)

Purpose

The purpose of this test case is to verify that the jitter component > 1.5MHz of common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 2.1, section 4.3.7.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. The differential signal will be transferred to the software for post processing to extract only RMS jitter > 1.5MHz.

The conformance range for High Frequency Jitter is less than 3.1ps RMS.

8.3.5.2 Low Frequency RMS Jitter (10kHz to 1.5MHz)

Purpose

The purpose of this test case is to verify that the jitter component from 10kHz to 1.5MHz of common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 2.1, section 4.3.7.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. The differential signal will be transferred to the software for post processing to extract RMS jitter between 10kHz to 1.5MHz. The conformance range for Low Frequency Jitter is less than 3.0ps RMS.

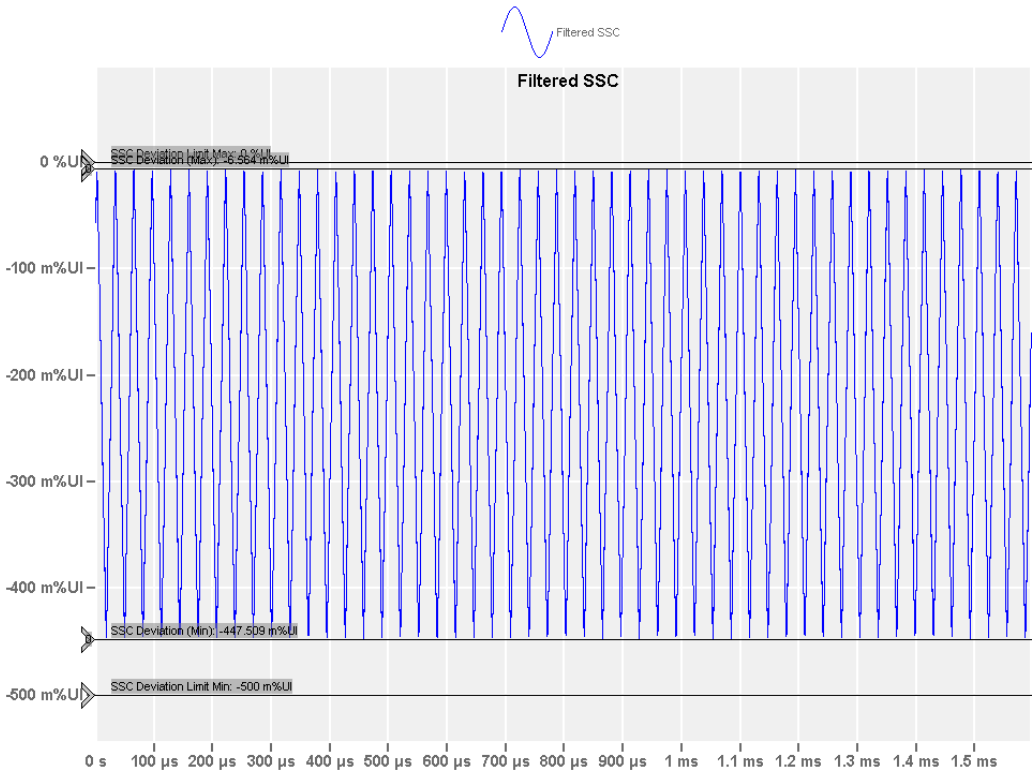
8.3.5.3 SSC Residual

Purpose

The purpose of this test case is to verify that the residual SSC jitter of common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 2.1, section 4.3.7.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. The differential signal will be transferred to the software for post processing to extract jitter after removing effect of SSC. The conformance range for SSC Residual is less than 75ps. The following picture show a SSC waveform extracted from a SSC-enabled reference clock.



8.3.5.4 SSC Deviation

Purpose

The purpose of this test case is to verify that the deviation of the SSC for SSC-enabled common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 2.1, section 4.3.7.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. SSC is extracted by analyzing all clock cycles after removing high frequency jitter components. The maximum and minimum length of the clock cycles are measured as deviation.

The conformance range for SSC Deviation is within 0 to 0.5%.

8.3.5.5 SSC Max Period Slew

Purpose

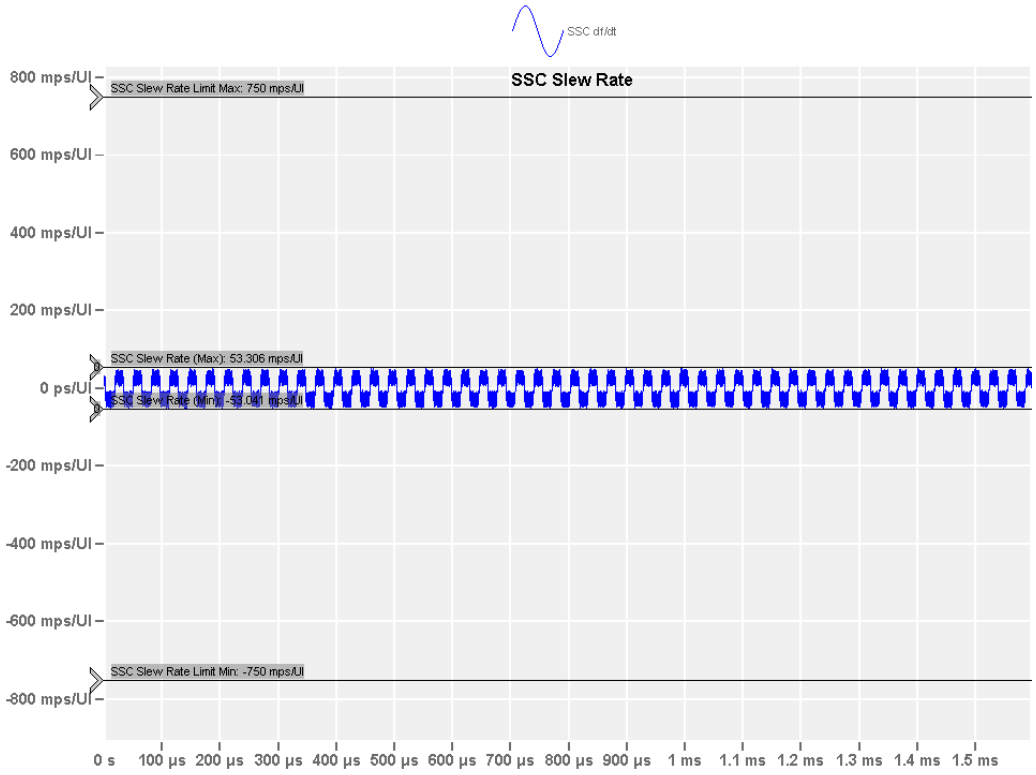
The purpose of this test case is to verify that the maximum slew rate of the SSC for SSC-enabled common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 2.1, section 4.3.7.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. SSC is extracted by analyzing all clock cycles after removing high frequency jitter components. The rate of changes of SSC frequency will be analyzed and reported as slew rate. Maximum rate will be reported.

The conformance range for SSC Max Period Slew is less than 0.75 ps/UI.

The following picture shows the slew rate for the SSC waveform.



8.4 PCIe 3.0 Reference clock tests

8.4.1 Test equipment

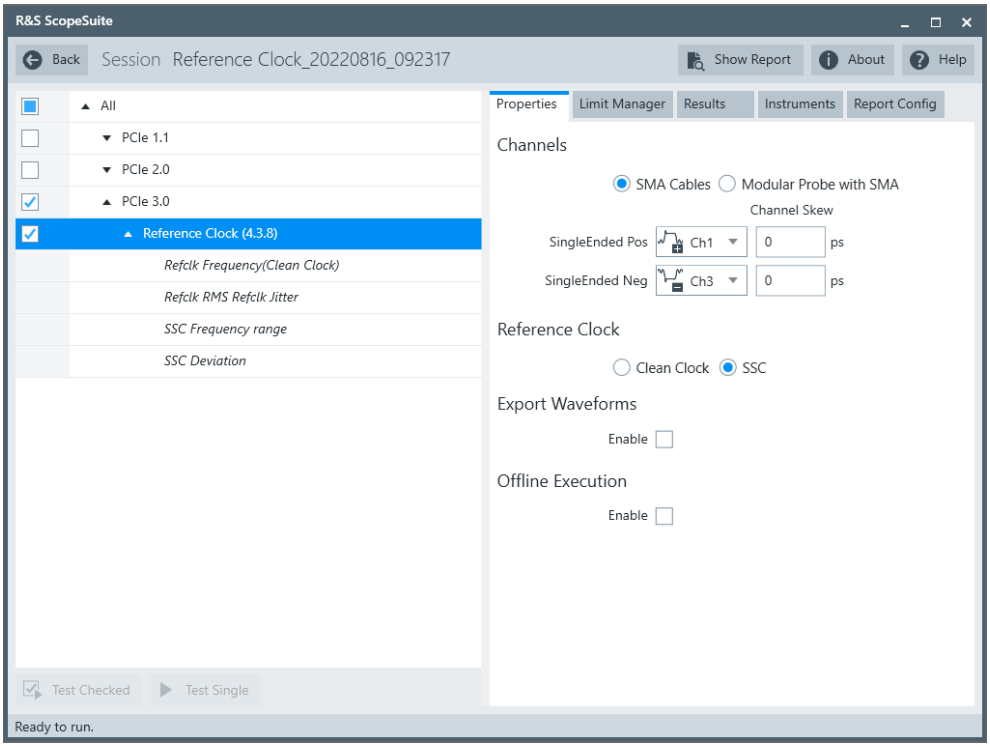
Table 8-3: Equipment for Reference Clock system board tests

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S R&S RTP with at least 16 GHz bandwidth and (20 GS/s available)	1
Compliance load board[1]	PCISIG Gen 3.0 Compliance Load Board (CLB)	1
SMP to SMA cable	Connected to SMP probing points on CLB	2

Item	Description, model	Quantity
DUT	System board	1
We recommend PCI Express Compliance Load Board (CLB3.0) from PCI-SIG.		

8.4.2 Performing the tests

1. Start the test as described in Chapter 8.1, "Starting reference clock tests", on page 42.
2. Select "PCIe 3.0" > "Reference Clock (4.3.8)" test case:



3. For spread spectrum clocking (SSC) reference clock tests, ensure that the SSC settings are activated through the system board's BIOS.
4. Click "Test Single" to run only the selected test case.
   Click "Test Checked" to run all test cases that are checked on the tree.
5. Follow the instructions of the step-by step guide.
   When you have finished all steps, the compliance test runs automatically.

8.4.3 Purpose

The purpose of Reference Clock tests is to verify various requirements specific to Reference Clock under Rev 3.0 of the PCI Express Card Electromechanical Specification.

This group of test cases is typically performed on PCI Express motherboard.

8.4.4 Test setup

This group of tests uses PCI Express Compliance Load Board (CLB3.0) from PCI-SIG. The CLB test fixture provides Reference Clock SMP Probing Points that are used to connect the system reference clock to the oscilloscope.

Refer to Compliance Load Board (CLB3.0) Test Fixture User's Document for details.

8.4.5 Test cases

Reference Clock (clean clock) consist of 2 test cases. Reference Clock (SSC) consist of 2 test cases. These perform related system reference clock test and measurement defined in Rev 3.0 of the PCI Express Card Electromechanical Specification.

8.4.5.1 Refclk Frequency (Clean Clock)

Purpose

The purpose of this test case is to verify that the frequency of the clean (without SSC) common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 3.0, Section 4.3.8.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. Then a statistics measurement of frequency for all the cycles is performed over the differential clock signal. Average value of the measured frequencies will be reported.

The conformance range for SSC Frequency is within 99.97MHz and 100.03MHz.

8.4.5.2 Refclk RMS Refclk Jitter

Purpose

The purpose of this test case is to verify that the RMS jitter of the common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 3.0, Section 4.3.8.2.

Measurements

The software firstly commands the scope to construct a differential signal (REFCLK+ minus Refclk-) of the reference clock via MATH function. The differential signal will then be analyzed to calculate RMS Jitter which be the result of this test.

The conformance range for RMS Jitter is less than 1.0 ps RMS.

8.4.5.3 SSC Frequency range

Purpose

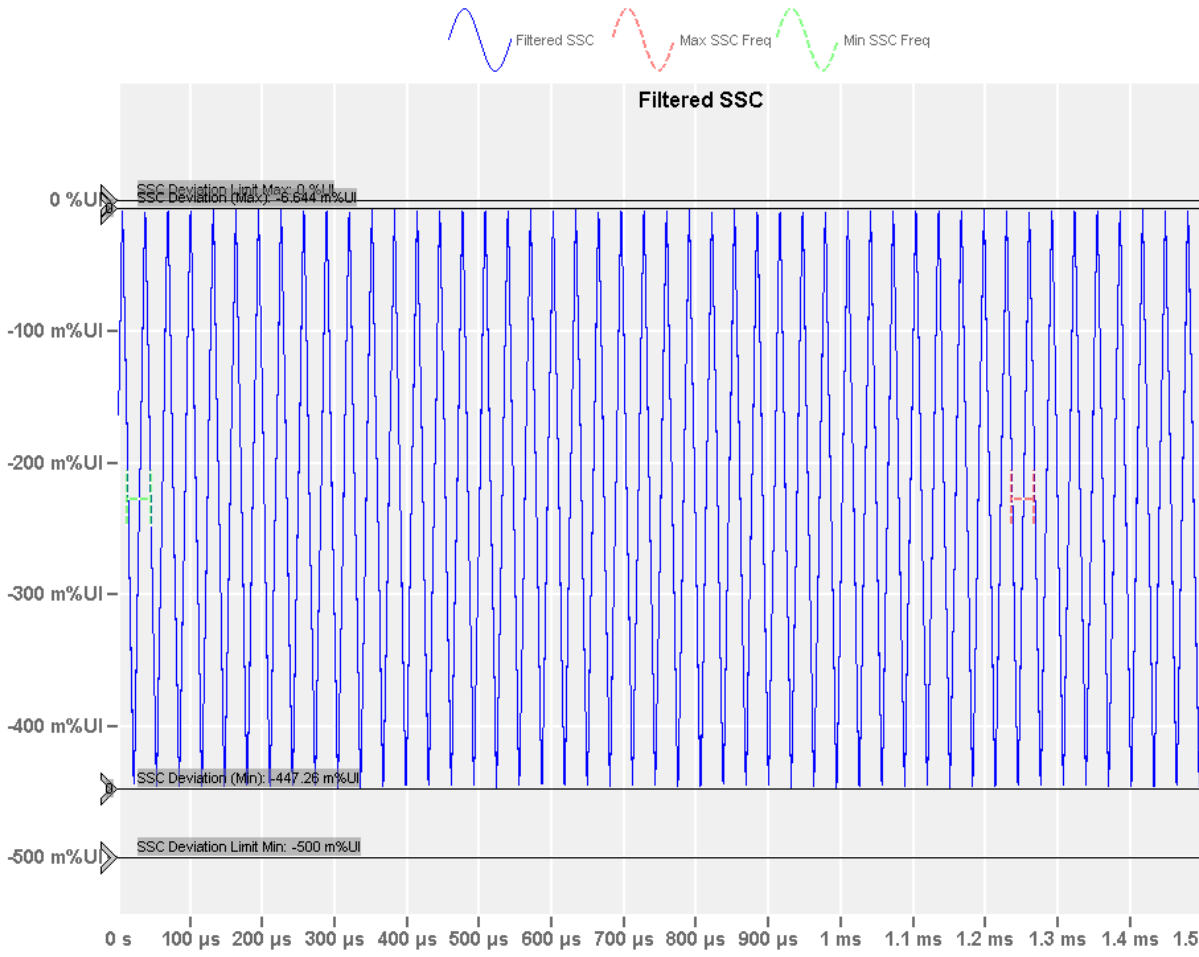
The purpose of this test case is to verify that the frequency range of the SSC of the SSC-enabled common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 3.0, Section 4.3.8.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. SSC is extracted by analyzing all clock cycle after removing high frequency jitter components. Frequency of the extracted SSC will be measured as result of the test.

The conformance range for SSC Frequency is within 30kHz to 33kHz.

The following figure shows maximum and minimum frequency measured on SSC waveform extracted from SSC-enabled reference clock.



8.4.5.4 SSC Deviation

Purpose

The purpose of this test case is to verify that the deviation of the SSC of the SSC-enabled common reference clock is within the compliance limits of the PCI Express Base Specification Rev. 3.0, Section 4.3.8.2.

Measurements

The software firstly commands the scope to construct a differential signal (Refclk+ minus Refclk-) of the reference clock via MATH function. SSC is extracted by analyzing all clock cycles after removing high frequency jitter components. The maximum and minimum length of the clock cycles are measured as deviation.

The conformance range for SSC Deviation is within 0 to 0.5%.