R&S[®]RTP-K114/-K115 DisplayPort Compliance Test User Manual





Make ideas real



This document describes the DisplayPort Compliance Test Procedures of the following options:

- R&S[®]RTP-K114 DisplayPort (DP) 1.4a compliance test (1803.6903.02)
- R&S[®]RTP-K115 Embedded DisplayPort (eDP) 1.4b/1.5 compliance test (1803.6910.02)

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1179.7640.02 | Version 01 | R&S®RTP-K114/-K115

Throughout this manual, $\mathsf{R}\&\mathsf{S}^{\circledast}$ is indicated as $\mathsf{R}\&\mathsf{S}.$

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1 R&S ScopeSuite overview

The R&S ScopeSuite software is used with R&S RTP oscilloscopes. It can be installed on a test computer or directly on the oscilloscope. For system requirements, refer to the Release Notes.



The R&S ScopeSuite main panel has several areas:

- "Settings": connection settings to oscilloscope and other instruments also default report settings
- "Compliance Tests": selection of the compliance test
- "Demo": accesses demo test cases that can be used for trying out the software without having a connection to an oscilloscope
- shift sideways to change the transparency of the dialog box
- "Help": opens the help file, containing information about the R&S ScopeSuite configuration
- "About": gives information about the R&S ScopeSuite software
- "Tile View": allows a personalization of the compliance test selection You can configure which tests are visible in the compliance test section and which are hidden, so that only the ones you use are displayed.
- ▶ To hide a test from the "Compliance Tests" view, do one of the following:

Right-click on the compliance test that you want to hide.
 The icon of the test changes, see Figure 1-1. Now with a left click you can hide the test.



Figure 1-1: Unpin icon

b) Click on "Title View" to show a list of the available test cases. By clicking a test case in the show list, you can pin/unpin it from the main panel.

2 Preparing the measurements

2.1 Test equipment

DisplayPort 1.4

For DisplayPort 1.4 compliance tests, the following test equipment is needed:

- R&S RTP with 4 channels and minimum 16 GHz bandwidth
- R&S RTP-K114 DisplayPort 1.4 compliance test option (required option, installed on the R&S RTP)
- Additional R&S RTP options:
 - Option R&S RTP-K133 or R&S RTP-K134 Advanced jitter and noise
 - Option R&S RTP-K137 Advanced eye analysis
 - Option R&S RTP-K141 high-speed serial patter trigger
- For measuring Main-Link signals you need one of the following: For one lane measurements:
 - 1 differential probe with SMA module and 16 GHz bandwidth, e.g R&S ZM160 with RT-ZMA40.
 - 2 SMA cables

For dual lane measurements:

- 2 differential probes with SMA module and 16 GHz bandwidth, e.g R&S ZM160 with RT-ZMA40.
- 4 SMA cables
- For measuring AUX CH signal:
 - 1 differential probe, e.g R&S ZM160 and 1 SMA module R&S RT-ZMA40
 - 2 single-ended probes with at least 500MHz bandwidth
- Test fixtures:
 - DisplayPort AUX controller: recommended Unigraf UCD-323 for full DUT automated control
 - Auxiliary Control test Adapter: recommended Wilder Technologies Auxiliary Control Test Adapter or equivalent
 - Embedded DisplayPort test Adapter: recommended Wilder Technologies EDP-TPA40L or equivalent
- Optional for return loss tests: vector network analyzer with frequency range from 50MHz to 12GHz, eg. R&S ZNB, R&S ZNC, R&S ZND or R&S ZVA.
- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the R&S RTP.

Embedded DisplayPort 1.4b/1.5

For Embedded DisplayPort 1.4b/1.5 compliance tests, the following test equipment is needed:

- R&S RTP with 4 channels and minimum 16 GHz bandwidth
- R&S RTP-K115 EDP 1.4 compliance test option (required option, installed on the R&S RTP)
- Additional R&S RTP options:
 - Option R&S RTP-K133 or R&S RTP-K134 Advanced jitter and noise
 - Option R&S RTP-K137 Advanced eye analysis
- For measuring Main-Link signals you need one of the following:

For one lane measurements:

- 1 differential probe with SMA module and 16 GHz bandwidth, e.g R&S ZM160 with RT-ZMA40.
- 2 SMA cables

For dual lane measurements:

- 2 differential probes with SMA module and 16 GHz bandwidth, e.g R&S ZM160 with RT-ZMA40.
- 4 SMA cables
- For measuring AUX CH signal:
 - 1 differential probe, e.g R&S ZM160 and 1 SMA module R&S RT-ZMA40
 - 2 single-ended probes with at least 500MHz bandwidth
- Test fixtures:
 - DisplayPort AUX controller: recommended Unigraf UCD-323 for full DUT automated control
 - Auxiliary Control test Adapter: recommended Wilder Technologies Auxiliary Control Test Adapter or equivalent
 - Embedded DisplayPort test Adapter: recommended Wilder Technologies EDP-TPA40L or equivalent
- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the R&S RTP.

2.2 Installing software and license

The preparation steps are performed only once for each computer and instrument that are used for testing.



Uninstall older versions of the R&S ScopeSuite

If an older version of the R&S ScopeSuite is installed, make sure to uninstall the old version before you install the new one. You can find the version number of the current installation in "Help" menu > "About". To uninstall the R&S ScopeSuite, use the Windows " Control Panel" > "Programs".

For best operation results, we recommend that the installed firmware versions of the R&S ScopeSuite and the oscilloscope are the same.

To install the R&S ScopeSuite

- Download the latest R&S ScopeSuite software from the "Software" section on the Rohde & Schwarz R&S RTP website: www.rohde-schwarz.com/product/rtp.html www.rohde-schwarz.com/product/rto.html
- 2. Install the R&S ScopeSuite software:
 - On the computer that is used for testing, or
 - On the R&S RTP.

For system requirements, refer to the Release Notes.

To install the license key on the R&S RTP

- When you got the license key of the compliance test option, enable it on the oscilloscope using [Setup] > "SW Options".
 - For a detailed description, refer to the R&S RTP user manual, chapter "Installing Options", or to the online help on the instrument.

2.3 Setting up the network

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection.

There are two ways of connection:

- LAN (local area network): It is recommended that you connect to a LAN with DHCP server. This server uses the Dynamic Host Configuration Protocol (DHCP) to assign all address information automatically.
- Direct connection of the instruments and the computer or connection to a switch using LAN cables: Assign fixed IP addresses to the computer and the instruments and reboot all devices.

To set up and test the LAN connection

- 1. Connect the computer and the instruments to the same LAN.
- 2. Start all devices.
- 3. If no DHCP server is available, assign fixed IP addresses to all devices.
- 4. Ping the instruments to make sure that the connection is established.
- 5. If VISA is installed, check if VISA can access the instruments.
 - a) Start VISA on the test computer.
 - b) Validate the VISA address string of each device.

See also:

• Chapter 2.5, "Connecting the R&S RTP", on page 10

2.4 Starting the R&S ScopeSuite

To start the R&S ScopeSuite on the test computer or on the oscilloscope:

Double-click the R&S ScopeSuite program icon.

To start the R&S ScopeSuite on the instrument, in the R&S RTP firmware:

▶ In the "Apps" dialog, open the "Compliance" tab.

2.5 Connecting the R&S RTP

If the R&S ScopeSuite is installed directly on the instrument, the software detects the R&S RTP firmware automatically, and the "Oscilloscope" button is not available in the R&S ScopeSuite.

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection, see Chapter 2.3, "Setting up the network", on page 9. The R&S ScopeSuite software needs the IP address of the oscilloscope to establish connection.

- 1. Start the R&S RTP.
- 2. Start the R&S ScopeSuite software.
- 3. Click "Settings" > "Oscilloscope".

Connecting the R&S RTP

R&S ScopeSuite						•	_ 🗆 ×
					Tile	View 🚺 About	P Help
Settings	Compliance Tes	its					
Oscilloscope	Ethernet	금급 IG등을	USB3.2-RX	DisplayPort	Demo		
D Instruments	Ethernet 2.5/5/10G	Signal Si	DDR3	MIPI D-PHY			
Report	10BASE-T1	PCIe	DDR4	MIPI C-PHY			
	100M C	USB	НДМІ	eMMC			
Welcome to complia	aco toste coloction con	202					
welcome to compliar	ice rests selection sch	cen					

- Enter the IP address of the oscilloscope. To obtain the IP address: press the Rohde & Schwarz logo at the top-right corner of the oscilloscope's display.
- 5. Click "Get Instrument Information".

The computer connects with the instrument and gets the instrument data.

RSScopeSuite		_ 🗆 ×
G Back Oscilloscope Settings	1 About	P Help
Oscilloscope		
IP address: 10.113.10.30		
Get Instrument Information		
Device: RTO		
Serial Number: 400132		
Firmware Version: 2.60.2.7		
Restore Settings On Exit. () Never () Ask () Always		
Connect software to your RTO.		

If the connection fails, an error message is shown.

2.6 Connecting the vector network analyzer

The vector network analyzer (VNA) is required to perform Ethernet return loss measurements.

Similar to the AWG, the VNA can be used in automatic or manual mode. You can use the automatic mode only with supported instruments. A LAN connection and a VISA installation on the computer that is running the R&S ScopeSuite is required. If the R&S ScopeSuite is installed on the R&S RTP, no installation is needed because VISA is already installed on the instrument.

For manual test execution, it is recommended to use one of the listed VNAs. Moreover, any VNA can be used that meets the following requirements:

- S11 parameter measurements are possible
- Can export trace data in Touchstone (*.s1p) or *.csv format
- Supports frequency range 1 MHz to 500 MHz

In manual mode, you connect the vector network analyzer to the test board and configure the instrument manually.

To connect the vector network analyzer for automatic testing

1. Connect the computer and the VNA and set up the LAN connection, see Chapter 2.3, "Setting up the network", on page 9.

- In the R&S ScopeSuite, click "Instruments".
- 3. Click the "VNA" tab.
- 4. Select the "Automatic" operating mode.
- 5. Select the "VNA Type" and enter its IP address.
- 6. Click "Get Instrument Information".

The computer or R&S RTP connects with the instrument and retrieves the instrument data.

To connect the vector network analyzer for automatic testing

- 1. Connect the computer and the VNA. Set up the LAN connection, see Chapter 2.3, "Setting up the network", on page 9.
- 2. In the R&S ScopeSuite, click "Instruments".
- 3. Click the "VNA" tab.
- 4. Select the "Automatic" operating mode.
- 5. Select the "VNA Type" and enter its IP address.

Report configuration

RSScopeSuite	-	- ×
🕒 Back Instruments Se	ttings 1 About	Help
AWG VNA SA		
Vector Network Analyzer		
Operating Mode	Automatic v	
VNA Type	ZVL 💌	
IP Address:	10.10.10.10	
	Get Instrument Information	
Device:		
Serial Number:		
Firmware Version:		
Configure default settings for new	session	

6. Click "Get Instrument Information".

The computer or R&S RTP connects with the instrument and retrieves the instrument data.

2.7 Report configuration

In the "Report Configuration" menu, you can select the format of the report and the details to be included in the report. You can also select an icon that is displayed in the upper left corner of the report.

Also, you can enter common information on the test that is written in the "General Information" section of the test report.

Report configuration

R&S ScopeSuite			_ 🗆 ×
G Back Report Settings			1 About P Help
Content	Format	Icon	
Display Summary 📝	PDF	Change	
Display Detail 📝	O Word Document	\checkmark	
Display Properties 📝			
Display Screenshots 📝			
Reports Directory			
Directory		🛟 Change 📷 Open	
User Input			
Device Under Test (DUT)			
User			
Site			
Temperature			
Comments			
Configure default settings for new set	ssion		

3 Performing tests

3.1 Starting a test session

R&S ScopeSuite			×
G Back Complian	ce Tests DisplayPort		About P Help
Select Standard Versio	n		
OP 1	1.4a 🔵 eDP 1.4b 🔵 el	OP 1.5	
Session Name	Last Accessed	Comment	
DP 1.4a_20230917_202827	9/21/2023 9:06:38 AM	Type in your comment.	
DP 1.4a_20230917_202111	9/17/2023 8:21:12 PM	Type in your comment.	
DP 1.4a_20230912_153006	9/12/2023 3:30:08 PM	Type in your comment.	
🕂 Add 😭 Open	💼 Remove 🖳 Rem	ame 📮 Comment 🖹 Show Report	
Add new or open existing se	ession to run.		

After you open a compliance test, the "Session Selection" dialog appears. In this dialog, you can create new sessions, open or view existing report.

The following functions are available for handling test sessions:

Function	Description
"Add"	Adds a new session
"Open"	Opens the selected session
"Remove"	Removes the selected session
"Rename"	Changes the "Session Name"
"Comment"	Adds a comment
"Show report"	Generates a report for the selected session

To add a test session

- 1. In the R&S ScopeSuite window, select the compliance test.
- 2. In the "Session Selection" dialog press "Add".
- 3. If necessary change the "Session Name"

To open a test session

- 1. In the R&S ScopeSuite window, select the compliance test.
- 2. In the "Session Selection" dialog, select the session you want to open and double click on it.

Alternatively, select the session and press "Open".

To show a report for a test session

- 1. In the R&S ScopeSuite window, select the compliance test.
- In the "Session Selection" dialog, select the session you want the report for and press "Show report".

3.2 Configuring the test

- 1. In the R&S ScopeSuite window, select the compliance test to be performed:
 - "DisplayPort"
- 2. Open a test session, see Chapter 3.1, "Starting a test session", on page 15.
- 3. Adjust the "Properties" settings for the test cases you want to perform.
- 4. Click "Limit Manager" and edit the limit criteria, see Chapter 3.2.1.1, "Limit manager", on page 18.
- If you want to use special report settings the "Report Config" tab to define the format and contents of the report. Otherwise the settings defined in "RSScopeSuite" > "Settings" > "Report" are used. See Chapter 2.7, "Report configuration", on page 13.
- Click "Test Checked"/"Test Single" and proceed as described in the relevant test case chapter.

3.2.1 General test settings

R&S ScopeSui	ite								- 🗆 ×
G Back	Session DP 1.4a_20231122_102345					🖹 Sho	w Report	About	😮 Help
•	All	Properties	Limit Manage	er Results	Instruments	Report Config			
	▲ DisplayPort 1.4a			🔿 2 Single-	Ended SMA 🔘	Differential Probe	e (with ZMA	-40)	^
	▲ Main-Link Tests				Skew				
	3.1 Eye Diagram Tests (Normative)	Sir	ngleEnded Pos	√ Ch1 -	0.00 ps	5			
V	 Jitter measurement tests (Normative) 	Sin	gleEnded Neg	~ ~ Ch3 ↓	0.00 ps	3			
	3.9 Non-ISI Jitter measurement tests (Normative)								
	3.11 TJ/RJ/DJ measurement tests (Normative)				Retrieve Skew				
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 	DUT Con	itrol						
	3.4 HBR3/HBR2 Level Verification Test (Normative)	4	AUX Controller	Unigraf UCD	323 🔻				
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)			04004567					
	3.12 Main-Link Frequency Compliance Test (Normative)	Unigrat	Serial Number	01234567					
	 SSC Tests 	1	Num. Of Lanes	0102	04				
	3.7 Intra-pair Skew Test (Informative)		Data Rate	O RBR 1.62	Gbps 🔿 HBR 2	.7Gbps			
	3.8 AC Common Mode Noise Test (Informative)			O HBR2 5.4	1Gbps 💿 HBR3	8.1Gbps			
	3.6 Inter-Pair Skew Test	Pre-e	mphasis Level	0 0 1	0 2 0 3				
	3.10 HBR3 TX Differential RL Test (Informative)	Suina	Veltage Level		0101				
	 AUX_CH Tests 	Swing	voitage Level	001	0203				
	 DP_PWR Tests 		SSC	 Enable 					
		Test Setu	ıp						
			Lane	0 -					
		Ac	quisition Time	2000	kUI				
			Test Point	TP2 🔻	CTLE 🔻				
		Optin	nal CTLE index	0					
			Target BER	10e-6 🔻					- 1
		Export W	/aveforms						
Test Che	ecked Fast Single		Enable						v

Each session dialog is divided into several sections:

 "Properties": shows the settings that can be made for the test case selected on the left side of the dialog. You can differentiate between the "All" and the sub test properties

In the "All" > "Properties" tab you can configure the settings for all test cases in the current session. Once you change and save a setting in this tab, the changes will be done for all test in the sessions. At the same time, there will be a special marking for the functions that have different settings for different sub tests.

- "Limit Manager": sets the measurement limits that are used for compliance testing, see Chapter 3.2.1.1, "Limit manager", on page 18.
- "Results": shows an overview of the available test results for this session.
- "Instruments": defines instruments settings for connecting to external devices, that are specific for this test session.
 When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Instruments") are copied to the session. This "Instruments" tab can be used to change those copied defaults.
- "Report Config": defines the format and contents of the report for this session. When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Report") are copied to the session. This "Report Config" tab can be used to change those copied defaults.
- "Test Checked"/ "Test Single": starts the selected test group.

3.2.1.1 Limit manager

The "Limit Manager" shows the measurement limits that are used for compliance testing.

Each limit comprises the comparison criterion, the unit, the limit value A, and a second limit value B if the criterion requires two limits.

You can set the values to defaults, change the values in the table, export the table in xml format, or import xml files with limit settings.

You can also return the values to the original limits with "Reset to default".

Check and adjust the measurement limits.

Back	Session eDP 1.4b_20230923_221954							🔥 Sho	w Report	About	0
	▲ All	Properties	Limit Manager	Results	Instruments	Report Config					
]	▲ eDisplayPort 1.4b	Measurem	ent				Critoria	Unit	٨	P	
	 Main-Link Tests 	Data SSC [Deviation Max				cinteria XCA T	nom	300	0	
	Eye Diagram Test	Data SSC F	Deviation Min				x>A	nom	-5300		
	▼ Jitter Tests	Data SSC o	if/dt Max				x <a t<="" td=""><td>ppm/us</td><td>1250</td><td></td><td></td>	ppm/us	1250		
	Differential Voltage Test	Data SSC o	if/dt Min				x>A w	ppm/us	-1250		
	Main-Link Frequency Compliance Test	Data SSC M	Aodulation Free	uencv			A<=x<=B ▼	Hz	30000	33000	
	▼ SSC Tests	Data Main	-link Frequency	Min			x>A 🔻	ppm	-300		
	▼ Intra-Pair Tests	Differentia	I Transition Time	e			A<=x<=B ▼	s	5E-11	1.6E-10	
	Inter-Pair Skew Test	InterPair SI	kew				A<=x<=8 ▼	UI	-2	2	
	 AUX CH Tests 	Single End	Single Ended Transition Time A<=x<					s	5E-11	1.6E-10	
	▼ EYE Tests	Rise Fall Ti	Rise Fall Time Mismatch				x<=A *	%	15		
	Sensitivity Test	RBR/HBR A	AC Common Mo	de Noise			x <a td="" 🔻<=""><td>v</td><td>0.02</td><td></td><td></td>	v	0.02		
		HBR2 AC C	Common Mode	Noise			x <a td="" 🔻<=""><td>v</td><td>0.03</td><td></td><td></td>	v	0.03		
		HBR3 AC Common Mode Noise x <a< td=""><td>x<a td="" 🔻<=""><td>v</td><td>0.1</td><td></td><td></td></td></a<>				x <a td="" 🔻<=""><td>v</td><td>0.1</td><td></td><td></td>	v	0.1			
		Data Intra-	Pair Skew				x<=A 🔻	s	3E-11		
		AUX Chan	nel Unit Interval				A<=x<=B ▼	s	4E-07	6E-07	
		AUX Chan	nel Peak-to-Pea	k Voltage			A<=x<=B ▼	v	0.14	1.36	
		AUX Chan	nel Sensitivity Le	evel			x<=A 💌	v	0.28		
		Total Jitter	@BER 10e-9				x<=A *	UI	0.4		
		Differential Peak-to-Peak Output Voltage x<=A 💌					x<=A *	V	1.38		
		A Reset to	Default 📩	Export	a Import						

3.3 Initiating the test

To perform compliance tests, the device under test is connected to the test board in a test-specific way. Using a probe, the test board is connected with the R&S RTP. The probe connections are test-specific. The R&S ScopeSuite guides you step-by-step through the connection setup and the test sequence.

- 1. Set the test setup on a nonconductive, static-approved work surface.
- 2. In the R&S ScopeSuite window, select the compliance test.
- 3. Open a test session, see Chapter 3.1, "Starting a test session", on page 15.
- 4. Check the test configuration settings and adjust, if necessary. See: Chapter 3.2, "Configuring the test", on page 16.

5. Click "Test Checked" for starting all checked test cases or "Test Single" for starting only the selected test case.

The R&S ScopeSuite test wizard explains the following individual setup steps. A test description can be found in the "R&S Test Procedures" manual for the selected compliance test.

The R&S ScopeSuite test wizard explains the following individual setup steps. A detailed test description can be found in the following chapters:

- Chapter 4, "DP 1.4a", on page 27
- Chapter 5, "eDP 1.4b, eDP 1.5 tests", on page 59

3.4 Getting test results

For each test, the test data - report, diagrams and waveform files - is saved in the following folder:

```
<programData%\Rohde-Schwarz\RSScopeSuite\3.0\Sessions\
<Protocolgroup>\<Protocol>\<Session Name>.
```

If you resume an existing session, new measurements are appended to the report, new diagrams and waveform files are added to the session folder. Existing files are not deleted or replaced. Sessions data remain until you delete them in the "Results" tab of the session.

The report format can be defined in "RSScopeSuite" > "Settings" > "Report" for all compliance tests (see also Chapter 2.7, "Report configuration", on page 13). If you want to use special report settings for a session, you can define the format and contents of the report in the "Report Config" tab of the session.

All test results are listed in the "Results" tab. Reports can be provided in PDF, MSWord, or HTML format. To view and print PDF reports, you need a PDF viewer, for example, the Acrobat Reader.

The test report file can be created at the end of the test, or later in the "Session Selection" dialog.

To show a test report

- 1. In the R&S ScopeSuite window, select the compliance test to be performed.
- 2. Select the session name in the "Session Selection" dialog and click "Show report".

The report opens in a separate application window, depending on the file format. You can check the test results and print the report.

To delete the results, diagrams and waveform files of a session

- 1. In the "Session Selection" dialog select the session and open it.
- 2. In the "Results" tab, select the result to be deleted.
- 3. Click "Remove".

3.5 Starting DisplayPort tests

Before you run the test, complete the following actions:

- LAN connection of the oscilloscope and the computer running the R&S Scope-Suite, see Chapter 2.5, "Connecting the R&S RTP", on page 10
- VNA connection for Transmitter and Receiver Return Loss tests, see Chapter 2.6, "Connecting the vector network analyzer", on page 12.
- 1. Select "DisplayPort" in the R&S ScopeSuite start window.
- In the "Session Selection" dialog, set the "Select Standard Version" standard. The following "Types" are available:
 - "DP 1.4a"
 - "eDP 1.4b"
 - "eDP 1.5"
- 3. Add a new test session.
- Open the session. For details, see Chapter 3.1, "Starting a test session", on page 15.
- 5. Check the test configuration settings. Adjust, if necessary. See:
 - Chapter 3.6, "DisplayPort configuration", on page 20
 - Chapter 3.2.1.1, "Limit manager", on page 18
- 6. Select/check the test cases you want to run and click "Test Single"/"Test checked".
- 7. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

3.6 DisplayPort configuration

The test configuration consists of some DisplayPort specific configuration settings that depend on the selected standard version: "DP 1.4 a" or "eDP 1.4b/eDP1.5".

DisplayPort configuration

R&S Scopes	iuite					_	•	_ 🗆 ×
🖨 Back	Session DP 1.4a_20231122_112221					Show Report	About	Help
	All	Properties Limit M	/lanager	Results	Instruments	Report Config		
	▲ DisplayPort 1.4a	Channels						Î
	Main-Link Tests			-				
	3.1 Eye Diagram Tests (Normative)		() 2 Single-	Ended SMA () Differential Probe	(with ZMA-40))
	 Jitter measurement tests (Normative) 				Skew			
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 	SingleEndec	d Pos 🎜	Ch1 ▼	0.00	ps		
	3.4 HBR3/HBR2 Level Verification Test (Normative)	SingleEnded	Neg 7	J [™] Ch3 ▼	0.00	ps		
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)		(4 Single-	Ended SMA 🤇) Differential Probe	(with ZMA-40))
	3.12 Main-Link Frequency Compliance Test (Normative)				Skew			
	▼ SSC Tests	Lane A	α Pos ≯	🔓 Ch1 🔻	0.00	ps		
	3.7 Intra-pair Skew Test (Informative)	Lane A	Neg J	Ch3 🔻	0.00	ps		
	3.8 AC Common Mode Noise Test (Informative)	Lane E	B Pos √	🔓 Ch2 🔻	0.00	ps		
	3.6 Inter-Pair Skew Test	Lane B	Neg J	Ch4 ▼	0.00	ps		
	3.10 HBR3 TX Differential RL Test (Informative)		(2 Single-	Ended Probes	1 Differential P	robe	
	 AUX_CH Tests 				Skew			
	▼ EYE Tests	AUX CH	H Pos 🏷	∫ Ch2 ▼	0.00	ps		
	9.2 AUX_CH (Manchester-II) Sensitivity lest	AUX CH	Neg 7	∬ Ch4 ▼	0.00	ps		
	Iermination DC lests				Retrieve Ske	w		
	DP_PWR lests	DUT Control						
	5.6 infusi (Normative) and Outrush (informative) lest	AUX Control		Inigraf LICD2	22 -			
		Abx conta		mgrai_ocos	25 -			
		Unigraf Serial Nur	mber 0	01234567				
		Num. Of L	anes () 1 () 2 (• 4			
		Data	Rate () RBR 1.62	Gbps 🔿 HBR	2.7Gbps		
			() HBR2 5.4	Gbps 🔿 HBR	3 8.1Gbps		
		Pre-emphasis I	Level (0 () 1 (2 () 3			
		Swing Voltage I	Level (2202			
		sting totage			0200			
			ssc 🗸	Enable				
		Test Par	ittern		Ŧ			
		Test Setup						- 1
			Lane 0	Ŧ				
			Pair L	ane 0 to Lan	e1 🔻			
		Acquisition	Time					
		-						
		Test F	Point T	P2 =	CILE 🔻			
		Optimal CTLE in	index 0)				
		Target	t BER 1	0e-6 🔻				
		Export Waveform	ms					
		En	nable]				
		Offline Execution	n					
Tort C			nable 🗌	1				
i≊≱ rest C		En	able	1				
Ready to run	h							

Figure 3-1: Configuration settings for DP 1.4A

DisplayPort configuration

cas scopesuite	
G Back Session eDP 1.4b_20231120_102505	🖹 Show Report 🕕 About 😢 He
🗸 🔺 All	Properties Limit Manager Results Instruments Report Config
eDisplayPort 1.4b	Channels
Main-Link Tests	
Eye Diagram Test	2 Single-Ended SMA Differential Probe (with ZMA-40)
✓ ✓ Jitter Tests	Skew
Differential Voltage Test	SingleEnded Pos Ch1 v 0.00 ps
Main-Link Frequency Compliance Test	SingleEnded Neg Ch3 v 0.00 ps
✓ SSC Tests	4 Single-Ended SMA O Differential Probe (with ZMA-40)
✓ Intra-Pair Tests	Skew
Inter-Pair Skew Test	Lane A Pos Lane Ch1 = 0.00 ps
AUX CH Tests	Lane A Neg Ch3 v 0.00 ps
✓ V EYE Tests	Lane B Pos Ch2 = 0.00 ps
Sensitivity Test	Lane B Neg Ch4 v 0.00 ps
	● 2 Single-Ended Probes ◯ 1 Differential Probe
	Skew
	AUX CH Pos Ch2 V 0.00 ps
	AUX CH Neg Ch4 V 0.00 ps
	Retrieve Skew
	DUT Control
	AUX Controller Unigraf_UCD323 💌
	Unioraf Serial Number 01234567
	Num. Of Lanes 1 2 4
	Data nate R162 1.02Gbps C R210 2.10Gbps
	○ R243 2.43Gbps ○ R270 2.70Gbps
	○ R324 3.24Gbps ○ R432 4.32Gbps
	○ R540 5.40Gbps ○ R675 6.75Gbps
	R810 8.10Gbps
	Pre-emphasis Level () 0 1 2 3
	Swing Voltage Level $\bigcirc 0 \bigcirc 1 \bigcirc 2 \bigcirc 3$
	SSC 🗹 Enable
	Test Pattern CP2520 Pattern 1 💌
	Test Setup
	Lane 0 💌
	raii Lane U to Lane T *
	Acquisition Time 1000000 Unit Interval
	Export Waveforms
Tast Charled	Enable
	_

Figure 3-2: Configuration settings for eDP 1.4b/ eDP 1.5

Channels

In the "Channels" section you can select the channel of the probes used for the test setup and set the skew for each channel.

The skew compensates signal propagation differences between channels caused by the different length of cables, probes, and other sources.

You can set a fixed value or retrieve the skew value from the oscilloscope.

Num. of lanes

Selects the number of maximum lanes of the DUT for the main-link lanes. Available are 1, 2 or 4 lanes.

Lane

Selects the lane that is to be tested.

Pair

For inter-pair skew tests, specifies which pair of lane is under test.

AUX Controller, Unigraf Serial Number

Selects the model of the auxiliary channel (AUX) controller that is used for the measurements.

For Unigraf UCD323, select "Unigraf_UCD323". Also set the "Unigraf Serial Number" to enable the DP Sink operation.

For any other AUX controller model, select "Manual".

Data Rate

Sets the maximum supported data rate.

Supported data rates for DisplayPort:

- RBR (reduced bit rate): 1.62 Gbits/lane
- HBR (high bit rate): 2.70 Gbits/lane
- HBR2: 5.40 Gbits/lane
- HBR3: 8.10 Gbits/lane

Supported data rates for eDP 1.4b/ eDP 1.5:

- R162: 1.62 Gbits/lane
- R216: 2.16 Gbits/lane
- R270: 2.70 Gbits/lane
- R324: 3.24 Gbits/lane
- R432: 4.32 Gbits/lane
- R540: 5.40 Gbits/lane
- R810: 8.10 Gbits/lane

Test Point

Selects the test point.

Acquisition Time

Selects the length of signal to be analyzed in unit intervals. This setting is available for Eye tests and Jitter Tests.

Test Pattern

Selects the test pattern to be tested. Available are "D10.2", "PRBS7", "CP2520 Pattern1", "CP2520 Pattern 3 (TPS4)".

Optimal CTLE index

Sets an optimal continuous time linear equalizer (CTLE) index.

Number of bits

Sets the number of bits.

SSC

If enabled, only acquisitions that support spread spectrum clocking (SSC) is tested.

Pre-emphasis level

Selects a pre-emphasis level, the pre-emphasizing of the first bit of the continuous signal. Available are the following predefine values for 0 to 3:

- 0: 0dB
- 1: 3dB
- 2: 6dB
- 3: 9dB

Swing voltage level

Selects a swing voltage level, the adjustment of the output signals amplitude.

Available are the following predefined values for 0 to 3:

- 0: 400mV
- 1: 600mV
- 2: 800mV
- 3: 1200mV

Device power type

Selects if the device is a "Power provider" or "Power consumer".

Export Waveforms

Enables you to export a waveform. You can later load the waveforms to run the tests in the offline mode, see "Offline Execution" on page 25.

You can define an export directory, or use the default one:

```
\Rohde-Schwarz\RSScopeSuite\5.35.0\Waveforms\DisplayPort\
[DisplayPort14a or EDisplayPort14b or EDisplayPort15]\
<SessionName>
```

For example:

```
MyDocuments\Rohde-Schwarz\RSScopeSuite\5.35.0\Waveforms\
DisplayPort\DisplayPort14a\DP14a 20230910 144116
```

Offline Execution

Offline Execution

Enable	\checkmark	
DIFF waveform		Select
POS waveform		Select
NEG waveform		Select
DIFF1 waveform		Select
DIFF2 waveform		Select
AUXPOS waveform		Select
AUXNEG waveform		Select
AUXDiff waveform		Select

If enabled, allows you to use exported waveforms as a source for the execution of the compliance test.

You can select one waveform for each needed signal.

DisplayPort configuration

4 DP 1.4a

4.1 Test patterns

The following test patterns are used:

	Link rate	Test pattern
Eye & Jitter tests	RBR, HBR	PRBS7
Eye & Jitter tests	HBR2	CP2520 pattern 1, D10.2
Eye & Jitter tests	HBR3	CP2520 pattern 3
Differential voltage	All link rates	Custom pattern
Main link frequency	All link rates	D10.2
Spread spectrum clocking	All link rates	D10.2
Intra-Pair/Inter-Pair skew	All link rates	PRBS7
AC common mode noise test	RBR, HBR, HBR2	PRBS7
	HBR3	CP2520 pattern 3
HBR3 TX differential RL test	HBR3	PRBS7

4.2 Main-Link tests

4.2.1 Test equipment

The following equipment is needed for performing main link DisplayPort compliance tests.

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum bandwidth 16 GHz	1
Probes	R&S ZM160 with R&S RT-ZMA40	2
	SMA cables	2/4
Advanced jitter analysis	Option R&S RTP-K133 or R&S RTP-K134 Advanced jitter and noise	1
DisplayPort AUX controller	Unigraf's UCD-3233 or equivalent	1
Auxiliary control test adapter	Wilder Technologies auxiliary control test adapter or equivalent	1

Item	Description, model	Quantity	
Embedded DisplayPort test adapter	Wilder Technologies EDP-TPA40L or equivalent	1	
DUT	Any DisplayPort source device	1	

4.2.2 Eye diagram tests (normative)

The purpose of the test is to verify that the timing variables and amplitude trajectories support the overall DP system objectives of BER in data transmission.

4.2.2.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Eye Diagram Tests (Normative)".

R&S ScopeS	R&S ScopeSuite					
G Back	Session DP 1.4a_20231122_102345	R Show Report 1 About 1 Help				
	All	Properties Limit Manager Results Instruments Report Config				
	▲ DisplayPort 1.4a	Channels				
	 Main-Link Tests 					
	3.1 Eye Diagram Tests (Normative)	2 Single-Ended SMA Differential Probe (with ZMA-40)				
	 Jitter measurement tests (Normative) 	Skew				
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 	SingleEnded Pos				
	3.4 HBR3/HBR2 Level Verification Test (Normative)	SingleEnded Neg The Ch3 v 0.00 ps				
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)					
	3.12 Main-Link Frequency Compliance Test (Normative)	Retrieve Skew				
	▼ SSC Tests	DUT Control				
	3.7 Intra-pair Skew Test (Informative)	AUX Controller Unigraf_UCD323 💌				
	3.8 AC Common Mode Noise Test (Informative)	Unigraf Serial Number 01234567				
	3.6 Inter-Pair Skew Test					
	3.10 HBR3 TX Differential RL Test (Informative)					
	✓ AUX_CH Tests	Data Rate O RBR 1.62Gbps O HBR 2.7Gbps				
	 DP_PWR Tests 	HBR2 5.4Gbps HBR3 8.1Gbps				
		Pre-emphasis Level 💿 0 🔵 1 🔵 2 🔵 3				
		Swing Voltage Level				
		SSC 🕑 Enable				
		Test Setup				
		Lane 0 v				
		Acquisition Time 1000 kUI				
		Test Point TP2 T CTLE T				
🖉 Test C	hecked 🕨 Test Single					
Ready to run	h.					

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.2.2 Measurements

Eye source: Differential lane signal with appropriate filter applied.

Link rate	Test point	Filter		
HBR3	TP3_CTLE	HBR3 reference equalizer + Cable Model		
HBR3	TP3_CTLE	HBR3 reference equalizer		
HBR2/HBR	TP2	No filter applied		
HBR2	TP3_EQ	HBR2 reference equalizer + cable model		
HBR	TP3_EQ	HBR2 reference equalizer + cable model		
RBR	TP2/TP3	No filter applied		

Reference signal: Recover the reference clock using a 2nd order PLL with closed-loop tracking bandwidth and damping factor specified in Table 1 PLL 2nd order clock recovery.

Table 4-1: PLL 2nd order clock recovery

Link rate	Closed-loop tracking band- width (MHz)	Damping factor
HBR3	15	1.00
HBR2	10	1.00
HBR	10	1.51
RBR	5.4	1.51

HBR3 reference equalizer

The HBR3 reference equalizer transfer function is given by:

$$H(s) = A_{ac} \times \omega_{p2} \times \left[s + (A_{dc}/A_{ac}) \times \omega_{p1}\right] / (s + \omega_{p1}) \times (s + \omega_{p2})$$

where:

- A_{ac} = 3.5 dB
- A_{dc} = Integer within the range of 0 through 8 dB, inclusive, in steps of 1 dB
- ω_{p1} = 3.03 GHz
- ω_{p2} = 5.60 GHz

HBR2 reference equalizer

The HBR2 reference equalizer transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})(s + \omega_{p3})}$$

The magnitude is given by:

$$H|(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2}\sqrt{\omega^2 + \omega_{p2}^2}\sqrt{\omega^2 + \omega_{p3}^2}}$$

Where:

- $\omega_z = 2\pi (0.64 \times 10^9)$ for upstream device compliance
- $\omega_{p1} = 2\pi (2.7 \text{ x} 10^{9})$
- $\omega_{p2} = 2\pi (4.5 \times 10^{9})$
- $\omega_{p3} = 2\pi (13.5 \times 10^{9})$

HBR reference equalizer

The HBR reference equalizer transfer function is given by:

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

The magnitude is given by:

$$H\left|(j\omega)\right| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2}\sqrt{\omega^2 + \omega_{p2}^2}}$$

Where:

- $\omega_z = 2\pi (0.725 \text{ x} 10^9)$ for upstream device compliance
- ω_{p1} = 2π(1.35 x10 ⁹)
- $\omega_{p2} = 2\pi (2.5 \times 10^{9})$

HBR3/HBR2 mask

The figure below shows a passing mask test for an HBR3 signal.

DP 1.4a

Main-Link tests



Figure 4-1: Pass mask test for an HBR3 signal

HBR/RBR mask

The figure below shows a passing mask test for an RBR signal.



Figure 4-2: Pass mask test for an RBR signal

4.2.3 Jitter measurement tests (normative)

These tests evaluate the Total Jitter and Deterministic Jitter that accompany the data transmission. This measurement is a data time interval error (Data-TIE) jitter measurement.

4.2.3.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Jitter Measurement Tests (Normative)".

R&S ScopeSuite >										
🕒 Back	Session DP 1.4a_20231122_102345						R 5	Show Report	About	ut 🕜 Help
	All	Properties Limit Manag	er Resu	ults	Instrum	ients Re	port Config			
	▲ DisplayPort 1.4a		🔿 2 Si	ingle-E	Ended SM	A 🔿 Diff	erential Pro	be (with ZM	A-40)	
	Main-Link Tests				Skew					
	3.1 Eye Diagram Tests (Normative)	SingleEnded Pos	Ch	1 =	0.00	ps				
V	 Jitter measurement tests (Normative) 	SingleEnded Neg	" Chi	3 -	0.00	ps				
	3.9 Non-ISI Jitter measurement tests (Normative)									
	3.11 TJ/RJ/DJ measurement tests (Normative)				Retrieve	Skew				
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 	DUT Control								
	3.4 HBR3/HBR2 Level Verification Test (Normative)	AUX Controller	Unigraf	UCD3	23 🔻	1				
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)	Universit Carried November	012245]				
	3.12 Main-Link Frequency Compliance Test (Normative)	Unigraf Serial Number	012345	67						
	▼ SSC Tests	Num. Of Lanes	010	2 (9 4					
	3.7 Intra-pair Skew Test (Informative)	Data Rate		R 1.620	Gbps 🔿 I	HBR 2.7GI	ops			
	3.8 AC Common Mode Noise Test (Informative)		— нвя	R2 5.40	Gbps 💿	HBR3 8.10	Sbps			
	3.6 Inter-Pair Skew Test	Pre-emphasis Level	00	710	203					
	3.10 HBR3 TX Differential RL Test (Informative)	Cuine Maltana Laval								
	 AUX_CH Tests 	Swing voltage Level	000	510)2()3					
	▼ DP_PWR Tests	SSC	🖌 Enab	le						
		Test Setup								
		Lane	0	*						
		Acquisition Time	2000	k	UI					
		Test Point	TP2	•	CTLE 🔻					
		Optimal CTLE index	0							
		Target BER	10e-6	•						
		Export Waveforms								
≚≽ lest Cl	neckea 💌 Test Single	Enable								

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.3.2 Measurements

Using dual-direct Model equivalent method to discompose the jitter components from the differential lane signal. The appropriate equalization is applied as explained in Eye test section.

Reference clock

Recover the reference clock using a 2nd order PLL with closed-loop tracking bandwidth and damping factor specified in PLL 2nd order clock recovery.

Total jitter, deterministic jitter, random jitter

The total jitter is the peak-to-peak phase variation in the 0-V differential crossing point, measured at a 10e-9 BER for all link rates. It is estimated with the following equation:

 $TJ=DJ_{dd} + n \times RJ_{dd}$

Where:

 DJ_{dd} is the deterministic jitter.

RJ_{rms} is the random jitter, a standard deviation value of an idealized pure noise process.

N for link rate < 8.1 Gbit/s = 12, to accommodate a 1x10⁻⁹ BER value

N for link rate > = 8.1 Gbit/s = 12, to accommodate a 1×10^{-9} BER value

Non ISI jitter

Non-ISI Jitter can be computed using the following equation:

Jitter_{NON ISI}=TJ - Jitter_{ISI}

The following diagram shows the decomposition of the jitter components:



4.2.4 HBR/RBR level verification and peak to peak differential voltage tests

This test to ensure that for a DP device that supports RBR and HBR, the voltage swing levels are monotonic and the pre-emphasis settings are accurate.

4.2.4.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- Select "Main-Link Tests" > "HBR/RBR Level Verification and Peak to Peak Differential VoltageTests".

R&S Scop	eSuite	×
G Bac	k Session DP 1.4a_20231122_102345	🖹 Show Report 🚺 About 👔 Help
	▲ All	Properties Limit Manager Results Instruments Report Config
	▲ DisplayPort 1.4a	Channels
	▲ Main-Link Tests	
	3.1 Eye Diagram Tests (Normative)	2 Single-Ended SMA Differential Probe (with ZMA-40)
	 Jitter measurement tests (Normative) 	Skew
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 	SingleEnded Pos 🖓 Ch1 🔻 0.00 ps
	3.2 HBR/RBR Non-PE Level Verification Test (Normative)	SingleEnded Neg 🖓 Ch3 🔻 0.00 ps
	3.3 HBR/RBR Level Verification and Peak to Peak Differential Voltage Test (Normative)	
	3.4 HBR3/HBR2 Level Verification Test (Normative)	Retrieve Skew
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)	DUT Control
	3.12 Main-Link Frequency Compliance Test (Normative)	AUX Controller Unigraf_UCD323 🔹
	▼ SSC Tests	Unigraf Serial Number 01234567
	3.7 Intra-pair Skew Test (Informative)	
	3.8 AC Common Mode Noise Test (Informative)	Num. Or Lanes 0 1 0 2 • 4
	3.6 Inter-Pair Skew Test	Data Rate 💿 RBR 1.62Gbps 🔵 HBR 2.7Gbps
	3.10 HBR3 TX Differential RL Test (Informative)	◯ HBR2 5.4Gbps ◯ HBR3 8.1Gbps
	✓ AUX_CH Tests	SSC 📝 Enable
	 DP_PWR Tests 	
		Test Setup
		Lane 0 v
Z Tort	Chasted Test Single	
rest.	checkeu 🕐 lesconigie	
Ready to r	un.	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.4.2 Measurements

The DUT should be configured to output PRBS7 pattern.

HBR/RBR Non-PE level verification tests are performed while pre-emphasis set to 0. HBR/RBR PE level verification and maximum differential peak-to-peak voltage test while varying the pre-emphasis.

4.2.5 HBR3 /HBR2 level verification (normative)

The purpose of this test is to verify that the system budget is adhered to.

4.2.5.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "HBR3 /HBR2 Level Verification (Normative)".

R&S ScopeSuite	——————————————————————————————————————
G Back Session DP 1.4a_20231122_102345	💦 Show Report 🚺 About 👔 Help
All	Properties Limit Manager Results Instruments Report Config
DisplayPort 1.4a	Channels
Main-Link Tests	
3.1 Eye Diagram Tests (Normative)	2 Single-Ended SMA Differential Probe (with ZMA-40)
✓ Jitter measurement tests (Normative)	Skew
HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests	SingleEnded Pos Ch1 = 0.00 ps
✓ 3.4 HBR3/HBR2 Level Verification Test (Normative)	SingleEnded Neg Ch3 🔻 0.00 ps
3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)	
3.12 Main-Link Frequency Compliance Test (Normative)	Retrieve Skew
SSC Tests	DUT Control
3.7 Intra-pair Skew Test (Informative)	AUX Controller Unigraf_UCD323 👻
3.8 AC Common Mode Noise Test (Informative)	Unigraf Serial Number 01234567
3.6 Inter-Pair Skew Test	
3.10 HBR3 TX Differential RL Test (Informative)	
AUX_CH Tests	Data Rate RBR 1.62Gbps HBR 2.7Gbps
	HBR2 5.4Gbps
	SSC 🗹 Enable
	lest Setup
	Lane 0 💌
☑ Test Checked ► Test Single	
Ready to run.	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.5.2 Measurements



4.2.6 HBR3/HBR2 peak to peak differential voltage test (normative)

The purpose of this test is to verify that the peak-to-peak voltage accompanying the data transmission is within the limits defined by the DP1.4A Electrical Requirements Test Specification.

4.2.6.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- Select "Main-Link Tests" > "HBR3 /HBR2 Peak to Peak Differential Voltage Test (Normative)".
| R&S Scop | peSuite | | | | | | | _ 🗆 × |
|----------|--|------------|------------------|------------|--------------|------------------|--------------|--------|
| 🖨 Bac | * Session DP 1.4a_20231122_102345 | | | | Hà. | Show Report | About | 🕜 Help |
| | ▲ All | Properties | Limit Manager | Results | Instrument | s Report Config | | |
| | ▲ DisplayPort 1.4a | Channels | | | | | | |
| | Main-Link Tests | | | | | | | |
| | 3.1 Eye Diagram Tests (Normative) | | C |) 2 Single | -Ended SMA | Differential Pro | be (with ZMA | -40) |
| | Jitter measurement tests (Normative) | | | | Skew | | | |
| | ▼ HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests | Sin | gleEnded Pos | Ch1 🔹 | 0.00 | ps | | |
| | 3.4 HBR3/HBR2 Level Verification Test (Normative) | Sing | gleEnded Neg | Ch3 | 0.00 | ps | | |
| V | 3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative) | | | | | _ | | |
| | 3.12 Main-Link Frequency Compliance Test (Normative) | | | | Retrieve Ske | ew | | |
| | ▼ SSC Tests | DUT Cont | trol | | | | | |
| | 3.7 Intra-pair Skew Test (Informative) | A | UX Controller Ur | nigraf_UCD | 323 💌 | | | |
| | 3.8 AC Common Mode Noise Test (Informative) | Unigraf S | erial Number 0 | 1234567 | | | | |
| | 3.6 Inter-Pair Skew Test | N | lum. Of Lanes | 102 | A | | | |
| | 3.10 HBR3 TX Differential RL Test (Informative) | | | | | | | |
| | AUX_CH Tests | | Data Kate |) RBR 1.6 | 2Gbps () HBR | 2./Gbps | | |
| | DP_PWR Tests | | C |) HBR2 5. | 4Gbps 🔿 HBF | 3 8.1Gbps | | |
| | | | SSC 🗸 | Enable | | | | |
| | | Tost Sotu | n | | | | | |
| | | iest setu | P | | | | | |
| | | | Lane 0 | Ŧ | | | | |
| | | | | | | | | |
| 🔄 Test | t Checked 🕨 Test Single | | | | | | | |
| Ready to | run. | | | | | | | |

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

Measurements

The peak-to-peak voltage for transition and non-transition voltage levels is calculated using the following equations:

$$V_{N_LvIX_PP} = V_{N_LvIX_H} - V_{N_LvIX_L}$$
$$V_{T_LvIX_PP} = V_{T_LvIX_H} - V_{T_LvIX_L}$$

4.2.7 Main-link frequency compliance test (normative)

The purpose of this test is to verify that under any condition the average transfer rate does not exceed the minimum or maximum frequency range as defined by the DP1.4A Electrical Requirements Test Specification.

4.2.7.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Main-link Frequency Compliance Test (Normative)".

Back Session DP 1.4a_20231122_102345 All Exclusion of the sector of the se	Properties Limit Manager Results Instruments Report Config
All	Properties Limit Manager Results Instruments Report Config
Disels Dest 4.4s	
▲ DisplayPort 1.4a	Channels
Main-Link Tests	
3.1 Eye Diagram Tests (Normative)	2 Single-Ended SMA Differential Probe (with ZMA-40)
Jitter measurement tests (Normative)	Skew
HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests	SingleEnded Pos Ch1 = 0.00 ps
3.4 HBR3/HBR2 Level Verification Test (Normative)	SingleEnded Neg
3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)	
3.12 Main-Link Frequency Compliance Test (Normative)	Retrieve Skew
SSC Tests	DUT Control
3.7 Intra-pair Skew Test (Informative)	AUX Controller Unigraf_UCD323 💌
3.8 AC Common Mode Noise Test (Informative)	Unigraf Serial Number 01234567
3.6 Inter-Pair Skew Test	
3.10 HBR3 TX Differential RL Test (Informative)	Num. Of Lanes 0 1 0 2 0 4
	Data Rate 🚫 RBR 1.62Gbps 🚫 HBR 2.7Gbps
DP_PWR Tests	HBR2 5.4Gbps 💿 HBR3 8.1Gbps
	Pre-emphasis Level 💿 0 🗌 1 💭 2 💭 3
	Swing Voltage Level $\bigcirc 0 \cap 1 \cap 2 \cap 3$
	33C V Liable
	Test Setup
	Lane 0 v
	Export Waveforms
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	Offline Execution
Tart Charled	Enable Frable
rest checked Prest single	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.7.2 Measurements

The DUT is set to transmit D10.2 pattern, which consists of alternate 1 bit and 0 bits to simulate clock-liked signal as shown in figure below.



4.2.8 SSC tests

This test evaluates the range of the transmitter signal's SSC down spreading (in ppm). The SSC profile shall not include frequency deviations that exceed 1250ppm/us. SSC modulation frequency and validate that the frequency is within specification limits.

4.2.8.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "SSC Tests".



- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.8.2 Measurements

The DUT is configured to output test pattern D10.2 which consist of alternate 1 bit and 0 bits to simulate clock like signal.

Difference between successive 0v crossing times of the differential lane waveform is measured as UI values.

Instantaneous frequency of the clock signal is measured as the inverse value of the UI values computed. A 0.222us average window filtering is applied to remove the high frequency noise.

The filtered clock frequency is used to analyze modulation rate and deviation as shown in the picture below:

Filtered SSC 🥇 / Max Mod Freq , Min Mod Freq 1 kppm Filtered SSC SSC Deviation Limit Max: 300 ppm SSC Deviation (Max): 113.8 ppm 0 ppm -1 kppm -2 kppm -3 kppm--4 kppm--5 kppm – SSC Deviation Limit Min: -5.3 kppm 2 і 160 µs ا 80 µs і 120 µs 200 µs и 240 µs 280 µs і 320 µs 0 s 40 µs SSC df/dt SSC df/dt SSC df/dt Limit Max: 1.25 kppm/us > 1 kppm/us SSC df/dt (Max): 779.402 ppm/u > 500 ppm/us 0 ppm/us -500 ppm/us C df/dt (N 2 -1 kppm/us SSC df/dt Limit Min: -1.25 kppm/us >-1.5 kppm/usі 100 µs и 200 µs и 350 µs 50 µs 150 µs 250 µs и 300 µs 0 s

Spread spectrum modulation frequency test

The SSC modulation frequency test evaluates the frequency of the SSC modulation and validates that the frequency lies within the specification limits of the DP1.4A Electrical Requirements Test Specification.

Spread-spectrum modulation deviation test

The SSC modulation deviation test evaluates the range of SSC down-spreading of the transmitter signal in parts per million (ppm).

One of the requirements of spread spectrum clocking is that the sink receiver follows the instantaneous frequency of the transmitter signal. This test measures the range of frequency deviation with SSC. The more the frequency deviates from the standard limits, the higher are the risks of interoperability in DP1.4a sources.

dF/dT spread-spectrum deviation high-frequency variation test

The objective of this test is to verify that the SSC profile does not include any frequency deviation that exceeds 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth lowpass filter with a 3dB corner frequency of 1.98MHz.

4.2.9 Intra-pair skew test (informative)

This test evaluates the skew between respective sides of a differential data lane in a DP interface.

4.2.9.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Intra-pair Skew Test (Informative)".



- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.9.2 Measurements

Waveforms of both signal polarities on one lane are simultaneously captured using two single-ended measurement channels. The rising edge of the data true signal (D+) is compared with the complement's (D-) falling edges, and the rising edge of the complement is compared to the falling edge of the data true signal. The time of transition is found by determining when the waveform crosses the transition amplitude.

Each lane is composed of two single-ended signals D+ and D-. For each D+ and D- signal, the average value over the 0.6 to 0.75UI region past the edge of the V_H and V_L is found.

For D+, measure VH+, VL+. For D-, measure VH-, VL-.

$$V_{Transition_D+} = \frac{V_{H+} + V_{L+}}{2}$$
$$V_{Transition_D-} = \frac{V_{H-} + V_{L-}}{2}$$

 $IntraPairSkew = \{1/NumEdges\} \Sigma \{ [(T_{Trans_D+_High} - T_{Trans_D-_Low}) + (T_{Trans_D+_High} - T_{Trans_D-_Low})] / 2 \}$

4.2.10 AC common mode noise test (informative)

The purpose of this test is to report the common mode noise (unfiltered RMS) present in the main link differential pairs. You can use these measurements to predict the EMI/RFI performance of the channels.

4.2.10.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "AC Common Mode Noise Test (Informative)".

R&S ScopeS	iuite					_	•	_ 🗆 ×
G Back	Session DP 1.4a_20231122_102345					C Show Report	About	🕐 Help
	All	Properties	Limit Manager	Results	Instruments	Report Config		
	▲ DisplayPort 1.4a	Channels						
	Main-Link Tests							
	3.1 Eye Diagram Tests (Normative)				Skew			
	 Jitter measurement tests (Normative) 	Sir	gleEnded Pos 🗸	Ch1 ▼	0 ps			
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 	Sin	leEnded Neg	∫ [™] Ch3 ▼	0 ps	5		
	3.4 HBR3/HBR2 Level Verification Test (Normative)					_		
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)				Retrieve Skew			
	3.12 Main-Link Frequency Compliance Test (Normative)	DUT Con	trol					
	▼ SSC Tests	Α	UX Controller Ur	nigraf_UCD32	3 🔻			
	3.7 Intra-pair Skew Test (Informative)	Unigraf	arial Number 0	1234567				
Z	3.8 AC Common Mode Noise Test (Informative)	onigrar.		1234307				
	3.6 Inter-Pair Skew Test	r I	lum. Of Lanes) 1 () 2 🤇	4			
	3.10 HBR3 TX Differential RL Test (Informative)		Data Rate	RBR 1.62G	bps 🔿 HBR 2	7Gbps		
	 AUX_CH Tests 		C) HBR2 5.4G	ibps 💿 HBR3	8.1Gbps		
	▼ EYE Tests	Pre-e	mphasis Level 🤇	0 0 1 0	2 () 3			
	9.2 AUX_CH (Manchester-II) Sensitivity Test	Suina	Voltago Loval					
	▼ Termination DC Tests	Swing	voitage Level		2 0 3			
	 DP_PWR Tests 		SSC 🗸	Enable				
	9.6 Inrush (Normative) and Outrush (Informative) Test	Test Setu	р					
			Lane 0	Ŧ				
		Export W	aveforms					
			Enable					
			chable					
		Offline E	ecution					
🔄 Test Cl	hecked Fast Single		Enable					
Ready to run	h.							

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.10.2 Measurements

The common mode noise is measured for each supported lane. The common mode noise is calculated from the signal's single-ended plus and single-ended minus signals with the following equation:

$$V_{TX-AC-CM} = \frac{V_{TX-PLUS} + V_{TX-MINUS}}{2}$$

The value of the common mode noise RMS is calculated with the following equation:

$$V_{TX-AC-CM_RMS} = \left[\frac{X_1^2 + X_2^2 + X_3^2 + \dots + X_n^2}{n}\right]^{0.5}$$

4.2.11 Inter-pair skew test

This test evaluates the skew (time delay) between respective sides of the differential main link lanes in the DP interface.

4.2.11.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Inter-pair Skew Test".

-				_		-	
•	All	Properties	Limit Manager	Results	Instruments	Report Config	
	▲ DisplayPort 1.4a	Channels					
	 Main-Link Tests 						
	3.1 Eye Diagram Tests (Normative)				Skew		
	 Jitter measurement tests (Normative) 		1st Diff 🎜	L Ch1 ▼	0.00 ps	5	
	 HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests 		2nd Diff 🎜	Ch3 🔻	0.00 ps	5	
	3.4 HBR3/HBR2 Level Verification Test (Normative)				Retrieve Skew		
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)	Main-Lin	< Lanes				
	3.12 Main-Link Frequency Compliance Test (Normative)	N	lum. Of Lanes) 1 () 2 (4		
	▼ SSC Tests						
	3.7 Intra-pair Skew Test (Informative)		Pair La	ne 0 to Lane	1 🔻		
	3.8 AC Common Mode Noise Test (Informative)	Test Setu	p				
V	3.6 Inter-Pair Skew Test						
	3.10 HBR3 TX Differential RL Test (Informative)	A	UX Controller Ut	nigraf_UCD3	23 🔻		
	▼ AUX_CH Tests	Unigraf S	erial Number 0	1234567			
	▲ DP_PWR Tests		Data Rate 🤇) RBR 1.620	Sbps 🔿 HBR 2	.7Gbps	
	9.6 Inrush (Normative) and Outrush (Informative) Test		C) HBR2 5 40	Shos () HBR3	8 1Ghns	
	9.7 DP_PWR DC Level Test (TBD)) 1101a2 0111		0.10000	
		Export W	aveforms				
			Enable				
		Offline Ex	ecution				
			Enable				

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.11.2 Measurements

The software captures waveforms from 2 lanes simultaneously while the DUT is outputting PRBS7 or a DUT dependent custom pattern. The inter-pair skew is regarded as the time difference between the lanes for a common point that is found at the waveform.

 $InterLaneSkew = \{1/NumEdges\} \Sigma |T_{Transition_LaneA} - T_{Transition_LaneB}| - NominalSkew$

4.2.12 HBR3 TX differential RL test (informative)

The purpose of this test is to verify that differential return loss of an HBR3-capable transmitter is within the limits defined by the DP1.4A Electrical Requirements Test Specification.

4.2.12.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "HBR3 TX Differential RL Test (Informative)".

U black	56550H DF 1.44_2025H22_102545			nd superior	(cport	• /	icijo.
A 100 A 1	All	Instruments		Report Co	nfig		
	▲ DisplayPort 1.4a	Properties	Limit Ma	nager	Results		
	 Main-Link Tests 	DUT Control					
	3.1 Eye Diagram Tests (Normative)	AUX C	ontroller	Unigraf_UC	D323	•	
	 Jitter measurement tests (Normative) 	Unigraf Serial	Number	01234567]		
	▼ HBR/RBR Level Verification and Peak to Peak Differential Voltage Tests	Tost Satup					
	3.4 HBR3/HBR2 Level Verification Test (Normative)	lest Setup					
	3.5 HBR3/HBR2 Peak to Peak Differential Voltage Test (Normative)						
	3.12 Main-Link Frequency Compliance Test (Normative)						
	▼ SSC Tests						
	3.7 Intra-pair Skew Test (Informative)						
	3.8 AC Common Mode Noise Test (Informative)						
	3.6 Inter-Pair Skew Test						
V	3.10 HBR3 TX Differential RL Test (Informative)						
	▼ AUX_CH Tests						
	▼ DP_PWR Tests						
🛃 Test Ch	ecked 🕨 Test Single						

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.

5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.2.12.2 Measurements

The test requires a vector network analyzer. For details on how to set up the VNA refer to Connecting the vector network analyzer.

The differential return loss is measured and compared to the pass criteria:

$$SDD22(f) = \begin{cases} -6.5, 0.05 < f_{GHz} \le 3 & (dB) \\ -1.5 + 8.3 \times \log_{10}(\frac{f_{GHz}}{12}), 3 < f_{GHz} \le 12 & (dB) \end{cases}$$

4.3 AUX_CH tests

The group of tests evaluate if the AUX_CH waveforms are within the DisplayPort specification limits.

4.3.1 Test equipment

The following equipment is needed for performing main link DisplayPort compliance tests.

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum bandwidth 16 GHz	1
Probes	R&S ZM160 with R&S RT-ZMA40	2
	SMA cables	2/4
DisplayPort AUX controller	Unigraf's UCD-3233 or equivalent	1
Auxiliary control test adapter	Wilder Technologies auxiliary control test adapter or equivalent	1
Embedded DisplayPort test adapter	Wilder Technologies EDP-TPA40L or equivalent	1
DUT	Any DisplayPort source device	1

4.3.2 Test setup

The following graphics show the test setup for the AUX channel test measurements.



Figure 4-3: AUX channel test setup with 2 single-ended probes



Figure 4-4: AUX channel test setup with 1 differential probe

4.3.3 Eye tests

This test verifies that the timing variables and amplitude trajectories of the AUX_CH waveform support DisplayPort BER system objectives in data transmission.

4.3.3.1 Performing the tests

1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.

R&S ScopeSuite					•	_		
Back Session DP 1.4a_20231122_102345				🖹 Show Rep	port 🚺 About	🕐 Help		
All	Properties	Limit Manager	Results	Instruments	Report Config			
DisplayPort 1.4a	Channels							
Main-Link Tests								
AUX_CH Tests					~			
✓ ► EYE Tests			2 Single-E	nded Probes (1 Differential Prol	be		
9.1 AUX_CH (Manchester-II) EYE Test		20	~	Skew				
9.5 AUX_CH Slew Rate Test		AUX CH Pos	∫ Ch2 ▼	0 p	s			
9.2 AUX_CH (Manchester-II) Sensitivity Test		AUX CH Neg	Ch4 -	0 p	s			
Termination DC Tests				Retrieve Skew	v			
9.3 AUX_CH_N Termination DC Test	DUT Con	trol						
9.4 AUX_CH_P Termination DC Test	A	UX Controller Ut	nigraf_UCD32	23 🔻				
DP_PWR Tests	Unigraf S	erial Number 0	1234567					
	Test Setu	р						
	Export W	aveforms						
		Fnable						
	Ottline Ex	ecution						
Z tardinata N tarfinta		Enable						
lest Checked P lest Single								
Ready to run.								

2. Select "AUX_CH Tests" > "Eye tests".

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.3.3.2 Measurements

The software collects the waveform containing AUX CH data transaction. A simple decoding is applied to separate the signal. Only signal transmitted from source DUT is used to construct the eye diagram.

The following figure shows an eye diagram that passed the mask test:

DP 1.4a AUX CH tests



4.3.6.2 AUX_CH slew rate test

This test evaluates the AUX_CH waveform, to ensure that the slew rate of the transition edges stays within the DisplayPort specification.

The software collects the waveform containing AUX CH data transaction. A simple decoding is applied to separate the signal. Only rising and falling edges of signal transmitted from source DUT are used to measure the slew rate. Slew rates are calculated by measuring time needed of rising edges to transit from 20% to 80% of final peak-peak voltage and time needed for falling edges to transit from 80% to 20% of the final Peak-Peak voltage.

Collective of rising and falling edges are shown in the figures below respectively.



9 48 mV/ns 52 mV/ns 56 mV/ns 60 mV/ns 64 mV/ns 68 mV/ns 72 mV/ns

4.3.4 AUX_CH (Manchester-II) sensitivity test

This test evaluates minimum voltage swing the receiver part of the source DUT is able to response to.

4.3.4.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "AUX_CH Tests" > "AUX_CH (Manchester-II) Sensitivity Test".

R&S ScopeSi	uite						•	_ 🗆 ×
🖨 Back	Session DP 1.4a_20231122_102345				🖹 Sho	w Repo	ort 1 About	Help
•	All	Properties	Limit Manag	er Results	Instrum	ents	Report Config	
	▲ DisplayPort 1.4a	Channels						
	▼ Main-Link Tests							
	 AUX_CH Tests 						<u>_</u>	
	▼ EYE Tests			2 Sing	le-Ended Prob	ies () 1 Differential Pro	obe
	9.2 AUX_CH (Manchester-II) Sensitivity Test			n. m	Skew	_		
	 Termination DC Tests 		AUX CH Pos	Ch2	• 0.00	ps		
	 DP_PWR Tests 		AUX CH Neg	Ch4	▼ 0.00	ps		
					Retrieve	Skew		
		DUT Con	trol					
		A	UX Controller	Unigraf_UC	D323 🔻			
		Unigraf S	erial Number	01234567				
		TICI			_			
		lest Setu	р					
🖳 Test Ch	necked 🕨 Test Single							
Ready to run								

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.3.4.2 Measurements

This test requires a DP AUX controller that is able to change the voltage swing of the AUX CH.

The software iterates through various voltage swing values while commanding the AUX controller to induce a normal AUX transaction. For each swing value iterate, the software inspects if the transaction is indeed acknowledged by the DUT. The smallest

swing value of the AUX CH for which the source DUT is still able to respond is the minimum sensitivity level of the DUT.

The figure below shows the minimum voltage swing the source DUT is able to response to.



4.3.5 Termination DC tests

The termination DC test measures the form of AUX_CH_N and AUX_CH_P. The purpose of this test is to verify that the DC voltage from

4.3.5.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "AUX_CH Tests" > "Termination DC Tests".



- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.3.5.2 Measurements

AUX_CH_N termination DC test

The DC voltage from AUX_CH_N to GND on the link's source side is measured when a 1-M Ω resistance is connected from AUX_CH_N to GND.

								ingger		nonzontat		equipition		2025-00-	04 /
							<mark>□</mark> ▲	Edge O	V Auto Trg'd	2.5 ns/ 0 s	20 GSa/s 1 kpts	s Sample	Π	14:03:4	5 💖
5.6 V [OUT Power O	N: C2,C4	×											1	
		Probe	Aeter 2 🔹	- ×											
- 4.4 V	Ţ			93 mV											
		Probe	Aeter 4 🛛 🗕	- ×											
- 3.8 V	Ŧ			2.735 V			_								
- 3.2 V	•														
÷ 2.6 V		(1 AUX CH	I N Terminatio	n DC Voltag	ge******		~~~			~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	~~~~		\		-4
-							-								
- 2 V															
- 1.4 V															
- 800 mV															
-							_								
Cu4.X2		44- A LANK 278	n minim via su	Downlaw		A A.4.A									
-400 m V	-10014.1	(1 ADX CF	-7.5 ns	-5 ns	-2.5 r	ns O	s	2.5	5 ns	5 ns	رف این است.	7.5 ns	1	0 ns	12.5 ns
Cu 1 2	X1		X2		ΛΧ	1/0X	-	¥1		Y2		ΔΥ		٨٢/٨)	(
2 📿 🛇		-12.5 ns	-1	2.5 ns	0 s	i juk			0.093		-0.4		193 mV		
4 🕻 🐼		-12.5 ns	-1	2.5 ns	0 s				2.743		-0.4	4	3.143 V		
Ω.	_	C4													
600 mV/	/	600 mV	1/												
2.6 V DC-50 O	3 GHz RT-7530	2.6 V DC-50 O	3 GHz RT-7530												

Figure 4-5: AUX_CH_N termination DC test with power on



Figure 4-6: AUX_CH_N termination DC test with power off

AUX_CH_P termination DC test

The DC voltage from AUX_CH_P to GND on the link's source side is measured when a 1-M Ω resistance is connected from AUX_CH_P to a 3.3-VDC termination voltage.

4.4 DP_PWR tests

4.4.1 Test equipment

The following equipment is needed for performing main link DisplayPort compliance tests.

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum bandwidth 16 GHz	1
Active probe	Minimum bandwidth: 500MHz	2
	2/4	
Inrush/Outrush test fixture	V-Prime DP Inrush/Outrushtest fixture or equivalent	
DUT	Any DisplayPort source device	1

4.4.2 Inrush (normative) and outrush (informative) test

The purpose of this test is to verify that the inrush energy at the power supply input of a power-consuming DUT and the inrush tolerance at the power supply output of a power-providing DUT system-dependent operation is maintained during a hot Plug event.

4.4.2.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "AUX_CH Tests" > "Inrush (Normative) and Outrush (Informative) Test".

R&S ScopeSuite	×
G Back Session DP 1.4a_20231122_102345	🗞 Show Report 🚺 About 👔 Help
 All DisplayPort 1.4a Main-Link Tests AUX_CH Tests EVE Tests 9.2 AUX_CH (Manchester-II) Sensitivity Test Termination DC Tests DP_PWR Tests 9.6 Inrush (Normative) and Outrush (Informative) Test 	Properties Limit Manager Results Instruments Report Config Channels Vd Vd
Test Checked Test Single	
Ready to run.	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

4.4.2.2 Measurements

If a power-consuming device has excessive inrush, this may cause a power-providing device to fail. A power-consuming device shall not exceed this inrush energy. A power-providing device shall be able to handle this amount of inrush energy.

		Trigger	Horizontal Ac	quisition Info	2023-08-04
	<mark>0</mark>	Edge 100 mV Norm	200 µs/ 5 GSa/s	Sample RT	16:12:01
315 mV	<u>ک</u>		000 µ3 10 mpts		
Diagram1: C1,C2 × nrush Current — — —					
140 mV					
сси п.X.2 цадоб m W qCu1.Y2 20 р да 40 р да	600 με	1 ms	1.2 ms	1.4 ms	6 m's 1:8 ms
315 mV Current Zoom: C1 C2 X					
280 mV					
245 mV					
710 mV					
			anna sa ann an a		
- 175 mV +					
					-
	Winterie .				
- 105 mV					TA
					-
					-
35 mV				lan Wakan na kana kana sa	A MINA MINA AND A MINA MINA
←Cu1.X2			a series and a series of the s	and make about the state	
-35 mV 4 s Cu1.Y2-1 μs 4.2 μs	6.3 µs 8.4 µs	10.5 µs 12.6 µ	14.7 μs	16.8 µs	18.9 µs 20 µs
Meas Group 1 🛄 Meas Group 2 💆					_
Max 261.74 mV Amplitude	3.2609 V				•
Cu 1 2 X1 X2	ΔΧ 1/ΔΧ	Y1	Y2	ΔΥ	ΔΥ/ΔΧ
1 C1 😵 -200 μs -200 μs	0 s	0.262	-0.035	-296.74 mV	-
C1 C2 C2					
35 m\// 500 m\//					
5 GHZ 5 GHZ					

5 eDP 1.4b, eDP 1.5 tests

5.1 Main-Link tests

The purpose of the Main-Link tests is to verify that the eDP source device under test is outputting signal that complies with the eDP 1.4b or eDP 1.5 Standard.

5.1.1 Test equipment

The following equipment is needed for performing main link eDP 1.4b, eDP 1.5 compliance tests.

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum bandwidth 16 GHz	1
Probes	R&S ZM160 with R&S RT-ZMA40	2
	SMA cables	2/4
Advanced jitter analysis	Option R&S RTP-K133 or R&S RTP-K134 Advanced jitter and noise	1
DisplayPort AUX controller	Unigraf's UCD-3233 or equivalent	1
Auxiliary Control test adapter	Wilder Technologies Auxiliary control test adapter or equivalent	1
Embedded DisplayPort test adapter	Wilder Technologies EDP-TPA40L or equivalent	
DUT	Any eDP source device	1

5.1.2 Test patterns

The following test patterns are used:

	Link rate	Test pattern	
Eye & Jitter tests	2.7 Gbps	PRBS7	
Eye & Jitter tests	> 2.7 Gbit/s and ≤ 5.4 Gbps	CP2520 pattern 1	
Eye & Jitter tests	> 5.4 Gbit/s and ≤ 8.1 Gbps	CP2520 pattern 3	
Differential voltage	All link rates	Custom pattern	
Main link frequency	All link rates	D10.2	
Spread spectrum clocking	All link rates	D10.2	
Intra-Pair/Inter-Pair skew	All link rates	PRBS7	

5.1.3 Eye diagram tests

The purpose of the test is to ensure that timing variables and amplitude trajectories support the overall DP system objectives of BER in data transmission.

5.1.3.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Eye Diagram Tests".

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Back Session eDP 1.5_20230918_134943	🖹 Show Report 🚺 About 👔 Help
All	Properties Limit Manager Results Instruments Report Config
 eDisplayPort 1.5 	Channels
Main-Link Tests	
✓ Eye Disgram Test	2 Single-Ended SMA Differential Probe (ZMA-40)
itter Tests	Skew
Differential Voltage Test	SingleEnded Pos
Main-Link Frequency Compliance Test	SingleEnded Neg 🖵 Ch3 💌 0.00 ps
SSC Tests	Retrieve Skew
	Main-Link Lanes
Inter-Pair Skew Test	Num: Of Lanes 🔵 1 🔵 2 🖲 4
AUX_CH Tests	Lane 0 v
EYE Tasts	
Sensitivity Test	Test Setup
	AUX Controller Ungerd UG0023 * Ungerd Send Numer 013487 Dels Rei R124 142000 R1 Rei R216 21600 R216 21600 R124 14200 R126 2160 R124 14200 R126 14200
✓ Test Checked ► Test Single	Swina Voltage Level

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.3.2 Measurements

For Link rate < 5.4Gbps (eDP 1.4b & eDP 1.5):

Construct an eye diagram for the lane under test using the following condition:

Eye source: Differential lane signal with link rate-appropriate TP3_EQ Reference Equalizer applied.

Reference signal: Recover the reference clock using a 2nd order PLL with closedloop tracking bandwidth and damping factor as specified in PLL 2nd order clock recovery.

Table 5-1: PLL 2nd order clock recovery

Link rate	Closed-loop tracking band- width (MHz)	Damping factor		
> = 5.4Gbps	15	1.0		
> 2.7 Gbps and < 5.4 Gbps	10	1.0		
> 1.62 Gbps and < = 2.7 Gbps	10	1.51		
< =1.62Gbps	5.4	1.51		

The figure below shows a pass case for eye test:



Figure 5-1: Eye test with pass criteria

For Link Rate > 5.4Gbps (eDP 1.5):

Construct an eye diagram for the lane under test using the following condition:

Eye Source: Differential lane signal with link rate-appropriate HBR3 CTLE Reference applied.

Reference Signal: Recover the reference clock using a 2nd Order PLL with closedloop tracking bandwidth and damping factor specified in PLL 2nd order clock recovery.

The figure below shows a pass case for eye test:



Figure 5-2: Eye test with pass criteria for eDP 1.5

5.1.4 Jitter tests

These tests evaluate the Total Jitter and Deterministic Jitter that accompany the data transmission. This measurement is a data time interval error (Data-TIE) jitter measurement.

5.1.4.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Jitter Tests".

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 eDisplayPort 1.5 	Channels			í.
Main-Link Tests				
Eye Diagram Test	2 Single-Ended SMA () Differential Probe (ZMA-40)			
🗹 🔺 Jitter Tests	Skew			
Non ISI litter	SingleEnded Pos			
Total Jitter	SingleEnded Neg 🔓 Ch3 💌 0 ps			
Random Jitter	Retrieve Skew			
Deterministic Jätter	Main-Link Lanes			
Differential Voltage Test	Num. Of Lanes 🔿 1 🔿 2 💌 4			
Main-Link Frequency Compliance Test	Lane 0 v			
▼ SSC Tests				
▼ Intra-Pair Tests	Test Setup			
Inter-Pair Skew Test	AUX Controller Univer UCD323			
AUX_CH Tests				
▼ EYE Tests	Unigraf Serial Number 01234567			
Sensitivity Test	Data Rate 💿 R162 1.62Gbps 🔘 R216 2.16Gbps			
	R243 2.43Gbps R270 2.70Gbps			
	R324 3.24Gbps R432 4.32Gbps			
	P540 5 40Ghm P675 6 75Ghm			
	Acquisition Time 1000000 Unit Interval			
	TP3 Reference EQ_CTLE Optimal ~			
	Test Pattern CP2520 Pattern 1 👻			- 1
	SSC 🗸 Enable			
C Test Checked F Test Single	Swing Voltage Level			

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.4.2 Measurements

The following measurements are performed:

- "Non ISI Jitter"
- "Total Jitter"
- "Random Jitter"
- "Deterministic Jitter"

Using Dual-Direct Model equivalent method to discompose the jitter components from the differential lane signal. The appropriate equalization is applied.

Total Jitter, Deterministic Jitter, Random Jitter

The total jitter is the peak-to-peak phase variation in the 0-V differential crossing point, measured at a 10e-9 BER for all link rates. It is estimated with the following equation:

 $TJ=DJ_{dd} + n \times RJ_{dd}$

Where:

 DJ_{dd} is the deterministic jitter

RJ_{rms} is the random jitter, a standard deviation value of an idealized pure noise process.

N for link rate < 8.1 Gbit/s = 12, to accommodate a 1x10⁻⁹ BER value

N for link rate > = 8.1 Gbit/s = 12, to accommodate a $1x10^{-9}$ BER value

Non ISI Jitter

Non ISI Jitter can be computed using the following equation:

Jitter_{NON_SIS}=TJ - Jitter_{ISI}

The following diagram shows the decomposition of the jitter components:



5.1.5 Differential voltage test

This test measures differential voltages on transition and non-transition levels when the DUT is operating at the different voltage and pre-emphasis settings.

5.1.5.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Differential Voltage Test".

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All	Properties Limit Manager Results Instruments Report Config
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Main-Link Tests	
Eye Diagram Test	2 Single-Ended SMA O Differential Probe (ZMA-40)
✓ Jitter Tests	Skew
✓ Differential Voltage Test	SingleEnded Pos
Main-Link Frequency Compliance Test	SingleEnded Neg Ch3 🔻 0 ps
SSC Tests	Retrieve Skew
☐ Intra-Pair Tests	Main-Link Lanes
Inter-Pair Skew Test	Num. Of Lanes 1 2 • 4
AUX_CH Tests	Lane 0 💌
Sensitivity Test	Test Setup
	AUX Controller Unigraf_UCD323 👻
	Unigraf Serial Number 01234567
	Data Rate 💿 R162 1.62Gbps 🔘 R216 2.16Gbps
	○ R243 2.43Gbps ○ R270 2.70Gbps
	○ R540 5.40Gbps ○ R675 6.75Gbps
	R810 8.10Gbps
	SSC 🗹 Enable
Test Checked Test Single	
Ready to run.	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.5.2 Measurements

The DUT is configured to transmit a custom pattern which consists of 111110000 bit pattern.

Transition voltages ($V_{T_LvIX_H}$, $V_{T_LvIX_L}$) are the average value measured at 0.4 to 0.7 UI of the 5 consecutive bits while non-transition voltage ($V_{N_LvIX_H}$. $V_{N_LvIX_L}$) are the average values measure from 2.5 to 4.5 UI of the consecutive bits.



5.1.6 Main-link frequency compliance test

This test ensures that the average data rate under all conditions does not exceed the minimum or maximum link rate set by the specification.

5.1.6.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Main-link Frequency Compliance Test".

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G Back Session eDP 1.5_20230918_134943	🖹 Show Report 🚺 About 👔 Help
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Main-Link Tests	
Eye Diagram Test	2 Single-Ended SMA O Differential Probe (ZMA-40)
▼ Jitter Tests	Skew
Differential Voltage Test	SingleEnded Pos
Main-Link Frequency Compliance Test	SingleEnded Neg Ch3 💌 0 ps
SSC Tests	Retrieve Skew
Intra-Pair Tests	Main-Link Lanes
Inter-Pair Skew Test	Num. Of Lanes 🔵 1 🔵 2 💿 4
AUX_CH Tests	Lane 0 v
EYE Tests	
Sensitivity Test	Test Setup
	ALIX Controller Heigerf HCD222
	Unigraf Serial Number 01234567
	Data Rate 💿 R162 1.62Gbps 🗌 R216 2.16Gbps
	R243 2.43Gbps R270 2.70Gbps
	○ R324 3.24Gbps ○ R432 4.32Gbps
	R540 5.40Gbps R675 6.75Gbps
	R810 8.10Gbps
	SSC 📝 Enable
	Pre-emphasis Level 🔍 U 🔾 1 🔾 2 🔾 3
Test Checked Fast Single	Swing Voltage Level 💿 0 🔾 1 🔾 2 🔾 3
Ready to run.	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.6.2 Measurements

The DUT is set to transmit D10.2 pattern, 2 which consist of alternate 1 bit and 0 bits to simulate clock-liked signal as shown in figure below:

eDP 1.4b, eDP 1.5 tests

Main-Link tests



The software measures and reports frequency of the clock-liked signal.



Figure 5-3: Main-link frequency with SSC enabled



Figure 5-4: Main-link frequency with SSC disabled

5.1.7 SSC tests

This test evaluates the range of the transmitter signal's SSC down spreading (in ppm). The SSC profile shall not include frequency deviations that exceed 1250 ppm/us.

5.1.7.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "SSC Tests".

kas scope:	Suite	@
G Back	Session eDP 1.4b_20230923_221954	K Show Report 1 About
	▲ All	Properties Limit Manager Results Instruments Report Config
	 eDisplayPort 1.4b 	Channels
	 Main-Link Tests 	
	Eye Diagram Test	② 2 Single-Ended SMA () Differential Probe (ZMA-40)
	✓ Jitter Tests	Skew
	Differential Voltage Test	SingleEnded Pos
	Main-Link Frequency Compliance Test	SingleEnded Neg ☐ Ch3 ▼ 0.00 ps
	▲ SSC Tests	Retrieve Skew
	Modulation Frequency	Main-Link Lanes
	Modulation Deviation	Num. Of Lanes 0 1 0 2 0 4
	dF/dT Spread-spectrum Deviation High-frequency Variation	Lane 0 v
	▼ Intra-Pair Tests	
	Inter-Pair Skew Test	Test Setup
	✓ AUX CH Tests	AllY Controller Heines (HCD222 w
		Unigraf Serial Number 01234567
		Data Rate 💿 R162 1.62Gbps 🗌 R216 2.16Gbps
		○ R243 2.43Gbps ○ R270 2.70Gbps
		O R324 3.24Gbps O R432 4.32Gbps
		○ R540 5.40Gbps ○ R675 6.75Gbps
		O Kello al loubps
		SSC 🗹 Enable
		Pre-emphasis Level 💿 0 🔵 1 💭 2 🔵 3
		Swing Voltage Level
		Export Waveforms
		English
	Thankad 🐚 Tart Single	
iest c	ancena processinge	Offline Execution

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.7.2 Measurement

The DUT is configured to output test pattern D10.2 which consist of alternate 1 bit and 0 bits to simulate clock like signal.

The difference between the successive 0v crossing times of the differential lane waveform are measured as UI values.

Instantaneous frequency of the clock signal is measured as the inverse value of the UI values computed. A 0.222us average window filtering is applied to remove the high frequency noise.

The filtered clock frequency is used to analyze the modulation rate and deviation as shown in the picture below:



5.1.8 Intra-pair skew test

This test evaluates the skew between respective sides of a differential data lane in a Dipslay Port interface.

5.1.8.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Intra-pair Skew Test (Informative)".

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■ eDisplayPort 1.5	Channels						Î
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Eye Diagram Test				Skew			
✓ Jitter Tests	Sin	gleEnded Pos 🎜	℃h1 🔻	0.00 ps	5		
Differential Voltage Test	Sing	JleEnded Neg 거	∫ [™] Ch3 ▼	0.00 ps	5		
Main-Link Frequency Compliance Test				Retrieve Skew	,		
SSC Tests	Main-Lin	k Lanes			_		
Intra-Pair Tests	N	lum. Of Lanes) 1 () 2 🤇	4			
Inter-Pair Skew Test		lane 0					
AUX_CH Tests		Lunc 0	-				
EYE Tests	Test Setu	р					
Sensitivity Test							
	A	UX Controller U	nigraf_UCD32	23 🔻			
	Unigraf S	erial Number 0	1234567				
		Data Rate 🤇	R162 1.62	Gbps 🔿 R216	2.16Gbps		
			R243 2.43	Gbps 🔿 R270	2.70Gbps		
			R324 3 24	Ghns C R432	432Gbps		
		C) R540 5.40	Gbps () R675	6.75Gbps		
		C	R810 8.10	Gbps			
		SSC 🗸	Enable				
	Export W	aveforms					
		Enable					
	0.000						
	Ottline Ex	ecution					
Test Checked Test Single		Enable					Y
Ready to run.							

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.8.2 Measurements

Waveforms of both signal polarities on one lane are simultaneously captured using two single-ended measurement channels. The rising edge of the data true signal (D+) is
compared with the complement's (D-) falling edges, and the rising edge of the complement is compared to the falling edge of the data true signal. The time of transition is found by determining when the waveform crosses the transition amplitude.

Each lane is composed of two single-ended signals D+ and D-. For each D+ and D- signal, the average value over the 0.6 to 0.75UI region past the edge of the V_H and V_L is found:

$$V_{Transition_D+} = \frac{V_{H+} + V_{L+}}{2}$$
$$V_{Transition_D-} = \frac{V_{H-} + V_{L-}}{2}$$

 $IntraPairSkew = \{1/NumEdges\} \Sigma \{ [(T_{Trans_D+_High} - T_{Trans_D-_Low}) + (T_{Trans_D+_High} - T_{Trans_D-_Low})] / 2 \}$

5.1.9 Inter-pair skew test

This test evaluates the skew (time delay) between respective sides of the differential main link lanes in the DisplayPort interface.

5.1.9.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "Main-Link Tests" > "Inter-pair Skew Test".

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eDisplayPort 1.5	Channels						
Main-Link Tests							
Eye Diagram Test				Skew			
▼ Jitter Tests		1st Diff 🎝	Ch1 🔻	0.00 ps	5		
Differential Voltage Test		2nd Diff 🎜	Ch3 🔻	0.00 ps	5		
Main-Link Frequency Compliance Test				Retrieve Skew			
SSC Tests	Main-Lin	Lanes					
▼ Intra-Pair Tests	N	um. Of Lanes () 1 () 2 🤇	4			
Inter-Pair Skew Test		a : [.					
AUX_CH Tests		Pair	ane 0 to Lane	1 🔻			
EYE Tests	Test Setu	с					
Sensitivity Test							
	A	UX Controller	Inigraf_UCD32	23 🔻			
	Unigraf S	erial Number	1234567				
		Data Rate	R162 1.620	Gbps 🔿 R216	2.16Gbps		
) R243 2.430	Gbps 🔿 R270	2.70Gbps		
			R324 3.24	Gbps 🔿 R432	4.32Gbps		
		(R540 5 400	Shos O R675	6 75Gbps		
					0.756665		
		() R810 8.100	Gbps			
	Export W	aveforms					
		Enable]				
	Offline Ev	ecution					
	S MILLE	Enable	1				
Test Checked Test Single		Liable	1				
Ready to run.							

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.1.9.2 Measurements

The measurement only applies to DUT with either 2 or 4 lanes.

The software captures waveforms from 2 lanes simultaneously while the DUT is outputting PRBS7. The inter-pair skew is regarded as the time difference between the lanes for a common point that is found at the waveform. At least 100 measurements are needed to pass the test.

 $InterLaneSkew = \{1/NumEdges\} \Sigma |T_{Transition_LaneA} - T_{Transition_LaneB}| - NominalSkew$

5.2 AUX_CH tests

The group of tests evaluate if the AUX_CH waveforms are within the DisplayPort specification limits.

5.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum bandwidth 16 GHz	1
Probes	R&S ZM160 with R&S RT-ZMA40	1
	Active Probe with minimum bandwidth of 500 MHz and minimum Input impendence: 100kohm	2
Embedded DP test adapter	Wilder Technologies's EDP-TPA40L or equivalent	1
DP auxiliary control test adapter	Wilder Technologies' DPI-TPA-A or equivalent	1
DP AUX control	Unigraf's UCD-3233 or equivalent	1
DUT	Any eDP source device	1

5.2.2 Test setup

The following graphic show the test setup for the AUX channel test measurements.



Figure 5-5: AUX channel test setup with 2 single-ended probes



Figure 5-6: AUX channel test setup with 1 differential probe

5.2.3 Eye tests

This test verifies that the timing variables and amplitude trajectories of the AUX_CH waveform support DisplayPort BER system objectives in data transmission.

5.2.3.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "AUX_CH Tests" > "Eye tests".

AUX_CH tests

R&S ScopeSuite	• _ ¤ ×				
G Back Session eDP 1.5_20230918_134943	Real Show Report 1 About 1 Help				
 All 	Properties Limit Manager Results Instruments Report Config				
eDisplayPort 1.5	Channels				
Main-Link Tests					
Eye Diagram Test	2 Single-Ended Probes 1 Differential Probe				
Jitter Tests	Skew				
Differential Voltage Test	AUX CH Pos Ch2 V 0.00 ps				
Main-Link Frequency Compliance Test	AUX CH Neg				
SSC Tests	Dation Chan				
▼ Intra-Pair Tests	Retrieve Skew				
Inter-Pair Skew Test	Test Setup				
AUX_CH Tests					
✓ ▲ EYE Tests	AUX Controller Unigrat_UCD323				
Mask Test	Unigraf Serial Number 01234567				
Peak to Peak Voltage	Export Waveforms				
Unit Interval	Enable				
Sensitivity Test					
	Offline Execution				
	Enable				
Test Checked Test Single					
Ready to run.					

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 5. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.2.3.2 Mask test

This test verifies that the timing variables and amplitude trajectories of the AUX_CH waveform support DisplayPort BER system objectives in data transmission.

The software collects the waveform containing AUX CH data transaction. A simple decoding is applied to separate the signal. Only signal transmitted from source DUT are used to construct the eye diagram.

eDP 1.4b, eDP 1.5 tests

AUX_CH tests



5.2.3.3 Peak to peak voltage

This test verifies that the peak-to-peak voltage of the AUX_CH waveform, stays within the limits defined by the DisplayPort specification.

The software collects the waveform containing AUX CH data transaction. A simple decoding is applied to separate the signal. Only the signal transmitted from the source DUT is used to construct the eye diagram. Only waveform data within 40% to 60% of the unit interval of each bit used. The peak-to-peak voltage is defined as the difference between the average of upper half to of the waveform data and the lower half.

The following figure shows the upper voltage, lower voltage and the difference between the 2 voltages.

eDP 1.4b, eDP 1.5 tests

AUX CH tests



5.2.3.4 Unit interval

This test verifies that the overall variation of the Manchester transaction Unit Interval for the AUX CH waveform stays within the DisplayPort specification limits.

The software collects the waveform containing AUX CH data transaction. A simple decoding is applied to separate the signal. Only signals transmitted from the source DUT are used. Unit interval of the signal is measured by collecting all edges and estimate a uniform clock pulse that best fits the separated signal.

5.2.4 Sensitivity test

This test evaluates the minimum voltage swing that the receiver part of the source DUT is able to respond to.

5.2.4.1 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DisplayPort tests", on page 20.
- 2. Select "AUX_CH Tests" > "Sensitivity test".

AUX_CH tests

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G Back Session eDP 1.5_20230918_134943	R Show Report 1 About 1 Help
All	Properties Limit Manager Results Instruments Report Config
eDisplayPort 1.5	Channels
Main-Link Tests	
Eye Diagram Test	2 Single-Ended Probes 1 Differential Probe
	Skew
Differential Voltage Test	AUX CH Pos
Main-Link Frequency Compliance Test	AUX CH Neg
SSC Tests	
☐ Intra-Pair Tests	Retrieve skew
Inter-Pair Skew Test	Test Setup
AUX_CH Tests	
EYE Tests	AUX Controller Unigraf_UCD323 v
Mask Test	Unigraf Serial Number 01234567
Peak to Peak Voltage	Export Waveforms
Unit Interval	Enable
Sensitivity Test	
	Offline Execution
	Enable
Test Checked Fast Single	
Ready to run.	

- 3. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 25.

5.2.4.2 Measurements

This test requires a DP AUX controller that is able to change the voltage swing of the AUX CH.

The software iterates through various voltage swing values while commanding the AUX controller to induce a normal AUX transaction. For each swing value, the software inspects if the transaction is acknowledged by the DUT. The smallest swing value of the AUX CH for which the source DUT is still able to respond, is the minimum sensitivity level of the DUT.

The figure below shows the minimum voltage swing the source DUT is able to respond to.

eDP 1.4b, eDP 1.5 tests AUX_CH tests

