R&S[®]RTP-K93 DDR4 Compliance Test User Manual



1178991002 Version 08



Make ideas real



This document describes the DDR4 Compliance Test Procedures of the following option:

• R&S[®]RTP-K93 (1801.3671.02)

Other functionality of the option is described in the instrument's user manual.

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Throughout this manual, products from Rohde & Schwarz are indicated without the ® symbol , e.g. R&S[®]ScopeSuite is indicated as R&S ScopeSuite.

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1 R&S ScopeSuite overview

The R&S ScopeSuite software is used with R&S RTP oscilloscopes. It can be installed on a test computer or directly on the oscilloscope. For system requirements, refer to the Release Notes.



The R&S ScopeSuite main panel has several areas:

- "Settings": connection settings to oscilloscope and other instruments also default report settings
- "Compliance Tests": selection of the compliance test
- "Demo": accesses demo test cases that can be used for trying out the software without having a connection to an oscilloscope
- shift sideways to change the transparency of the dialog box
- "Help": opens the help file, containing information about the R&S ScopeSuite configuration
- "About": gives information about the R&S ScopeSuite software
- "Tile View": allows a personalization of the compliance test selection You can configure which tests are visible in the compliance test section and which are hidden, so that only the ones you use are displayed.
- To hide a test from the "Compliance Tests" view, do one of the following:

Right-click on the compliance test that you want to hide.
 The icon of the test changes, see Figure 1-1. Now with a left click you can hide the test.



Figure 1-1: Unpin icon

b) Click on "Title View" to show a list of the available test cases. By clicking a test case in the show list, you can pin/unpin it from the main panel.

2 Preparing the measurements

2.1 Test equipment

For DDR4 compliance tests, the following test equipment is needed:

- R&S RTP with 4 channels and minimum 8 GHz bandwidth
- R&S RTP-K93 DDR4 compliance test option (required option, installed on the R&S RTP)
- 4 modular probes, R&S ZM90 with 9 GHz bandwidth. See also Chapter 2.1.1, "Soldering guide for modular probes", on page 9.
- 4 modular probe tips R&S RT-ZMA10 or R&S RT-ZMA14
- The free-of-charge R&S ScopeSuite software, which can be installed on a computer or directly on the R&S RTP.

2.1.1 Soldering guide for modular probes

All single-ended signals such as ADD, CMD, DQ, DM, CS, CKE should be soldered so that the signal is connected to the + part on the probe tip. The ground of the signal should be connected to the - part on the same probe tip.

All differential signals such as CK, DQS should be soldered differentially:

- The + signal is connected to the + part on the probe tip.
- The signal is connected to the part on the same probe tip.
- The ground of the signal is connected to the ground of the same probe tip.

2.2 Installing software and license

The preparation steps are performed only once for each computer and instrument that are used for testing.



Uninstall older versions of the R&S ScopeSuite

If an older version of the R&S ScopeSuite is installed, make sure to uninstall the old version before you install the new one. You can find the version number of the current installation in "Help" menu > "About". To uninstall the R&S ScopeSuite, use the Windows " Control Panel" > "Programs".

For best operation results, we recommend that the installed firmware versions of the R&S ScopeSuite and the oscilloscope are the same.

To install the R&S ScopeSuite

- Download the latest R&S ScopeSuite software from the "Software" section on the Rohde & Schwarz R&S RTP website: www.rohde-schwarz.com/product/rtp.html
- 2. Install the R&S ScopeSuite software:
 - On the computer that is used for testing, or
 - On the R&S RTP.

For system requirements, refer to the Release Notes.

To install the license key on the R&S RTP

When you got the license key of the compliance test option, enable it on the oscilloscope using [Setup] > "SW Options".

For a detailed description, refer to the R&S RTP user manual, chapter "Installing Options", or to the online help on the instrument.

2.3 Setting up the network

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection.

There are two ways of connection:

- LAN (local area network): It is recommended that you connect to a LAN with DHCP server. This server uses the Dynamic Host Configuration Protocol (DHCP) to assign all address information automatically.
- Direct connection of the instruments and the computer or connection to a switch using LAN cables: Assign fixed IP addresses to the computer and the instruments and reboot all devices.

To set up and test the LAN connection

- 1. Connect the computer and the instruments to the same LAN.
- 2. Start all devices.
- 3. If no DHCP server is available, assign fixed IP addresses to all devices.
- 4. Ping the instruments to make sure that the connection is established.
- 5. If VISA is installed, check if VISA can access the instruments.
 - a) Start VISA on the test computer.
 - b) Validate the VISA address string of each device.

See also:

• Chapter 2.5, "Connecting the R&S RTP", on page 11

2.4 Starting the R&S ScopeSuite

To start the R&S ScopeSuite on the test computer or on the oscilloscope:

Double-click the R&S ScopeSuite program icon.

To start the R&S ScopeSuite on the instrument, in the R&S RTP firmware:

▶ In the "Apps" dialog, open the "Compliance" tab.

2.5 Connecting the R&S RTP

If the R&S ScopeSuite is installed directly on the instrument, the software detects the R&S RTP firmware automatically, and the "Oscilloscope" button is not available in the R&S ScopeSuite.

If the R&S ScopeSuite software runs on a test computer, the computer and the testing oscilloscope require a LAN connection, see Chapter 2.3, "Setting up the network", on page 10. The R&S ScopeSuite software needs the IP address of the oscilloscope to establish connection.

- 1. Start the R&S RTP.
- 2. Start the R&S ScopeSuite software.
- 3. Click "Settings" > "Oscilloscope".

R&S ScopeSuite					-		_ 🗆 ×
					Tile V	'iew 🚺 About	P Help
Settings	Compliance Tes	ts					
Oscilloscope	Ethermet	1000BASE-T1	USB3.2-RX	НДМІ	eMMC		
C Instruments		- ワ - 二 2.5/5/106 2.5/5/106 MGBASE-T1	DDR3	DisplayPort	Demo		
Report	10BASE-T1	PCle	DDR4	MIPI D-PHY			
	100BASE-T1	USB	DDR5	MIPI C-PHY			
Welcome to complia	nce tests selection scr	een.					

4. Enter the IP address of the oscilloscope.

To obtain the IP address: press the Rohde & Schwarz logo at the top-right corner of the oscilloscope's display.

5. Click "Get Instrument Information".

The computer connects with the instrument and gets the instrument data.

RSScopeSuite	_ 🗆 ×
G Back Oscilloscope Settings	1 About 1 Help
Oscilloscope	
IP address: 10.113.10.30	
Get instrument information	
Device: RTO	
Serial Number: 400132	
Firmware Version: 2.60.2.7	
Restore Settings On Exit: 💿 Never 🔿 Ask 🔿 Always	
Connect software to your RTO.	

If the connection fails, an error message is shown.

2.6 Report configuration

In the "Report Configuration" menu, you can select the format of the report and the details to be included in the report. You can also select an icon that is displayed in the upper left corner of the report.

Also, you can enter common information on the test that is written in the "General Information" section of the test report.

Report configuration

R&S ScopeSuite						•	_ 🗆 🗙
G Back Report Settings						() About	P Help
Content	Format		lcon				
Display Summary 🗸		PDF		Re C	Change		
Display Detail 🗸		O Word Document		X9			
Display Properties 🗸							
Display Screenshots 🗸		Display SVG Chart ✔					
Reports Directory							
Directory				🗘 Change	😭 Open		
User Input							
Device Under Test (DUT)							
User							
Site							
Temperature							
Comments							
Configure default settings for new se	ession						

3 Performing tests

3.1 Starting a test session

R&S ScopeSuite						×	
G Back Complian	ce Tests DDR4				About	P Help	
Select Type	Select Type DDR4 OLPDDR4 LPDDR4X 						
Select Speed	Select Speed 1600 1866 2133 2400 2666 2933 3200 4266 Custom 0						
Session Name	Last Accessed	Comment					
DDR4_4266_20230524_140	5/24/2023 9:14:40 PM	Type in your comment.					
DDR4_4266_20230523_15	5/23/2023 3:17:36 PM	Type in your comment.					
🕂 Add 🖬 Open	Remove 🖳 Ren	ame 舅 Comment	Show Report				
Add new or open existing s	ession to run.						

After you open a compliance test, the "Session Selection" dialog appears. In this dialog, you can create new sessions, open or view existing report.

The following functions are available for handling test sessions:

Function	Description
"Add"	Adds a new session
"Open"	Opens the selected session
"Remove"	Removes the selected session
"Rename"	Changes the "Session Name"
"Comment"	Adds a comment
"Show report"	Generates a report for the selected session

To add a test session

- 1. In the R&S ScopeSuite window, select the compliance test.
- 2. In the "Session Selection" dialog press "Add".
- 3. If necessary change the "Session Name"

To open a test session

- 1. In the R&S ScopeSuite window, select the compliance test.
- 2. In the "Session Selection" dialog, select the session you want to open and double click on it.

Alternatively, select the session and press "Open".

To show a report for a test session

- 1. In the R&S ScopeSuite window, select the compliance test.
- 2. In the "Session Selection" dialog, select the session you want the report for and press "Show report".

3.2 Configuring the test

- 1. In the R&S ScopeSuite window, select the compliance test to be performed:
 - "DDR4"
- 2. Select the DDR4 type and the speed.
- 3. Open a test session, see Chapter 3.1, "Starting a test session", on page 14.
- 4. Adjust the "Properties" settings for the test cases you want to perform.
- Click "Limit Manager" and edit the limit criteria, see Chapter 3.2.1.1, "Limit manager", on page 17.
- If you want to use special report settings the "Report Config" tab to define the format and contents of the report. Otherwise the settings defined in "RSScopeSuite" > "Settings" > "Report" are used. See Chapter 2.6, "Report configuration", on page 12.
- Click "Test Checked"/"Test Single" and proceed as described in the relevant test case chapter.

3.2.1 General test settings

R&S Scop	R&S ScopeSuite								
G Back	Session DDR4_1600_20190724_143734					C Show Report	About	🕜 Help	
	▲ All	Properties	Limit Manage	er Results	Report Config				
	▲ Timing Tests	Threshold	d Settinas					Â	
	 Clock Timing (13.3) 			4.0	7			- 1	
	 Data Timing (4.24.1.2, 4.24.1.3) 		Vdd	1.2	v			- 1	
	 Strobe Timing (8.3.1, 4.24.1, 4.25.1) 		Vref	0.6	v			- 1	
	 Command Timing (13.7) 		VrefDQ	0.84	v			- 1	
	 Address Timing (13.7) 		Vss	0	v			- 1	
	 Chip Select Timing (13.7) 		Vdda	1.2	v			- 1	
	Electrical Tests							- 1	
	 Single-Ended Measurements 		Vtt		v			- 1	
	▼ AC & DC Input Levels for ADD and CMD (8.1)		Vssq	0	V			- 1	
	 AC Input Levels for CK (8.3.3) 	A	C Level for CA	◉ 100				- 1	
	 AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4) 	D	C Level for CA	0 75				- 1	
	 AC Overshoot & Undershoot for CK (8.3.5) 	DQS Trig	gering for R	ead/Writ	e Separation			- 1	
	 AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6) 	T			An all and a			- 1	
	 Input Slew Rate for ADD and CMD (8.4.2) 	i rigger	ing Method	Phase		Ē	Advanced	- 1	
	 AC & DC Output Levels for DQ (9.2) 	In	esnola Mode	 Absolut 	e O Relative			- 1	
	 Output Slew Rate for DQ (9.4) 	Upj	per Threshold	0.5	V			- 1	
	 Differential Measurements 	Mid	dle Threshold	0	v			- 1	
	 AC & DC Input Levels for CK (8.3.2) 	Lov	ver Threshold	-0.5	v			- 1	
	 Input Slew Rate for CK (8.4.1) 				_			- 1	
	 Differential Cross Point Voltage for CK (8.5) 	Test Setu	р					- 1	
	 AC Input Levels for DQS (8.7.2) 	A.c.	rago Window	200	Pariode			- 1	
	 AC Differential Cross Point Voltage for DQS (8.7.4) 	~~~~	rage window	200	renous			- 1	
	 Input Slew Rate for DQS (8.7.5) 	Ave	rage Window	200	Periods			- 1	
	 Differential AC Output Levels for DQS (9.3) 	R	ecord Length	20	us			- 1	
	 Differential Output Slew Rate for DQS (9.5) 		Burst Count	All 🔻]				
		Speed Bin(C	L-nRCD-nRP)	1600J(🔻]				
		CA	S Latency(CL)	9 🔻					
		CAS Write	Latency(CWL)	9 🔻					
🛃 Test	Checked	Data	Bus Inversion						
Ready to re	un.								

Each session dialog is divided into several sections:

 "Properties": shows the settings that can be made for the test case selected on the left side of the dialog. You can differentiate between the "All" and the sub test properties

In the "All" > "Properties" tab you can configure the settings for all test cases in the current session. Once you change and save a setting in this tab, the changes will be done for all test in the sessions. At the same time, there will be a special marking for the functions that have different settings for different sub tests.

- "Limit Manager": sets the measurement limits that are used for compliance testing, see Chapter 3.2.1.1, "Limit manager", on page 17.
- "Results": shows an overview of the available test results for this session.
- "Instruments": defines instruments settings for connecting to external devices, that are specific for this test session.
 When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Instruments") are copied to the session. This "Instruments" tab can be used to change those copied defaults.
- "Report Config": defines the format and contents of the report for this session.

When a session is first created the global settings ("RSScopeSuite" > "Settings" > "Report") are copied to the session. This "Report Config" tab can be used to change those copied defaults.

• "Test Checked"/ "Test Single": starts the selected test group.

3.2.1.1 Limit manager

The "Limit Manager" shows the measurement limits that are used for compliance testing.

Each limit comprises the comparison criterion, the unit, the limit value A, and a second limit value B if the criterion requires two limits.

You can set the values to defaults, change the values in the table, export the table in xml format, or import xml files with limit settings.

You can also return the values to the original limits with "Reset to default".

► Check and adjust the measurement limits.

Configuring the test

Properties Limit Manager Results Report C	Config			
Measurement	Criteria	Unit	А	В
Clock Period Absolute Min	x>=A 💌	s	1.18E-09	
Clock Period Absolute Max	x<=A 💌	s	1.57E-09	
Clock Average Low Pulse Width	A<=x<=B ▼	%	47	53
Clock Absolute Low Pulse Width	x>=A 🐨	%	43	
Clock Average High Pulse Width	A<=x<=B ▼	%	47	53
Clock Absolute High Pulse Width	x>=A 📼	%	43	
Clock Period Jitter maximum value	A<=x<=B ▼	s	-7E-11	7E-11
Clock Period Jitter minimum value	x>=A 📼	s	-7E-11	
Clock Cycle-to-Cycle Period Jitter	x<=A ▼	s	1.4E-10	
Cumulative Error for 2 cycle minimum value	A<=x<=B ▼	s	-1.03E-10	1.03E-10
Cumulative Error for 3 cycle minimum value	A<=x<=B ▼	s	-1.22E-10	1.22E-10
Cumulative Error for 4 cycle minimum value	A<=x<=B ▼	s	-1.36E-10	1.36E-10
Cumulative Error for 5 cycle minimum value	A<=x<=B ▼	s	-1.47E-10	1.47E-10
Cumulative Error for 6 cycle minimum value	A<=x<=B ▼	s	-1.55E-10	1.55E-10
Cumulative Error for 7 cycle minimum value	A<=x<=B ▼	s	-1.63E-10	1.63E-10
Cumulative Error for 8 cycle minimum value	A<=x<=B ▼	s	-1.69E-10	1.69E-10
Cumulative Error for 9 cycle minimum value	A<=x<=B ▼	s	-1.75E-10	1.75E-10
Cumulative Error for 10 cycle minimum value	A<=x<=B ▼	s	-1.8E-10	1.8E-10

3.2.2 Test configuration for DDR4

The test configuration consists of some test-specific configuration settings. The values for the settings in this tab depend on the selected "Speed" and "Type" of standard.

Configuring the test

R&S ScopeSuite _ 🗆 X								
🕒 Bac	Session DDR4_1600_20190724_143734					🖹 Show Report	About	🕜 Help
	▲ All	Properties	Limit Manage	er Results	Report Config			
	▲ Timing Tests	Threshold	d Settinas					Î
	 Clock Timing (13.3) 				1			
	 Data Timing (4.24.1.2, 4.24.1.3) 		Vdd	1.2	v			
	 Strobe Timing (8.3.1, 4.24.1, 4.25.1) 		Vref	0.6	V			
	 Command Timing (13.7) 		VrefDQ	0.84	v			
	 Address Timing (13.7) 		Vss	0	v			
	 Chip Select Timing (13.7) 		Vddq	1.2	lv			
	Electrical Tests							
	 Single-Ended Measurements 		Vtt] v			
	 AC & DC Input Levels for ADD and CMD (8.1) 		Vssq	0	v			
	 AC Input Levels for CK (8.3.3) 	A	C Level for CA	100				
	 AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4) 	D	C Level for CA	0 75				
	 AC Overshoot & Undershoot for CK (8.3.5) 	DQS Trig	gering for R	lead/Write	e Separation			
	 AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6) 	Triago	ing Mathod	Z Bhase	Amplituda			
	 Input Slew Rate for ADD and CMD (8.4.2) 	The	asheld Meda			Ē	Advanced	
	▼ AC & DC Output Levels for DQ (9.2)		esnoid wode	Absolution	e 🔾 Relative			
	 Output Slew Rate for DQ (9.4) 	Up	per Threshold	0.5	v			
	Differential Measurements	Mid	dle Threshold	0	v			
	 AC & DC Input Levels for CK (8.3.2) 	Lov	wer Threshold	-0.5	v			
	 Input Slew Rate for CK (8.4.1) 	T 1 C 1			-			
	 Differential Cross Point Voltage for CK (8.5) 	Test Setu	р					
	 AC Input Levels for DQS (8.7.2) 	Ave	rage Window	200	Periods			
	 AC Differential Cross Point Voltage for DQS (8.7.4)]			
	▼ Input Slew Rate for DQS (8.7.5)	AVe	rage window	200	Periods			
<u> </u>	Differential AC Output Levels for DQS (9.3)	F	lecord Length	20	us			
	 Differential Output Slew Rate for DQS (9.5) 		Burst Count	All 🔻]			
		Speed Bin(C	L-nRCD-nRP)	1600J(🔻]			
		CA	S Latency(CL)	9 🔻				
		CAS Write	Latency(CWL)	9 🔻]			
✓ Test	Checked	Data	Bus Inversion					
Ready to r	un.							

Figure 3-1: Configuration for DDR4 compliance tests

Signals

Selects the channel for the specified signal.

For electrical tests, consider also how many test signals are enabled. For example, if only the ADD/CMD signal is selected, only ADD/CMD signal is used to run the test. If both the ADD and the CMD signals are selected, test is run using ADD signal first, followed by the CMD signal.

Also, for some test cases "Invert" is available. To invert means to reflect the voltage values of all signal components against the ground level.

You can use inversion, for example, to switch the polarity of a differential signal without changing the probe connections.

The following signals are available according to the selected test case:

'ADD"	Address	signal.
-------	---------	---------

- "CMD" Command signal.
- "CK" Differential clock input signal.
- "DQS" Data strobe signal.
- "DQ" Data input/output signal.
- "DM" Data mask signal.

"CS" Chip select signal.

"CKE" Clock enable signal.

Probe mode

Selects between the "Single ended" and "Differential" mode for connecting the probe tips.

Available for the following electrical single-ended signals tests: "AC Input Levels for CK", "AC overshoot & undershoot for CK" and "AC overshoot & undershoot for DQ, DQS, and DM".

Threshold Settings

The following threshold settings are defined:

"V _{DD} "	Power supply
"V _{REF} "	Reference voltage
"V _{REFDQ} "	DQ reference voltage
"V _{SS} "	Ground
"V _{DDQ} "	DQ power supply
"V _{TT} "	$V_{TT} = V_{DDQ}/2$
"V _{SSQ} "	DQ Ground
"AC Level for CA"	AC level for the command address.
"DC Level for CA"	DC level for the command address.
"Hysteresis"	Hysteresis in %.

Separation method

Selects the separation method.

"Phase"	Checks the phase difference between DQ and DQS to differentiate
	the type (read or write) of burst.

"Amplitude" Checks the peak-peak amplitude difference between read and write signals on DQS to differentiate the type (read or write) of burst.

"Advanced" Enables the definition of more detailed trigger conditions:

- "Min Phase for Read"/"Max Phase for Read": sets the minimum/ maximum phase for the read burst.
- "Min Phase for Write"/"Max Phase for Write": sets the minimum/ maximum phase for the write burst.
- "Amplitude Relationship": sets the amplitude relationship between the read and write burst.
- "P-P Amplitude Threshold": sets the peak-peak amplitude threshold.

Threshold Mode

Selects between the absolute and relative threshold mode.

Upper/Middle/Lower Threshold ← Threshold Mode

Sets the upper/middle/lower for the absolute threshold mode.

Set the top/middle/base ratio for the relative threshold mode.

Selects the trigger method.

Preamble type

Selects the preamble type to process read or write bursts with different preamble configurations as defined in the specifications.

You can select between:

- "Auto": can be selected for preamble configurations that are not defined in specifications.
- 1TCK
- 2TCK

Scaling method

Selects the scaling method.

"Auto" The vertical scaling of the oscilloscope is adjusted so that the waveform is displayed around 80% of the screen.

"Reference" The vertical scaling is fixed with accordance to the specification.

Write Trigger Method

Selects the type of trigger used to trigger the write bursts in the waveforms.

Edge - Write Trigger Method

For "Edge" trigger, DQS and DQ signals are triggered by their edges. For DQS, edges along 0 V are triggered. For DQ, edges along V_{ref} are triggered.

ABR - Write Trigger Method

Selects an A-B-R trigger sequence:

- A: Trigger on DQ edge.
- B: Trigger on DQS edge.
- R: Reset if cannot find a burst with DQ and DQS edge with half UI difference.

"A -> B Delay": sets the time that the instrument waits after an A-trigger until it recognizes B-triggers.

"Reset Timeout": the instrument waits for the "Reset Timeout" time for the specified number of B-triggers. If no trigger occurs during that time, the sequence is restarted with the A-trigger.

"DQS Noise Reject" / "DQ Noise Reject": sets the number of neighboring samples that are skipped for differentiation of DQ/DQS.

Width Write Trigger Method

For "Width" trigger, triggers DQS signal if its pulse width is within the specified width. "Width": the width defines the center of a range which is defined by the limits of "Delta". "Delta": defines a range around the given width value.

"Noise Reject": sets the number of neighboring samples that are skipped for differentiation.

Zone - Write Trigger Method

For "Zone" trigger, three exclusion zones are placed to trigger write bursts.

Average Window

Sets the average window in periods.

Record Length

Sets the number of waveform samples in one waveform record.

Timeout Length

Sets how long the oscilloscope waits for a signal transition before throwing out timeout error.

Eye stable wait time

The time that is waited for, before starting to build the eye for "Input Receiver Compliance Mask for Voltage and Timing" tests.

Burst Count

Sets the burst count.

Speed Bin (CL-nRCD-nRP)

Selects which speed bin is used for the tests.

CAS Latency (CL)

Selects the value for the CAS latency. It is the delay, measured in clock cycles, between the internal read command and the availability of the first bit of output data.

CAS Write Latency (CWL)

Selects the value for the CAS write latency. It is the delay, measured in clock cycles, between the internal write command and the availability of the first bit input data.

Clear Scope Internal

Clears the oscilloscope, if a communication error has occurred.

Expert Mode

If enabled, the "Expert Mode" allows you to bypass the guided steps of the test case.

Data Bus Inversion

Enables data bit inversion. It helps to improve the signal integrity and reduce the power consumption.

Test Setup for Mask Compliance

Defines the mask settings for the "Input Receiver Compliance Mask for Voltage and Timing (13.6)" test case.

"Acquisition Length for Eye"	The time length of waveform used to draw eye.
"Mask Height"	Sets the height of the waveform mask in the vertical direction.
"Mask Width"	Sets the width of the waveform mask in the horizontal direction.
"Jump Step"	Sets how much % the mask is moved for each iteration.

Histogram Settings for Mask Compliance

Defines the histogram settings for the "Input Receiver Compliance Mask for Voltage and Timing (13.6)" test case.

You can set the following parameters as the boundaries of the histogram:

- "Left Horizontal Start"
- "Left Horizontal Stop"
- "Right Horizontal Start"
- "Right Horizontal Stop"
- "Vertical Start"

Export Waveforms

Enables you to export a waveform. You can later load the waveforms to run the tests in the offline mode, see Offline Execution.

You can define an export directory, or use the default one:

MyDocuments\Rohde-Schwarz\RSScopeSuite\<Version>\Waveforms\
<ComplianceTest>\<SubTest>\<Speed>\<SessionName>

For example:

```
MyDocuments\Rohde-Schwarz\RSScopeSuite\4.10.0\Waveforms\DDR4\
DDR4\2133\DDR4_2133_20190114_144116
```

Offline Execution

Offline Execution			
Enable	✓		
CK waveform		-7	Select
DQS waveform			Select
DQ waveform		-	Select
CMD waveform		-	Select
ADD waveform		-	Select
CS waveform			Select
CKP waveform			Select
CKN waveform			Select
DQSP waveform			Select
DQSN waveform			Select
DM waveform			Select
CKCM waveform			Select
DQSCM waveform		-	Select

If enabled, allows you to use exported waveforms as a source for the execution of the compliance test.

You can select one waveform for each needed signal.

3.3 Initiating the test

To perform compliance tests, the device under test is connected to the test board in a test-specific way. Using a probe, the test board is connected with the R&S RTP. The probe connections are test-specific. The R&S ScopeSuite guides you step-by-step through the connection setup and the test sequence.

- 1. Set the test setup on a nonconductive, static-approved work surface.
- 2. In the R&S ScopeSuite window, select the compliance test.
- 3. Open a test session, see Chapter 3.1, "Starting a test session", on page 14.
- Check the test configuration settings and adjust, if necessary. See: Chapter 3.2, "Configuring the test", on page 15.

5. Click "Test Checked" for starting all checked test cases or "Test Single" for starting only the selected test case.

The R&S ScopeSuite test wizard explains the following individual setup steps. A detailed test description can be found in the following chapters:

Chapter 3.5, "Starting DDR4 tests", on page 26

3.4 Getting test results

For each Ethernet test, the test data - report, diagrams and waveform files - is saved in the following folder:

```
%ProgramData%\Rohde-Schwarz\RSScopeSuite\5.40.1\Sessions\
Sessions\<DDR category>\<Session Name>
```

If you resume an existing session, new measurements are appended to the report, new diagrams and waveform files are added to the session folder. Existing files are not deleted or replaced. Sessions data remain until you delete them in the "Results" tab of the session.

The report format can be defined in "RSScopeSuite" > "Settings" > "Report" for all compliance tests (see also Chapter 2.6, "Report configuration", on page 12). If you want to use special report settings for a session, you can define the format and contents of the report in the "Report Config" tab of the session.

All test results are listed in the "Results" tab. Reports can be provided in PDF, MSWord, or HTML format. To view and print PDF reports, you need a PDF viewer, for example, the Acrobat Reader.

The test report file can be created at the end of the test, or later in the "Session Selection" dialog.

To show a test report

- 1. In the R&S ScopeSuite window, select the compliance test to be performed.
- 2. Select the session name in the "Session Selection" dialog and click "Show report".

The report opens in a separate application window, depending on the file format. You can check the test results and print the report.

To delete the results, diagrams and waveform files of a session

- 1. In the "Session Selection" dialog select the session and open it.
- 2. In the "Results" tab, select the result to be deleted.
- 3. Click "Remove".

3.5 Starting DDR4 tests

Before you run the test, complete the following actions:

- LAN connection of the oscilloscope and the computer running the R&S Scope-Suite, see Chapter 2.5, "Connecting the R&S RTP", on page 11
- 1. Select "DDR4" in the R&S ScopeSuite start window.
- In the "Session Selection" dialog, set the "Select Type" standard. The following "Types" are available:
 - "DDR4": Double data rate type three. Used for desktops and servers.
 - "LPDDR4": low power DDR4. Consumes very low power and is used for mobile phones.
 - "LPDDR4X": low power DDR4 extended. Consumes very low power and is used for mobile phones. Its headlined lower I/O voltage to save system power.
- Set the "Select Speed". There are preset speeds you can select from: "1600"/"1866"/"2133"/"2400"/"2666"/"2933"/"3200"/"4266"/
 "Custom": user selected value. The values in the "Limit Manager" tab are set according to the selected speed.
- 4. Add a new test session.
- 5. Open the session. For details, see Chapter 3.1, "Starting a test session", on page 14.
- 6. Check the test configuration settings. Adjust, if necessary. See:
 - Chapter 3.2.2, "Test configuration for DDR4", on page 18
 - Chapter 3.2.1.1, "Limit manager", on page 17
- 7. Select/check the test cases you want to run and click "Test Single"/"Test checked".
- 8. A step-by step guide explains the following individual setup steps. When you have finished all steps of the step-by-step guide, the compliance test runs automatically.

4 Timing tests

4.1 Clock timing

4.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	probe with minimum 9 GHz bandwidth	1
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	1
DUT	DDR4 device that supports the selected type	1

4.1.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Timing Tests" > "Clock Timing".

R&S ScopeS	uite	• - □ >
G Back	Session DDR4_1600_20240610_173755	🖹 Show Report 🕧 About 👔 Help
	. All	Properties Limit Manager Results Report Config
	▲ Timing Tests	Signals
✓	 Clock Timing (13.3) 	Invert
 Image: A start of the start of	tCK(abs) (13.3.1)	CK 🕰 Ch1 🔻
✓	tCK(avg) (13.3.2)	Test Setup
~	tCL(avg) (13.3.3)	
~	tCH(avg) (13.3.3)	Average Window 200 Periods
~	t/IT(per) (13.3.4)	Record Length 10 us
~	tJIT(duty) (13.3.4)	Speed Pip/CL pDCD pDD
 Image: A start of the start of	tJIT(cc) (13.3.4)	Speed Bil(CL=IKCD=IKP) 1600J(*
~	tERR(nper) (13.3.4)	CAS Latency(CL) 12
	▼ Data Timing (4.24.1.2, 4.24.1.3)	CAS Write Latency(CWL) 9 👻
	▼ Strobe Timing (8.3.1, 4.24.1, 4.25.1)	Clear Scope Internal 📮 Clear
	 Command Timing (13.7) 	Expert Mode
	 Address Timing (13.7) 	
	▼ Chip Select Timing (13.7)	Export Waveforms
	✓ Electrical Tests	Enable
		Offline Execution
		Enable
🛃 Test Cl	hecked 🕨 Test Single	
eady to run	h.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

4.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

4.1.4 Measurements

The clock timing measurements consist of up to eight measurements. They test the limits as defined in the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4) specifications.

4.1.4.1 Average clock period - t_{CK(avg)}

This test aims to verify that the average clock period tCK(avg) is within the limits defined in section 13.3.2 (DDR4)/ 10.1.1 (LPDDR4/LPDDR4X) of the specification. tCK(avg) is the average clock period calculated across any consecutive 200 cycle window. The clock period is defined from rising edge to rising edge.

4.1.4.2 Absolute clock period - t_{CK(abs)}

This test aims to verify that the average absolute clock period tCK(abs) is within the limits defined in section 13.3.1 (DDR4)/ 10.1.2 (LPDDR4/LPDDR4X) of the specification. tCK(abs) is the absolute clock period from one rising edge to the next rising edge.

4.1.4.3 Average low pulse width - t_{CL(avg)}

This test aims to verify that the average low pulse width tCL(avg) is within the limits defined in section 13.3.3 (DDR4)/ 10.1.3 (LPDDR4/LPDDR4X) of the specification. tCL(avg) is the average low pulse width, as calculated across any consecutive 200 low pulses.

4.1.4.4 Average high pulse Width - t_{CH(avg)}

This test aims to verify that the average high pulse width tCH(avg) is within the limits defined in section 13.3.3 (DDR4)/ 10.1.3 (LPDDR4/LPDDR4X) of the specification. tCH(avg) is the average low pulse width, as calculated across any consecutive 200 low pulses.

4.1.4.5 Clock period jitter - t_{JIT(per)}

This test aims to verify that the clock period jitter tJIT(per) is within the limits defined in section 13.3.4 (DDR4)/ 10.1.5 (LPDDR4/LPDDR4X) of the specification. It is the largest deviation of any signal t_{CK} from $t_{CK(avg)}$. It defines the single period jitter when the DLL is already locked.

4.1.4.6 Half period jitter - t_{JIT(duty)}

This test aims to verify that the half period jitter tJIT(duty) is within the limits defined in section 13.3.4 (DDR4)/ 10.1.6 (LPDDR4/LPDDR4X) of the specification. tJIT(duty) is the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.

4.1.4.7 Cycle to cycle period jitter - t_{JIT(cc)}

This test aims to verify that the cycle to cycle period jitter tJIT(cc) is within the limits defined in section 13.3.4 (DDR4)/ 10.1.6 (LPDDR4/LPDDR4X) of the specification. tJIT(cc) is the absolute difference in clock period between two consecutive clock cycles. It defines the cycle to cycle jitter when the DLL is already locked.

4.1.4.8 Cumulative error - t_{ERR(nper)}

This test aims to verify that the cumulative error tERR(nper) is within the limits defined in section 13.3.4 (DDR4)/ 10.1 (LPDDR4/LPDDR4X) of the specification. tERR(nper) is the cumulative error across n multiple consecutive cycles from tCK(avg).

4.2 Data timing

4.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	probe with minimum 9 GHz bandwidth	3

Item	Description, model	Quantity
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR4 device that supports the selected type	1

4.2.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Timing Tests" > "Data Timing".

R&S ScopeSuite	×
G Back Session DDR4_1600_202406	10_173755 Report 1 About 1 Help
All	Properties Limit Manager Results Report Config
Timing Tests	Invert
Clock Timing (13.3)	CK V ch1 V
Data Timing (4.24.1.2, 4.24.1.3)	
✓ tDQSQ (4.24.1.2)	DQ w the Ch3 v
✓ tQH (4.24.1.2)	Threshold Settings
✓ tLZ(DQ) (4.24.1.3)	Vdd 1.2 V
✓ tHZ(DQ) (4.24.1.3)	Vref 0.6 V
▼ Strobe Timing (8.3.1, 4.24.1, 4.2	5.1)
Command Timing (13.7)	VretDQ 0.84 V
Address Timing (13.7)	Vddq 1.2 V
Chip Select Timing (13.7)	Vtt 0.84 V
Electrical Tests	DOS Triggoring for Pood Mirito Separation
	Dus inggening for kead/write separation
	Separation Method 🗹 Phase 🗌 Amplitude 😝 Advanced
	Threshold Mode Absolute Relative
	Upper Threshold 0.5 V
	Middle Threshold 0 V
	lower Threshold -0.5 V
	Scaling Method Auto
	Write Trigger Method 💿 Edge 🛛 ABR 🔷 Width 🔷 Zone
	Test Setup
	Record Length 10 us
	Burst Count 10 🔻
Test Checked Test Single	Data Bus Inversion
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

4.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

4.2.4 Measurements

The data timing measurements consist of up to 10 measurements. They test the limits as defined in the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4) specifications.

4.2.4.1 DQS-DQ Skew for DQS and associated DQ Signals - t_{DQSQ}

This test aims to verify that the strobe to data skew, per group, per access is within the limits defined in section 4.24.1.2 (DDR4)/ 10.5 (LPDDR4/LPDDR4X) of the specification.

4.2.4.2 DQ/DQS output hold time from DQS - t_{QH}

This test aims to verify that the data output hold time from strobe is within the limits defined in section 4.24.1.2 (DDR4)/ 10.5 (LPDDR4/LPDDR4X) of the specification.

4.2.4.3 DQ Out high impedance time from CK_t/CK_c - t_{HZ(DQ)}

This test aims to verify that the data high impedance time from CK_t/CK_c is within the limits defined in section 4.24.1.3 (DDR4) of the specification.

4.2.4.4 DQ Low-Impedance time from CK_t/CK_c - t_{LZ(DQ)}

This test aims to verify that the data low impedance time from CK_t/CK_c is within the limits defined in section 4.24.1.3 (DDR4) of the specification.

4.3 Strobe timing

4.3.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR4 device that supports the selected type	1

4.3.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Timing Tests" > "Strobe Timing".

R&S Scop	eSuite	• _ ¤ ×
G Back	k Session DDR4_4266_20230524_140535	Kan Show Report 1 About 1 Help
	▲ All	Properties Limit Manager Results Report Config
	Timing Tests	Signals
	 Clock Timing (13.3) 	Junet .
	▼ Data Timing (4.24.1.2, 4.24.1.3)	CK J ch1 -
	▲ Strobe Timing (8.3.1, 4.24.1, 4.25.1)	DQS V ch2 -
 Image: A set of the set of the	tDVAC(Strobe) (8.3.1)	DQ V Ch3 V
 Image: A second s	tDVAC(Clock) (8.3.1)	Threshold Settings
 Image: A start of the start of	tLZ(DQS) (4.24.1)	
 Image: A start of the start of	tHZ(DQS) (4.24.1)	Vdd 1.2 V
 Image: A start of the start of	tDQSCK (4.24.1)	Vref 0.6 V
	tQSH (4.24.1)	VrefDQ 0.84 V
 Image: A set of the set of the	tQSL (4.24.1)	Vddq 1.2 V
	tRPRE (4.24.1)	Vtt 0.84 V
 Image: A start of the start of	tRPST (4.24.1)	
	tDQSS (4.25.1)	DQS Triggering for Read/Write Separation
	tDQSH (4.25.1)	Separation Method 🗸 Phase Amplitude 📕 Advanced
	tDQSL (4.25.1)	
	tDSS (4.25.1)	
	tDSH (4.25.1)	Upper Inresnola U.S
	tWPRE (4.25.1)	Middle Threshold 0 V
	tWPST (4.25.1)	Lower Threshold -0.5 V
	 Command Timing (13.7) 	Scaling Method 💿 Auto 🔷 Reference
	✓ Address Timing (13.7)	Write Trigger Method Fdge ABR Width Zone
	▼ Chip Select Timing (13.7)	
	✓ Electrical Tests	Test Setup
		Preamble Type 🔵 Auto 💿 1TCK 💿 2TCK
		Record Length 10 us
		Timeout Length 35 s
		Burst Count 10 -
		Data Bus Inversion
		Expert Mode
		Export Waveforms
		Enable
		Offline Execution
Test	Checked 🕨 Test Single	Enable

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.

 You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

4.3.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

4.3.4 Measurements

The strobe measurements consist of up to 10 measurements. They test the limits as defined in the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4) specifications.

4.3.4.1 Time before ringback - t_{DVAC(Strobe)}

This test aims to verify that the time before ringback for strobe is within the limits defined in section 8.3.1 of the DDR4 specification. tDVAC(Strobe) is the "time above AC-level" during a differential AC-swing.

4.3.4.2 Time before ringback - t_{DVAC(Clock)}

This test aims to verify that the time before ringback for CK /CK# is within the limits defined insection 8.3.1 of the DDR4 specification. tDVAC(Clock) is the "time above AC-level" during a differential AC-swing.

4.3.4.3 Low-Impedance time from CK/CK# - t_{LZ}(DQS)

This test aims to verify that the strobe low-impedance time is within the limits defined in section 4.24.1 (DDR4) of the specification.

4.3.4.4 High-Impedance time from CK/CK# - t_{HZ}(DQS)

This test aims to verify that the strobe high-impedance time is within the limits defined in section 4.24.1 (DDR4) of the specification.

4.3.4.5 DQS output access time from CK/CK # - t_{DQSCK}

This test aims to verify that the strobe rising edge output access time from rising CK/CK# is within the limits defined in section 4.24.1 (DDR4) of the specification.

4.3.4.6 Differential read preamble - t_{RPRE}

This test aims to verify that the strobe differential READ preamble is within the limits defined in section 4.24.1 (DDR4) of the specification.

4.3.4.7 Read postamble - t_{RPST}

This test aims to verify that the strobe differential READ postamble is within the limits defined in section 4.24.1 (DDR4) of the specification.

4.3.4.8 Differential output high time - t_{QSH}

This test aims to verify that the strobe differential output high time is within the limits defined in section 4.24.1 (DDR4)/ 10.5 (LPDDR4/LPDDR4X) of the specification.

4.3.4.9 Differential output low time - t_{QSL}

This test aims to verify that the strobe differential output low time is within the limits defined in section 4.24.1(DDR4)/ 10.5 (LPDDR4/LPDDR4X) of the specification.

4.3.4.10 DQS latching transition to associated clock edge - t_{DQSS}

This test aims to verify that the time interval from the strobe rising edge to CK/CK# rising edge is within the limits defined in section 4.25.1 (DDR4)/ 4.11.2 (LPDDR4/ LPDDR4X) of the specification.

4.3.4.11 DQS input high pulse width - t_{DQSH}

This test aims to verify that the strobe differential input high pulse width is within the limits defined in section 4.25.1 (DDR4)/ 4.11.2 (LPDDR4/LPDDR4X) of the specification.

4.3.4.12 DQS input low pulse width - t_{DQSL}

This test aims to verify that the strobe differential input low pulse width is within the limits defined in section 4.25.1 (DDR4)/ 4.11.2 (LPDDR4/LPDDR4X) of the specification.

4.3.4.13 DQS falling edge to CK setup time - t_{DSS}

This test aims to verify that the time interval from the strobe falling edge setup time to the CK/CK# rising edge is within the limits defined in section 4.25.1 (DDR4)/ 4.11.2 (LPDDR4/LPDDR4X) of the specification.

4.3.4.14 DQS falling edge hold time from CK - t_{DSH}

This test aims to verify that the strobe falling edge hold time from CK/CK# rising edge is within the limits defined in section 4.25.1 (DDR4)/ 4.11.2 (LPDDR4/LPDDR4X) of the specification.

4.3.4.15 Write preamble - t_{WPRE}

This test aims to verify that the strobe differential WRITE preamble is within the limits defined in section 4.25.1 (DDR4) of the specification.

4.3.4.16 Write postamble - t_{WPST}

This test aims to verify that the strobe differential WRITE postamble is within the limits defined in section 4.25.1 (DDR4) of the specification.

4.4 Command timing

4.4.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

4.4.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Timing Tests" > "Command Timing".
Command timing

R&S ScopeSuite		×
G Back Session DDR4_1600_20240610_173755		Show Report About P Help
All	Properties Limit Manager Results	Report Config
Timing Tests	Signals	
Clock Timing (13.3)	-	Invert
Data Timing (4.24.1.2, 4.24.1.3)	CMD 🎝 Ch4 🔻	
▼ Strobe Timing (8.3.1, 4.24.1, 4.25.1)	CK 🛴 Ch1 🔻	
Command Timing (13.7)	Threshold Settings	
✓ tlS(base) (13.7)	Vdd 12 V	
✓ tlH(base) (13.7)	Vdd 1.2 V	
✓ tIPW (13.7)	Vref 0.6 V	
Address Timing (13.7)	Hysteresis 7.5 %	
Chip Select Timing (13.7)	AC Level for CA 💿 100	
Electrical Tests	DC Level for CA 🔘 75	
	Test Setup	
	Record Length 10 us	
	Burst Count 10 💌	
	Clear Scope Internal 📮 Clear	
	Expert Mode	
	Export Waveforms	
	Enable	
	Offline Execution	
	Enable	
✓ Test Checked Test Single		
Ready to run.		

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

4.4.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

4.4.4 Measurements

The command timing measurements consist of up to six measurements. They test the limits as defined in section 13.7 (DDR4) of the JESD79-4B(DDR4) specifications.

4.4.4.1 Address and control input setup time - t_{IS}

This test aims to verify that the command and address setup time from CK/CK# is within the limits defined in the specification.

4.4.4.2 Address and control input hold time - t_{IH}

This test aims to verify that the command and address hold time from CK/CK# is within the limits defined in the specification.

4.4.4.3 Address and control input pulse width t_{IPW}

This test aims to verify that the control and address input pulse width for each input is within the limits defined in the specification.

4.5 Address timing

4.5.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

4.5.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Timing Tests" > "Address Timing".

Address timing

R&S ScopeSuite	×
G Back Session DDR4_1600_20240610_173755	C Show Report D About D Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Clock Timing (13.3)	Invert
Data Timing (4.24.1.2, 4.24.1.3)	ADD Ch4 🐨
✓ Strobe Timing (8.3.1, 4.24.1, 4.25.1)	CK 🗸 Ch1 🔻
Command Timing (13.7)	Threshold Settings
Address Timing (13.7)	
✓ tlS(base) (13.7)	Vaa 1.2 V
✓ tlH(base) (13.7)	Vref 0.6 V
✓ tIPW (13.7)	Hysteresis 7.5 %
Chip Select Timing (13.7)	AC Level for CA 🔘 100
Electrical Tests	DC Level for CA 🔘 75
	Test Setup
	Record Length 10 us
	Burst Count 10 🐨
	Clear Scope Internal
	Expert Mode
	Export Waveforms
	Enable
	Offline Execution
Test Checked Test Single	Enable 🗌
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

4.5.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

4.5.4 Measurements

The address timing measurements consist of up to six measurements. They test the limits as defined in section 13.7 of the JESD79-4B(DDR4) specification.

For details on the measurements, see Chapter 4.4.4, "Measurements", on page 37.

4.6 Chip select timing

4.6.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

4.6.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Timing Tests" > "Chip Select Timing".

Chip select timing

R&S ScopeSuite	~ ×
G Back Session DDR4_1600_20240610_173755	C Show Report 1 About 1 Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Clock Timing (13.3)	Invert
✓ Data Timing (4.24.1.2, 4.24.1.3)	CK / _ Ch1 👻 🗌
▼ Strobe Timing (8.3.1, 4.24.1, 4.25.1)	CS ↓ Ch4 ▼
Command Timing (13.7)	Threshold Settings
Address Timing (13.7)	
Chip Select Timing (13.7)	Vdd 1.2 V
✓ tlS(base) (13.7)	Vref 0.6 V
✓ tlH(base) (13.7)	Hysteresis 7.5 %
✓ tIPW (13.7)	AC Level for CA 💿 100
Electrical Tests	DC Level for CA () 75
	Test Setup
	lest Setup
	Record Length 10 us
	Burst Count 10 👻
	Clear Scope Internal
	Expert Mode
	Export Waveforms
	Enable
	Offline Execution
	Enable
Test Checked Test Single	
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

4.6.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

4.6.4 Measurements

The chip select timing measurements consist of up to six measurements. They test the limits as defined in section 13.7 (DDR4) of the JESD79-4B(DDR4) specifications.

4.6.4.1 Address and control input setup time - t_{IS}

This test aims to verify that the chip select setup time from CK/CK# is within the limits defined in the specification.

4.6.4.2 Address and control input hold time - t_{IH}

This test aims to verify that the chip select hold time from CK/CK# is within the limits defined in the specification.

4.6.4.3 t_{IPW}

This test aims to verify that the chip select input pulse width for each input is within the limits defined in the specification.

5 Electrical tests

5.1 Single-ended signals

5.1.1 Input receiver compliance mask for voltage and timing

5.1.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.1.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "Input Receiver Compliance Mask for Voltage and Timing (13.6)".

Single-ended signals

R&S ScopeSuite	• - ¤
G Back Session DDR4_4266_20230524_140535	Ka Show Report 1 About 1 He
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Electrical Tests	Invert
Single-Ended Measurements	DQS Ch2 -
Input Receiver Compliance Mask for Voltage and Timing (13.6)	✓ DQ 🖓 Ch3 ▼
✓ tDQS2DQ	Threshold Settings
✓ TdIPW	
VIHL	VretDQ 0.84 V
✓ srr1	Vddq 1.2 V
✓ srf1	Vtt 0.6 V
✓ srr2	DOS Triggoring for Boad Allrito Soparation
✓ srf2	DQS higgening for Read/write Separation
AC & DC Input Levels for ADD and CMD (8.1)	Separation Method 🗹 Phase 🗌 Amplitude 📮 Advanced
AC Input Levels for CK (8.3.3)	Threshold Mode Absolute Relative
▲ AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4)	Upper Threshold 0.5 V
AC Overshoot & Undershoot for CK (8.3.5)	Middle Threshold 0 V
▲ AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6)	
Input Slew Rate for ADD and CMD (8.4.2)	Lower Infestiona -0.5
AC & DC Output Levels for DQ (9.2)	Test Setup
Output Slew Rate for DQ (9.4)	Deced Levels 10
Differential Measurements	kecord Length 10 us
	Burst Count 10 V
	Expert Mode
	Test Setup for Mask Compliance
	Acquisition Length for Eye 833 ns
	Mask Height 0.13 V
	Mask Width 0.2
	Jump Step 0.05
	Histogram Settings for Mask Compliance
	Left Horizontal Start 15 %
	Left Horizontal Stop 45 %
	Right Horizontal Start 60 %
	Right Horizontal Stop 90 %
	Vertical Start 35 %
	Export Waveforms
	Enable
	Offline Execution
☑ Test Checked ► Test Single	Enable
Ready to run.	

 Enable the "Signals" you want to use. If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.

If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.

- 4. Enable the tests that you want to run.
- 5. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.

7. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.1.4 Measurements

The AC and DC logic input levels for single-ended address and command measurements consist of up to four measurements. It tests the limits as defined in section 13.6 (DDR4) of the JESD79-4B(DDR4) specification.

tDQS2DQ

This tests aim to verify that the receiver Rx Mask DQS to DQ offset is within the limits defined in the specification.

T_{dIPW}

This test aims to verify that the DQ input pulse width is within the limits defined in the specification.

VIHL

This test aims to verify that V_{IHL} , the peak to peak voltage with respect to the Vcent DQ level is within the limits defined in the specification.

srr1/ srr2

This tests aim to verify that the rising edge slew rates are within the limits defined in the specification.

srf1/srf2

This tests aim to verify that the falling edge slew rates are within the limits defined in the specification.

5.1.2 AC & DC input levels for ADD and CMD

5.1.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.2.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "AC & DC Input Levels for ADD and CMD".

R&S ScopeSu	ite				- 🗆 ×
🕒 Back	Session DDR4_4266_20231024_102526		💦 Show Report	About	🕜 Help
•	All	Properties Limit Manager Results Report Config			
	 Timing Tests 	Signals			
	 Electrical Tests 	Invert			
	 Single-Ended Measurements 	🖌 ADD 🖓 Ch2 🔻			
	 Input Receiver Compliance Mask for Voltage and Timing (13.6) 	🗸 CMD 🆓 Ch4 🔻			
	 AC & DC Input Levels for ADD and CMD (8.1) 	Threshold Settings			
	VIH(AC)				
	VIL(AC)	Vdd 1.2 V			
	VIH(DC)	Vref 0.6 V			
	VIL(DC)	AC Level for CA 💿 100			
	 AC Input Levels for CK (8.3.3) 	DC Level for CA 💿 75			
	 AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4) 	Test Setup			
	 AC Overshoot & Undershoot for CK (8.3.5) 				
	 AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6) 	Record Length 10 us			
	 Input Slew Rate for ADD and CMD (8.4.2) 	Clear Scope Internal			
	 AC & DC Output Levels for DQ (9.2) 	Emert Made			
	 Output Slew Rate for DQ (9.4) 	Expert Mode			
	 Differential Measurements 	Export Waveforms			
		Enable			
		Offline Execution			
🛃 Test Che	ccked 🕨 Test Single	Enable			
Ready to run.					

3. Enable the "Signals" you want to use.

If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.

If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.

4. Enable the tests that you want to run.

- 5. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 7. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.2.4 Measurements

The AC and DC logic input levels for single-ended address and command measurements consist of up to four measurements. It tests the limits as defined in section 8.1.1(DDR4) of the JESD79-4B(DDR4) specification.

V_{IH(AC)}

This test aims to verify that the AC input logic high is within the limits defined in the specification.

V_{IL(AC)}

This test aims to verify that the AC input logic low is within the limits defined in the specification.

V_{IH(DC)}

This test aims to verify that the DC input logic high is within the limits defined in the specification.

V_{IL(DC)}

This test aims to verify that the DC input logic low is within the limits defined in the specification.

5.1.3 AC input levels for CK

5.1.3.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.3.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Single-Ended Signals" > "AC Input Levels for CK".

R&S ScopeSuite	• _ □ ×
G Back Session DDR4_4266_20230928_151732	🖹 Show Report 🚺 About 👔 Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Electrical Tests	Broke Made CircleTeded
Single-Ended Measurements	
Input Receiver Compliance Mask for Voltage and Timing (13.6)	CK Ch1 T
	Thrashold Sattings
AC Input Levels for CK (8.3.3)	
VSEH VSEH	Vdd 1.2 V
✓ VSEL	Vref 0.6 V
➡ AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4)	AC Level for CA 💿 100 🔿 135 🔿 150 🔿 160 🔾 175
	Tart Satur
AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6)	lest setup
Input Slew Rate for ADD and CMD (8.4.2)	Record Length 10 us
Output Slew Rate for DQ (9.4)	
Differential Measurements	Expert Mode
	Export Waveforms
	Enable
	Office Execution
	Online Execution
	Enable
Test Checked Fast Single	
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.

 You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.3.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.3.4 Measurements

The single-ended AC input levels for clock and strobe measurements consist of up to two measurements. It tests the limits as defined in section 8.3.3 (JESD79-4B(DDR4))/ 7.2.3 JESD209-4B(LPDDR4) of the specifications.

V_{SEH(AC)}

This test aims to verify that the single-ended high level for strobes/clock is within the limits defined in the specification.

V_{SEL(AC)}

This test aims to verify that the single-ended low level for strobes/clock is within the limits defined in the specification.

5.1.4 Output levels for DQ

5.1.4.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.4.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Single-Ended Signals" > "Output Levels for DQ".

R&S Scop	tas ScopeSuite 🛛 🚽 🗠 🗸 🗆 🗸 🗠				
G Back	Session LPDDR4_4266_20231024_104543		C Show Report	About	🕐 Help
	▲ All	Properties Limit Manager Results Report Config			
	▼ Timing Tests	Signals			î
	 Electrical Tests 	Invert			
	 Single-Ended Measurements 	DQS Ch2 🔻			
	▼ AC Input Levels for CK (7.2.3)	DQ DQ Ch3 🔻			
	▲ Output Levels for DQ (7.4)	Threshold Settings			
	VOH	Vidia 11 V			
	VOL				
	 AC Overshoot & Undershoot for ADD and CTRL (7.1.3.1) 	Vtt 0.55 V			
	 Overshoot & Undershoot for LVSTL for CK, CS, CKE, and ODT (7.6) 	DQS Triggering for Read/Write Separation			
	 Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6) 				
	 Output Slew Rate for DQ 	Separation Method 🗹 Phase 🗌 Amplitude	Advanced		
	 Differential Measurements 	Threshold Mode Absolute Relative			
		Upper Threshold 0.12 V			
		Middle Threshold -0.055 V			
		Lower Threshold -0.18 V			
		Test Setup			- 1
		Record Length 10 us			
		Burst Count 10 -			
		Clear Scope Internal 📮 Clear			
		Expert Mode			- 1
		E an a d M and fa man			
		export waveforms			
		Enable			
🕞 Test	Checked Fast Single	Offline Execution			v
Ready to r	un.				

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.4.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.4.4 Measurements

The single-ended output levels for strobe measurements consist of up to two measurements. It tests the limits as defined in section 7.4 of the JESD209-4B(LPDDR4) specification.

V_{OH}

This test aims to verify that the output high measurement level for the output slew rate is within the limits defined in the specification.

V_{OL}

This test aims to verify that the output low measurement level for the output slew rate is within the limits defined in the specification.

5.1.5 AC overshoot & undershoot for ADD, CMD and CTRL (DDR4)

This chapter is only relevant for DDR4 tests.

5.1.5.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.5.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "AC Overshoot & Undershoot for ADD, CMD and CTRL".

Single-ended signals

R&S ScopeSuite	×
G Back Session DDR4_4266_20231024_102526	🖹 Show Report 🚺 About 👔 Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Electrical Tests	Invert
Single-Ended Measurements	ADD The Ch2 🔻
Input Receiver Compliance Mask for Voltage and Timing (13.6)	CMD Ch4 V
☐ ★ AC & DC Input Levels for ADD and CMD (8.1)	Threshold Settings
AC Input Levels for CK (8.3.3)	
AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4)	Vdd 1.2 V
VAOSP	Vref 0.6 V
VAOS VAOS	Vss 0 V
VAUS VAUS	Test Satur
AAOS2	lest Setup
AAOS1	Record Length 10 us
AAUS	
✓ AC Overshoot & Undershoot for CK (8.3.5)	
AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6)	Expert Mode
	Export Waveforms
✓ AC & DC Output Levels for DQ (9.2)	Enable
Output Slew Rate for DQ (9.4)	
Differential Measurements	Offline Execution
Test Chacked Test Single	Enable
- rest officience	
Ready to run.	

3. Enable the "Signals" you want to use.

If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.

If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.

- 4. Enable the tests that you want to run.
- 5. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.5.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.5.4 Measurements

The overshoot and undershoot for address and control measurements consist of up to six measurements. It tests the limits as defined in section 8.3.4 of the JESD79-4B(DDR4) specification.

VAOSP

This test aims to verify that the maximum peak amplitude above V_{AOS} is within the limits defined in the specification.

V_{AOS}

This test aims to verify that the upper boundary of overshoot area A_{AOS1} is within the limits defined in the specification.

V_{AUS}

This test aims to verify that the maximum peak amplitude allowed for undershoot is within the limits defined in the specification.

A_{AOS2}

This test aims to verify that the maximum overshoot area per 1 t_{CK} above V_{AOS} is within the limits defined in the specification.

A_{AOS1}

This test aims to verify that the maximum overshoot area per 1 t_{CK} between VDD and V_{AOS} is within the limits defined in the specification.

A_{AUS}

This test aims to verify that the maximum undershoot area per 1 t_{CK} below VSS is within the limits defined in the specification.

A_{AOS}

This test aims to verify that the maximum overshoot area per 1 t_{CK} below VSS is within the limits defined in the specification.

5.1.6 AC overshoot & undershoot for ADD and CTRL (LPDDR4/ LPDDR4X)

This chapter is only relevant for LPDDR4/LPDDR4X tests.

5.1.6.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.6.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "AC Overshoot & Undershoot for ADD and CTRL".

R&S ScopeSuite	¤ ×
G Back Session LPDDR4_4266_20231024_104543	Show Report About Help
AII	Properties Limit Manager Results Report Config
Timing Tests	Signals
Clock Timing (10.1)	Invert
✓ Data Timing (10.5)	ADD Ch2 V
✓ Strobe Timing (4.11.2, 10.5)	CMD CH4 🔻
Command Timing	Threshold Settings
▲ Address Timing	
Chip Select Timing	Vaa I.I V
Electrical Tests	Vref 0.55 V
Single-Ended Measurements	Vss 0 V
AC Input Levels for CK (7.2.3)	Tast Satur
▼ Output Levels for DQ (7.4)	lest Setup
AC Overshoot & Undershoot for ADD and CTRL (7.1.3.1)	Record Length 10 us
Overshoot & Undershoot for LVSTL for CK, CS, CKE, and ODT (7.6)	Clear Scope Internal 📃 Clear
Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6)	
Output Slew Rate for DQ	Expert Mode
Differential Measurements	Export Waveforms
	Enable
	Offling Execution
Iest Checked Field Iest Single	Enable
Ready to run.	

3. Enable the "Signals" you want to use.

If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.

If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.

- 4. Enable the tests that you want to run.
- 5. Click "Test Single".

- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.6.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.6.4 Measurements

The overshoot and undershoot for address and control measurements consist of up to four measurements. It tests the limits as defined in section 7.1.3.1 of the JESD209-4B(LPDDR4) specification.

For details on the measurements, see Chapter 5.1.5.4, "Measurements", on page 53.

V_{AOS}

This test aims to verify that the upper boundary of overshoot area A_{AOS} is within the limits defined in the specification.

V_{AUS}

This test aims to verify that the maximum peak amplitude allowed for undershoot is within the limits defined in the specification.

A_{AOS}

This test aims to verify that the maximum overshoot area per 1 t_{CK} below VSS is within the limits defined in the specification.

A_{AUS}

This test aims to verify that the maximum undershoot area per 1 t_{CK} below VSS is within the limits defined in the specification.

5.1.7 AC overshoot & undershoot for CK

This chapter is only relevant for DDR4 tests.

5.1.7.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	1
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	1
DUT	DDR4 device that supports the selected type	1

5.1.7.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "AC Overshoot & Undershoot for CK".

R&S ScopeSuite	×
G Back Session DDR4_4266_20231024_102526	R Show Report 1 About 1 Help
All	Properties Limit Manager Results Report Config
	Signals
Electrical Tests	- Broho Mada O CircleForded Differential
Single-Ended Measurements	
 Input Receiver Compliance Mask for Voltage and Timing (13.6) 	
AC & DC Input Levels for ADD and CMD (8.1)	
✓ AC Input Levels for CK (8.3.3)	
AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4)	Vdd 1.2 V
AC Overshoot & Undershoot for CK (8.3.5)	Vref 0.6 V
VCOSP	Vss 0 V
VCOS	
VCUS VCUS	lest Setup
ACOS2	Record Length 10 us
ACOS1	
ACUS	Clear Scope Internal E Clear
AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6)	Expert Mode
■ Input Slew Rate for ADD and CMD (8.4.2)	Export Waveforms
AC & DC Output Levels for DQ (9.2)	Fnable
Output Slew Rate for DQ (9.4)	
Differential Measurements	Offline Execution
Test Checked Test Single	Enable
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.7.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.7.4 Measurements

The overshoot and undershoot for clock measurements consist of up to six measurements. It tests the limits as defined in section 8.3.5 (DDR4) of the JESD79-4B(DDR4) specification.

V_{COSP}

This test aims to verify that the maximum peak amplitude above V_{COS} is within the limits defined in the specification.

V_{cos}

This test aims to verify that the upper boundary of overshoot area A_{DOS1} is within the limits defined in the specification.

V_{CUS}

This test aims to verify that the maximum peak amplitude allowed for undershoot is within the limits defined in the specification.

A_{COS2}

This test aims to verify that the maximum overshoot area per 1 UI above V_{COS} is within the limits defined in the specification.

A_{COS1}

This test aims to verify that the maximum overshoot area per 1 UI between VDD and V_{AOS} is within the limits defined in the specification.

Acos

This test aims to verify that the maximum overshoot area is within the limits defined in the specification.

A_{CUS}

This test aims to verify that the maximum undershoot area per 1 UI below VSS is within the limits defined in the specification.

5.1.8 Overshoot & undershoot for LVSTL for CK, CS, CKE and ODT

This chapter is only relevant for LPDDR4/LPDDR4X tests.

5.1.8.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	3
DUT	DDR4 device that supports the selected type	1

5.1.8.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "Overshoot & Undershoot for LVSTL for CK, CS, CKE and ODT".

▲ All Propertie Linkt Manager Report Config ● • Timing Tests Signals ● ▲ Electrical Tests Inverti ● ● A Clipput Levels for CK (7.2.3) Inverti ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● <td< th=""><th>G Back Session LPDDR4_4266_20231024_104543</th><th>Show Report O About V Help</th></td<>	G Back Session LPDDR4_4266_20231024_104543	Show Report O About V Help
Image TestsSignalsImage TestsImage TestsImag	All	Properties Limit Manager Results Report Config
 Electrical Tests Single-Ended Measurements AC Input Levels for CK (7.2.3) Output Levels for CQ (7.4) A C Overshoot & Undershoot for LVSTL for CX. CS. CKE. and ODT (7.6) AC Overshoot & Undershoot for LVSTL for CX. CS. CKE. and ODT (7.6) VCOS ACOS ACONFONDA & Undershoot for LVSTL for DQ. DQS and DMI (7.6) ACONFONDA & Undershoot for LVSTL for DQ. DQS and DMI (7.6) ACONFONDA & Undershoot for CK (7.2.1) ACONFONDA & Undershoot for CK (7.2.1) ACONFONDA & Undershoot for CK (7.2.4) ACONFONDA & Undershoot for CK (7.2.5) ACONFONDA & CONFONDA & CONF	▼ Timing Tests	Signals
 Single-Ended Measurements A Cliput Levels for CK (7.2.3) Output Levels for CK (7.2.3) Output Levels for DQ (7.4) A C Overshoot & Undershoot for LVSTL for CK, CK, E and ODT (7.6) VCOS VCOS VCOS A COS VCOS VCO	Electrical Tests	Invert
· AC Input Levels for CK (7.2.3) · Output Levels for DQ (7.4) · AC Overshoot & Undershoot for ADD and CTRL (7.13.1) · · · · · · · VCOS · · · VCOS · · · <td< td=""><td>Single-Ended Measurements</td><td>CK 🖓 Ch1 🔻</td></td<>	Single-Ended Measurements	CK 🖓 Ch1 🔻
· ○ Output Levels for DQ (7.4) · AC Overshoot & Undershoot for ADD and CTRL (7.13.1) · · · · · · · VCOS · · · VCUS · · · <td>AC Input Levels for CK (7.2.3)</td> <td>CS Ch2 🗸</td>	AC Input Levels for CK (7.2.3)	CS Ch2 🗸
• AC Overshoot & Undershoot for ADD and CTRL (7.13.1) • Overshoot & Undershoot for IVSTL for CK, CS, CKE, and ODI (7.6) • VCOS • VCUS • VCUS • ACOS • ACOS • Overshoot & Undershoot for IVSTL for CR, CS, CKE, and ODI (7.6) • VCUS • ACOS • ACOS • Overshoot & Undershoot for IVSTL for CR, CS, CKE, and ODI (7.6) • ACOS • ACOS • Overshoot & Undershoot for IVSTL for DQ, DQS and DMI (7.6) • Overshoot & Undershoot for IVSTL for DQ, DQS and DMI (7.6) • Output Slew Rate for DQ • Output Slew Rate for CR (7.2.1) • Input Slew Rate for CR (7.2.4) • Input Slew Rate for DQS (7.2.6) • Input Slew Rate for DQS (7.2.9) • AC Output Levels for DQS (7.2.9) • Output Slew Rate for DQS (7.5)	Output Levels for DQ (7.4)	CKE Ch3 🔻
Image: Constraint & Undershoot for UVSTL for CK, CS, CKE, and ODT (7.6) VCOS VCOS VCUS VCUS ACOS ACOS ACUS VOUTUS Output Slew Rate for DQ VAC & DC Input Levels for CK (7.2.1) Image: Control Light Levels for DQS (7.2.6) VAC Output Levels for DQS (7.2.9) VAC Output Slew Rate for DQS (7.5) VAC Output Slew Rate for DQS (7.5)	➡ AC Overshoot & Undershoot for ADD and CTRL (7.1.3.1)	Threshold Settings
VCOS VCUS VCUS Veef ACOS Veef ACOS Veef ACUS Veef Output Slew Rate for DQ Veef VOutput Slew Rate for CK (7.2.1) Test Setup AC Input Slew Rate for DQ (7.2.6) Expert Mode Veef Note Expert Mode Veef Note Expert Mode Veef Note Expert Mode Veef Note Clear Veef Note Expert Mode Veef Note Expert Mode Veef Note Expert Mode Veef Note Expert Mode	Overshoot & Undershoot for LVSTL for CK, CS, CKE, and ODT (7.6)	
VCUS Vef 0.55 V ACOS Vss 0 V ACUS Test Setup Output Slew Rate for DQ Record Length 10 us ACUS Burst Court 10 v ACUS Clear Scope Internal Elear ACUS Fortunation of the VSTL for DQS (7.2.6) Expert Mode ACUS Fortunation of the VSTL for DQS (7.2.9) Export Waveforms ACUS AC Couput Levels for DQS (7.2.9) Enable AC Output Slew Rate for DQS (7.5) Offline Execution	VCOS	vuu I.I
ACOS Vss ACUS Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6) Output Slew Rate for DQ Output Slew Rate for DQ AC & D C Input Levels for CK (7.2.1) AC A C Input Slew Rate for DQ (7.2.6) AC A C Unput Levels for DQS (7.2.6) AC A C Output Levels for DQS (7.2.9) AC A C Output Slew Rate for DQS (7.5) Output Slew Rate for DQS (7.5) Offline Execution	VCUS	Vref 0.55 V
ACUS • Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6) • Output Slew Rate for DQ • Output Slew Rate for DQ • AC & D Input Levels for CK (7.2.1) • Input Slew Rate for CK (7.2.4) • AC Input Levels for DQS (7.2.6) • Input Slew Rate for DQS (7.2.9) • AC Output Levels for DQS (7.2.9) • AC Output Slew Rate for DQS (7.5) • Output Slew Rate for DQS (7.5)	ACOS	Vss 0 V
• Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6) Record Length • Output Slew Rate for DQ Record Length • AC & Differential Measurements Burst Count • AC & DC Input Levels for CK (7.2.1) Clear Scope Internal • AC Input Slew Rate for DQS (7.2.6) Expert Mode • Input Slew Rate for DQS (7.2.9) Export Waveforms • AC Output Levels for DQS (7.5) Enable	ACUS ACUS	Tost Satura
Image: Control Stew Rate for DQ Record Length 10 us Image: Control Stew Rate for CK (7.2.1) Burst Count 10 Image: Clear Clear Scope Internal Image: Clear Scope	 Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6) 	lest Setup
A Differential Measurements Burst Count 10 ▼ AC & DC Input Levels for CK (7.2.1) Clear Scope Internal Clear Scope Internal ✓ Input Siew Rate for DQS (7.2.6) Expert Mode ✓ Input Siew Rate for DQS (7.2.9) Export Waveforms ✓ AC Output Levels for DQS Enable ✓ Output Siew Rate for DQS (7.5) Offline Execution	Output Slew Rate for DQ	Record Length 10 us
· AC & DC Input Levels for CK (7.2.1) Clear Scope Internal · Input Slew Rate for CK (7.2.4) Expert Mode · AC Input Levels for DQS (7.2.6) Expert Mode · Input Slew Rate for DQS (7.2.9) Export Waveforms · AC Output Levels for DQS Enable · Output Slew Rate for DQS (7.5) Offline Execution	Differential Measurements	Burst Count 10 -
Image:	▼ AC & DC Input Levels for CK (7.2.1)	Clear Scope Internal
• AC Input Levels for DQS (7.2.6) Expert Mode • Input Slew Rate for DQS (7.2.9) Export Waveforms • AC Output Levels for DQS Enable • Output Slew Rate for DQS (7.5) Offline Execution	▼ Input Slew Rate for CK (7.2.4)	
Image: market for DQS (7.2.9) Export Waveforms Image: market for DQS Enable Image: market for DQS (7.5) Offline Execution	AC Input Levels for DQS (7.2.6)	Expert Mode
A C Output Levels for DQS Enable Output Slew Rate for DQS (7.5) Offline Execution	▼ Input Slew Rate for DQS (7.2.9)	Export Waveforms
Output Slew Rate for DQS (7.5) Offline Execution	AC Output Levels for DQS	Enable
Offline Execution	Output Slew Rate for DQS (7.5)	
		Offline Execution

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.

 You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.8.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.8.4 Measurements

The overshoot and undershoot for clock measurements consist of up to four measurements. It tests the limits as defined in section 7.6 of the JESD209-4B(LPDDR4) specification.

For details on the measurements, see Chapter 5.1.7.4, "Measurements", on page 57.

5.1.9 AC overshoot & undershoot for DQ, DQS, and DM

This chapter is only relevant for DDR4 tests.

5.1.9.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2/3
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2/3
DUT	DDR4 device that supports the selected type	1

5.1.9.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "AC Overshoot & Undershoot for DQ, DQS, and DM".

Single-ended signals

R&S Scop	t&S ScopeSuite				
🕒 Bac	k Session DDR4_4266_20231024_102526	🖹 Show Report 🚺 About 👔 Help			
	▲ All	Properties Limit Manager Results Report Config			
	▼ Timing Tests	Signals			
	Electrical Tests				
	 Single-Ended Measurements 				
	 Input Receiver Compliance Mask for Voltage and Timing (13.6) 	DQ Ch3 =			
	 AC & DC Input Levels for ADD and CMD (8.1) 	DM 1 Ch4 =			
	 AC Input Levels for CK (8.3.3) 	✓ DQS_t √ Ch1 ▼			
	 AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4) 	DQS_c Ch2 V			
	 AC Overshoot & Undershoot for CK (8.3.5) 	Threshold Settings			
	 AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6) 				
	VDOSP	Vddq 1.2 V			
	VDOS	Vtt V			
	VDUS	Vssq 0 V			
	VDUSP				
	ADOS2	lest Setup			
	ADOS1	Record Length 10 us			
	ADUS1	_			
	ADUS2	Clear Scope Internal 📮 Clear			
	 Input Slew Rate for ADD and CMD (8.4.2) 	Expert Mode			
	 AC & DC Output Levels for DQ (9.2) 	Export Waveforms			
	 Output Slew Rate for DQ (9.4) 				
	Differential Measurements				
		Offline Execution			
☑ Test	t Checked 🕨 Test Single	Enable			
Ready to r	10				

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.9.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.9.4 Measurements

The overshoot and undershoot for data, strobe and mask measurements consist of up to 8 measurements. It tests the limits as defined in section 8.3.6 of the JESD79-4B(DDR4) specification.

VDOSP

This test aims to verify that the maximum peak amplitude above V_{DOS} is within the limits defined in the specification.

V_{DOS}

This test aims to verify that the upper boundary of overshoot area A_{DOS1} is within the limits defined in the specification.

V_{DUS}

This test aims to verify that the lower boundary of undershoot area is within the limits defined in the specification.

V_{DUSP}

This test aims to verify that the maximum peak amplitude below V_{DUS} is within the limits defined in the specification.

A_{DOS2}

This test aims to verify that the maximum overshoot area per 1 UI above V_{DOS} is within the limits defined in the specification.

A_{DOS1}

This test aims to verify that the maximum overshoot area per 1 UI between VDDQ and V_{DOS} is within the limits defined in the specification.

A_{DUS1}

This test aims to verify that the maximum undershoot area per 1 UI between VSSQ and V_{DUS1} is within the limits defined in the specification.

A_{DUS2}

This test aims to verify that the maximum undershoot area per 1 UI below V_{DUS} is within the limits defined in the specification.

5.1.10 Overshoot & undershoot for LVSTL for DQ, DQS, and DMI

This chapter is only relevant for LPDDR4/LPDDR4X tests.

5.1.10.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.10.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "Overshoot & Undershoot for LVSTL for DQ, DQS, and DMI".

R&S ScopeSuite	×
G Back Session LPDDR4_4266_20231024_104543	R Show Report 1 About 1 Help
All	Properties Limit Manager Results Report Config
▼ Timing Tests	Signals
Electrical Tests	Invert
Single-Ended Measurements	DQS The Ch2 -
AC Input Levels for CK (7.2.3)	🗸 DQ 🖓 ch3 🔻
✓ Output Levels for DQ (7.4)	Threshold Settings
AC Overshoot & Undershoot for ADD and CTRL (7.1.3.1)	Video 11 V
Overshoot & Undershoot for LVSTL for CK, CS, CKE, and ODT (7.6)	
Overshoot & Undershoot for LVSTL for DQ, DQS and DMI (7.6)	Vtt 0.55 V
VDOS VDOS	Vssq 0 V
VDUS	Tort Satur
ADOS	lest setup
ADUS	Record Length 10 us
Output Slew Rate for DQ	Burst Count 10 🔻
Differential Measurements	Clear Scope Internal
AC & DC Input Levels for CK (7.2.1)	
Input Slew Rate for CK (7.2.4)	Expert Mode
AC Input Levels for DQS (7.2.6)	Export Waveforms
Input Slew Rate for DQS (7.2.9)	Enable
AC Output Levels for DQS	Offling Eventtion
Output Slow Date for DOS (7.5)	- Online Execution
Ist Checked P lest Single	Enable
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.10.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.10.4 Measurements

The overshoot and undershoot for clock measurements consist of up to four measurements. It tests the limits as defined in section 7.6 of the JESD209-4B(LPDDR4) specification.

For details on the measurements, see Chapter 5.1.9.4, "Measurements", on page 60.

5.1.11 Input slew rate for ADD and CMD

This chapter is only relevant for DDR4 tests.

5.1.11.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	de & Schwarz oscilloscope R&S RTP with 4 channels and minimum 8 GHz band- width	
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.11.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "Input Slew Rate for ADD and CMD".

Single-ended signals



 Enable the "Signals" you want to use.
 If only the ADD/CMD signal is selected, only ADD/CMD signal will be used to run the test.

If both the ADD and the CMD signals are selected, test will be run using ADD signal first, followed by the CMD signal.

- 4. Enable the tests that you want to run.
- 5. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.11.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.11.4 Measurements

The input slew rates for address and command measurements consist of up to four measurements. It tests the limits as defined in sections 8.3.6 of the JESD79-4B(DDR4) specification.

Setup slew rate rising - SR(tIS) rising

This test aims to verify that the setup slew rate for rising signal is within the limits defined in the specification.

Setup slew rate falling - SR(tIS) falling

This test aims to verify that the setup slew rate for falling signal is within the limits defined in the specification.

Hold slew rate rising - SR(tIH) rising

This test aims to verify that the hold slew rate for rising signal is within the limits defined in the specification.

Hold slew rate falling - SR(tlH) falling

This test aims to verify that the hold slew rate for falling signal is within the limits defined in the specification.

5.1.12 AC & DC output levels for DQ

5.1.12.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.12.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Single-Ended Signals" > "AC & DC Output Levels for DQ".

R&S 5	copeSuite		×
G	Back Session DDR4_4266_20231024_102526	Rq Show Report 1 About 1 H	alp
	▲ All	Properties Limit Manager Results Report Config	
	▼ Timing Tests	Signals	î
	▲ Electrical Tests	Invert	
	▲ Single-Ended Measurements	DQS 🕂 Ch2 🔻	
	 Input Receiver Compliance Mask for Voltage and Timing (13.6) 	🗸 DQ 🎝 Ch3 🔻	
	 AC & DC Input Levels for ADD and CMD (8.1) 	Threshold Settings	
	▼ AC Input Levels for CK (8.3.3)		
	▼ AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4)	Vddq 1.2	
	▼ AC Overshoot & Undershoot for CK (8.3.5)	Vtt 0.6 V	
	▼ AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6)	DQS Triggering for Read/Write Separation	
	 Input Slew Rate for ADD and CMD (8.4.2) 		
	AC & DC Output Levels for DQ (9.2)	Separation Method 🗹 Phase 🗌 Amplitude 📕 Advanced	
	VOH(AC)	Threshold Mode Absolute Relative	
	VOL(AC)	Upper Threshold 0.5 V	
	VOH(DC)	Middle Threshold 0 V	
	VOL(DC)	Lower Threshold -0.5 V	
	 Output Slew Rate for DQ (9.4) 		
	 Differential Measurements 	Test Setup	
		Preamble Type 🔵 Auto 💿 1TCK 💿 2TCK 💿 Others	I
		Record Length 10 us	
		Burst Count 10 💌	I
		Clear Scope Internal 📮 Clear	I
		Expert Mode	I
		Export Waveforms	
	Test Checked Fast Single	Enable 🗌	Ļ
Ready	to run.		

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.12.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.12.4 Measurements

The AC & DC output levels for data measurements consist of up to four measurements. It tests the limits as defined in section 9.2 of the JESD79-4B(DDR4) specifications.

V_{OH(AC)}

This test aims to verify that the AC output high measurement level for the output slew rate is within the limits defined in the specification.

V_{OL(AC)}

This test aims to verify that the AC output low measurement level for the output slew rate is within the limits defined in the specification.

V_{OH(DC)}

This test aims to verify that the DC output high measurement level for IV curve linearity is within the limits defined in the specification.

V_{OL(DC)}

This test aims to verify that the DC output low measurement level for IV curve linearity is within the limits defined in the specification.

5.1.13 Output slew rate for DQ

5.1.13.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	cope R&S RTP with 4 channels and minimum 8 GHz band- width	
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.1.13.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Single-Ended Signals" > "Output Slew Rate for DQ".

R&S Sco	peSuite						• _ 🗆 ×
🕒 Ba	* Session DDR4_4266_20231024_102526				🖹 Show Re	port 🚺 Ab	out 🕜 Help
	▲ All	Properties	Limit Manager	Results	Report Config		
	▼ Timing Tests	Signals					î
	 Electrical Tests 				Invert		
	▲ Single-Ended Measurements		DQS	Ch2 🔻			
	 Input Receiver Compliance Mask for Voltage and Timing (13.6) 		🗸 DQ 🏹	Ch3 🔻			
	▼ AC & DC Input Levels for ADD and CMD (8.1)	Threshold	d Settings				
	▼ AC Input Levels for CK (8.3.3)) (dd= 1	2			
	▼ AC Overshoot & Undershoot for ADD, CMD and CTRL (8.3.4)		vaaq 1.	2 V			
	▼ AC Overshoot & Undershoot for CK (8.3.5)		Vtt 0.	6 V			
	 AC Overshoot & Undershoot for DQ, DQS and DM (8.3.6) 	DQS Tria	aerina for Rea	d/Write Se	paration		
	 Input Slew Rate for ADD and CMD (8.4.2) 	- 5.			_		
	▼ AC & DC Output Levels for DQ (9.2)	Separa	tion Method 🗹	Phase	Amplitude	📮 Advance	d
	 Output Slew Rate for DQ (9.4) 	Thi	reshold Mode 🧿	Absolute	 Relative 		
✓	SRQse Rising	Up	per Threshold 0.	5 V			
✓	SRQse Falling	Mid	dle Threshold 0	v			
	Differential Measurements	Lov	ver Threshold -0	0.5 V			
		Test Setu	p				
		P	reamble Type 🔵	Auto	ITCK	🔿 2ТСК	Others
		R	Record Length 10) us			
			Burst Count 10) 🔻			
		Clear S	Scope Internal 📮	Clear			
			Expert Mode				
		Export W	aveforms				
⊡≱ Tes	t Checked 🕨 Test Single		Enable				
Ready to	run.						×.

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.1.13.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.1.13.4 Measurements

The single-ended output slew rate for data consists of up to two measurements. It tests the limits as defined in section 9.4 (DDR4) / 7.4 (LPDDR4) / 4.2 (LPDDR4X) of the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4)/JESD209-4-1(LPDDR4X) specifications.

Slew rate query output single-ended signals rising- SRQse rising

This test aims to verify that the single-ended output slew rate for rising edge is within the limits defined in the specification. It is measured from VOL(AC) to VOH(AC).

Slew rate query output single-ended signals falling - SRQse falling

This test aims to verify that the single-ended output slew rate for falling edge is within the limits defined in the specification. It is measured from VOH(AC) to VOL(AC).

5.2 Differential signals

5.2.1 AC & DC input levels for CK

5.2.1.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	1
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	1
DUT	DDR4 device that supports the selected type	1

5.2.1.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Differential Signals" > "AC &DC Input Levels for CK".

Differential signals



- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.1.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.2.1.4 Measurements

The differential AC input levels for clock and strobe measurements consist of up to two measurements. It tests the limits as defined in section 8.3.2 (JESD79-4B(DDR4)) / 7.2.1 (JESD209-4B(LPDDR4)) of the specifications.

Differential input high AC - VIHdiff(AC)

This test aims to verify that the AC differential input high is within the limits defined in the specification.

Differential input low AC - VILdiff(AC)

This test aims to verify that the AC differential input low is within the limits defined in the specification.

Differential input high DC - VIHdiff(DC)

This test aims to verify that the DC differential input high is within the limits defined in the specification.

Differential input low DC - VILdiff(DC)

This test aims to verify that the DC differential input low is within the limits defined in the specification.

5.2.2 Input slew rate for CK

5.2.2.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	1
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	1
DUT	DDR4 device that supports the selected type	1

5.2.2.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Single-Ended Signals" > "Input Slew Rate for CK".

Differential signals

R&S ScopeSuite	×
G Back Session DDR4_4266_20231025_104711	🖹 Show Report 🚺 About 👔 Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Electrical Tests	Invert
Single-Ended Measurements	CK 🖓 Ch1 👻
Differential Measurements	Threshold Settings
AC & DC Input Levels for CK (8.3.2)	Ved 12 V
✓ Input Slew Rate for CK (8.4.1)	vuu 1.2 v
SRIdiff Rising	Vref 0.6 V
SRIdiff Falling	Test Setup
Differential Cross Point Voltage for CK (8.5)	
▼ AC Input Levels for DQS (8.7.2)	Record Length 10 us
AC Differential Cross Point Voltage for DQS (8.7.4)	Clear Scope Internal 📮 Clear
▼ Input Slew Rate for DQS (8.7.5)	Expert Mode
Differential AC Output Levels for DQS (9.3)	
Differential Output Slew Rate for DQS (9.5)	Export Waveforms
	Enable
	Offline Execution
	Enable
Test Checked Test Single	
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.2.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.2.2.4 Measurements

The input slew rates for clock measurements consist of up to two measurements. It tests the limits as defined in sections 8.4.1 (DDR4)/ 7.2.4 (LPDDR4/LPDDR4X) of the JESD79-4B(DDR4)/ (JESD209-4B(LPDDR4)) specifications.
Differential input slew rate rising - SR(diff) rising

This test aims to verify that the setup slew rate for rising signal is within the limits defined in the specification.

Differential input slew rate falling - SR(diff) falling

This test aims to verify that the setup slew rate for falling signal is within the limits defined in the specification.

5.2.3 Differential cross point voltage for CK

This chapter is only relevant for DDR4 tests.

5.2.3.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	1
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	1
DUT	DDR4 device that supports the selected type	1

5.2.3.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Differential Signals" > "Differential Cross Point Voltage for CK".

R&S ScopeSuite	——————————————————————————————————————
G Back Session DDR4_4266_20231025_104711	C Show Report D About P Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Electrical Tests	Broke Mede Circle Fridad
Single-Ended Measurements	
Differential Measurements	CK Ch1 -
AC & DC Input Levels for CK (8.3.2)	Thrachold Sattings
□ ▼ Input Slew Rate for CK (8.4.1)	
Differential Cross Point Voltage for CK (8.5)	Vdd 1.2 V
VIX(CK)	Vref 0.6 V
AC Input Levels for DQS (8.7.2)	Test Setup
AC Differential Cross Point Voltage for DQS (8.7.4)	lesi Setup
▼ Input Slew Rate for DQS (8.7.5)	Record Length 10 us
Differential AC Output Levels for DQS (9.3)	Clear Scope Internal 📕 Clear
Differential Output Slew Rate for DQS (9.5)	
	Expert Mode
	Export Waveforms
	Enable
	Offling Everytian
Test Checked Test Single	Enable
Ready to run.	

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.3.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.2.3.4 Measurements

The differential cross point voltage for clock measurement consists of one measurement. It tests the limits as defined in section 8.5 of the JESD79-4B(DDR4) specification.

Differential input cross point voltage - VIX(CK)

This test aims to verify that the differential input cross point voltage is within the limits defined in the specification. It is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

5.2.4 AC input levels for DQS

5.2.4.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.2.4.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Differential Signals" > "AC Input Levels for DQS".



- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.4.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

Consider also the soldering guide, see Chapter 2.1, "Test equipment", on page 9.

5.2.4.4 Measurements

The differential AC input levels for strobe measurements consist of up to two measurements. It tests the limits as defined in section 8.7.2 (DDR4)/ 7.2.6 (LPDDR4/ LPDDR4X) of the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4) specifications.

Differential input high AC - V_{IHdiff(Peak)}

This test aims to verify that the AC differential input high is within the limits defined in the specification.

Differential input low AC - VILLdiff(Peak)

This test aims to verify that the AC differential input low is within the limits defined in the specification.

5.2.5 AC differential cross point voltage for DQS

This chapter is only relevant for DDR4 tests.

5.2.5.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.2.5.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Differential Signals" > "AC Differential Cross Point Voltage for DQS".

K&S ScopeSuite	¤ ×
G Back Session DDR4_4266_20231025_104711	Kan Show Report 1 About 1 Help
All	Properties Limit Manager Results Report Config
Timing Tests	Signals
Electrical Tests	
Single-Ended Measurements	Invert
Differential Measurements	DQS La ch2 -
AC & DC Input Levels for CK (8.3.2)	🔽 DQ 🖓 Ch3 🔻
Input Slew Rate for CK (8.4.1)	Threshold Settings
Differential Cross Point Voltage for CK (8.5)	
AC Input Levels for DQS (8.7.2)	Vdd 1.2 V
AC Differential Cross Point Voltage for DQS (8.7.4)	Vref 0.6 V
Vix_DQS_ratio	Vddq 1.2 V
▼ Input Slew Rate for DQS (8.7.5)	Vtt 0.6 V
Differential AC Output Levels for DQS (9.3)	DOC Trianning for Dod divite Seconding
Differential Output Slew Rate for DQS (9.5)	DQS mggering for Read/write Separation
	Separation Method 🗹 Phase 🗌 Amplitude 😝 Advanced
	Threshold Mode Absolute Relative
	Upper Threshold 0.5 V
	Middle Threshold 0 V
	Lower Threshold -0.5 V
	Test Setup
	Preamble Type 🔵 Auto 💿 1TCK 🔵 2TCK
	Record Length 10 us
	Burst Count 10
	Clear Scope Internal 📮 Clear
	Expert Mode
	Export Waveforms
	Enable
-	Offline Execution
Test Checked Test Single	Enable

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.5.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

5.2.5.4 Measurements

The differential cross point voltage for strobe measurement consists of one measurement. It tests the limits as defined in section 8.7.4 of the JESD79-4B(DDR4) specification.

Differential input cross point voltage - V_{DQSmid_to_Vcent}

This test aims to verify that the differential input cross point voltage is within the limits defined in the specification. It is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

5.2.6 Input slew rate for DQS

5.2.6.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.2.6.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- 2. Select "Electrical Tests" > "Differential Signals" > "Input Slew Rate for DQS".

R&S ScopeSi	uite	¤ ×
🕒 Back	Session DDR4_4266_20231025_104711	Ro Show Report 1 About 1 Help
	All	Properties Limit Manager Results Report Config
	▼ Timing Tests	Signals
	▲ Electrical Tests	Invert
	 Single-Ended Measurements 	DQS Ch2 V
	Differential Measurements	DQ 🖓 Ch3 🔻
	 AC & DC Input Levels for CK (8.3.2) 	Threshold Settings
	 Input Slew Rate for CK (8.4.1) 	
	 Differential Cross Point Voltage for CK (8.5) 	vuu 1.2 V
	 AC Input Levels for DQS (8.7.2) 	Vref 0.6 V
	 AC Differential Cross Point Voltage for DQS (8.7.4) 	DQS Triggering for Read/Write Separation
	 Input Slew Rate for DQS (8.7.5) 	
	SRIdiff Rising	Separation Method 🗹 Phase 🗌 Amplitude 📮 Advanced
	SRIdiff Falling	Threshold Mode Absolute Relative
	 Differential AC Output Levels for DQS (9.3) 	Upper Threshold 0.5 V
	 Differential Output Slew Rate for DQS (9.5) 	Middle Threshold 0 V
		Lower Threshold -0.5 V
		Test Setup
		Preamble Type 🔿 Auto 💿 1TCK 🚫 2TCK
		Record Length 10 us
		Burst Count 10 💌
		Clear Scope Internal
		Expert Mode
		Export Waveforms
		Enable
Test Ch	necked Fast Single	Offline Execution

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.6.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

5.2.6.4 Measurements

The differential input slew rates for strobe measurements consist of up to two measurements. It tests the limits as defined in sections 8.7.5 (DDR4)/ 7.2.9(LPDDR4/ LPDDR4X) of the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4) specifications.

Differential input slew rate rising - SR(diff) rising

This test aims to verify that the setup slew rate for rising signal is within the limits defined in the specification.

Differential input slew rate falling - SR(diff) falling

This test aims to verify that the setup slew rate for falling signal is within the limits defined in the specification.

5.2.7 Differential AC output levels for DQS

5.2.7.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.2.7.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Differential Signals" > "Differential AC Output Levels for DQS".

R&S Sco	peSuite	×
🕒 Ba	ck Session DDR4_4266_20231025_104711	Ra Show Report 1 About 1 Help
	▲ All	Properties Limit Manager Results Report Config
	▼ Timing Tests	Signals
	▲ Electrical Tests	Invert
	 Single-Ended Measurements 	DQS Ch2 V
	Differential Measurements	DQ Ch3 -
	▼ AC & DC Input Levels for CK (8.3.2)	Threshold Settings
	▼ Input Slew Rate for CK (8.4.1)	
	 Differential Cross Point Voltage for CK (8.5) 	Vddq 1.2 V
	✓ AC Input Levels for DQS (8.7.2)	Vtt 0.6 V
	 AC Differential Cross Point Voltage for DQS (8.7.4) 	DQS Triggering for Read/Write Separation
	 Input Slew Rate for DQS (8.7.5) 	
	 Differential AC Output Levels for DQS (9.3) 	Separation Method 🗹 Phase 🔄 Amplitude 📑 Advanced
✓	VOHdiff(AC)	Threshold Mode Absolute Relative
✓	VOLdiff(AC)	Upper Threshold 0.5 V
	 Differential Output Slew Rate for DQS (9.5) 	Middle Threshold 0 V
		Lower Threshold -0.5 V
		Test Setup
		Preamble Type 🔿 Auto 💿 1TCK 🔷 2TCK
		Record Length 10 us
		Burst Count 10 💌
		Clear Scope Internal
		Expert Mode
		Export Waveforms
		Enable
🖌 Tes	st Checked Fast Single	Offline Execution

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.7.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

5.2.7.4 Measurements

The differential AC output levels for strobe measurements consist of up to two measurements. It tests the limits as defined in section 9.3 of the JESD79-4B(DDR4) specification.

V_{OHdiff(AC)}

This test aims to verify that the AC differential output high measurement level for the output slew rate is within the limits defined in the specification.

V_{OLdiff(AC)}

This test aims to verify that the AC differential output low measurement level for the output slew rate is within the limits defined in the specification.

5.2.8 Differential output slew rate for DQS

5.2.8.1 Test equipment

Item	Description, model	Quantity
Rohde & Schwarz oscilloscope	R&S RTP with 4 channels and minimum 8 GHz band- width	1
Modular probe	Probe with minimum 9 GHz bandwidth	2
Probe tip	R&S RT-ZMA10 or R&S RT-ZMA14	2
DUT	DDR4 device that supports the selected type	1

5.2.8.2 Performing the tests

- 1. Start the test as described in Chapter 3.5, "Starting DDR4 tests", on page 26.
- Select "Electrical Tests" > "Differential Signals" > "Differential Output Slew Rate for DQS".

R&S ScopeSuite	×
Back Session DDR4_4266_20231025_104711	R Show Report 1 About 1 Help
All	Properties Limit Manager Results Report Config
	Signals
Electrical Tests	Invert
Single-Ended Measurements	DQS Ch2 V
Differential Measurements	DQ 🖓 Ch3 🔻
	Threshold Settings
Input Slew Rate for CK (8.4.1)	
➡ Differential Cross Point Voltage for CK (8.5)	Vadq 1.2 V
	Vtt 0.6 V
■ AC Differential Cross Point Voltage for DQS (8.7.4)	DQS Triggering for Read/Write Separation
□ Input Slew Rate for DQS (8.7.5)	
Differential AC Output Levels for DQS (9.3)	Separation Method 🗹 Phase 🗌 Amplitude 📕 Advanced
Differential Output Slew Rate for DQS (9.5)	Threshold Mode Absolute Relative
SRQdiff Rising	Upper Threshold 0.5 V
SRQdiff Falling	Middle Threshold 0 V
	Lower Threshold -0.5 V
	Test Setup
	Preamble Type 🔵 Auto 💿 1TCK 🔵 2TCK
	Record Length 10 us
	Burst Count 10 💌
	Clear Scope Internal 📮 Clear
	Expert Mode
	Export Waveforms
	Enable
Test Checked Test Single	Offline Execution

- 3. Enable the tests that you want to run.
- 4. Click "Test Single".
- Follow the instructions of the step-by step guide.
 When you have finished all steps, the compliance test runs automatically.
- 6. You can also run the test in offline mode, using downloaded waveforms. For details, see "Offline Execution" on page 24.

5.2.8.3 Test setup

The software guides you to make the proper connections. Follow the steps to conduct the test.

The software is intended to facilitate the execution of a set of measurements on the relevant signals.

5.2.8.4 Measurements

The differential output slew rate for strobe consists of up to two measurements. It tests the limits as defined in section 9.5 (DDR4) / 7.2.9 (LPDDR4) / 4.3 (LPDDR4X) of the JESD79-4B(DDR4)/ JESD209-4B(LPDDR4)/JESD209-4-1(LPDDR4X) specifications.

Slew rate query output differential signals rising- SRQdiff rising

This test aims to verify that the differential output slew rate for rising edge is within the limits defined in the specification. It is measured from VOLdiff(AC) to VOHdiff(AC).

Slew rate query output differential signals falling - SRQdiff falling

This test aims to verify that the differential output slew rate for falling edge is within the limits defined in the specification. It is measured from VOHdiff(AC) to VOLdiff(AC).