

DDR5/LPDDR5 INTERFACES

Oscilloscope test software for systems with DDR5 or LPDDR5 DRAM memories



Application Brochure
Version 01.00

ROHDE & SCHWARZ

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With the Rohde & Schwarz DDR5/ LPDDR5 test solutions, you can quickly and reliably identify and debug signal integrity issues, verify compliance with JEDEC standards and optimize your design for improved performance and reliability. The R&S®RTP-K94 DDR5 and R&S®RTP-K95 LPDDR5 oscilloscope options offer a wide range of test capabilities from signal integrity analysis to compliance testing.

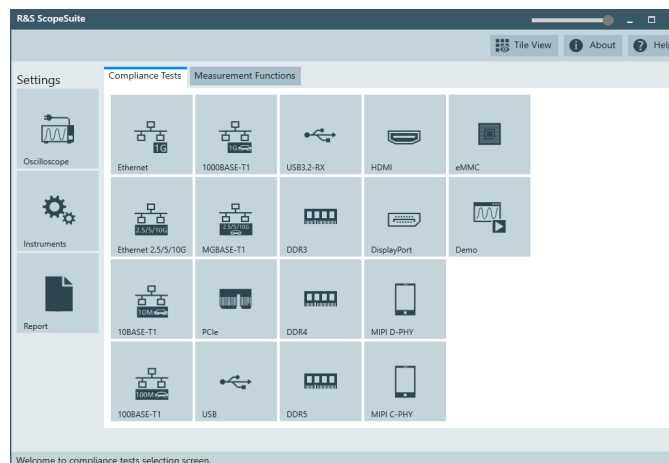
When used for debugging or key performance parameter analysis, based on decoding results, the eye function can filter for READ and WRITE burst. The powerful zone trigger helps focus on dedicated signal details. For system testing in line with the JEDEC standards, the R&S®ScopeSuite helps with automated compliance tests. A test wizard guides the user through the compliance test flow with illustrated step-by-step instructions. Finally, a configurable test report documents the test results.

Key facts

- ▶ Automated compliance testing for DDR5 and LPDDR5 in line with JESD79-5B and JESD209-5C
- ▶ Step-by-step wizard guidance
- ▶ Clear and comprehensive test documentation
- ▶ Signal integrity debugging with data eye view
- ▶ Decoding of READ and WRITE cycles
- ▶ Powerful zone trigger to focus on dedicated signal sequences

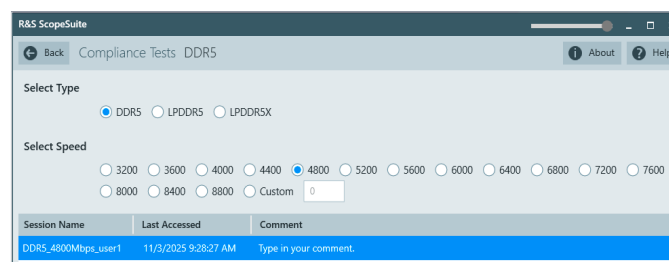
R&S®ScopeSuite overview

R&S®ScopeSuite streamlines automation for various digital interface standards, including JEDEC specified DDR and LPDDR SDRAM memory interfaces. The DDR5 and LPDDR5 test solutions encompass all pertinent test cases. For ease of reference, the software's intuitive homepage conveniently lists all supported and readily available standards.



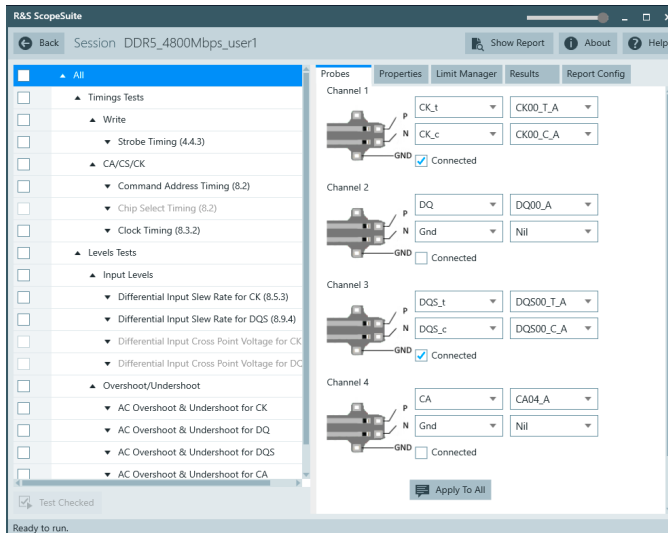
R&S®ScopeSuite compliance test framework

R&S®ScopeSuite software completely controls the connected R&S®RTP high-performance oscilloscope for seamless compliance testing and precise measurements in line with the JEDEC standards. The individual test sessions depend on the selected DDR5 memory type and the respective speed.



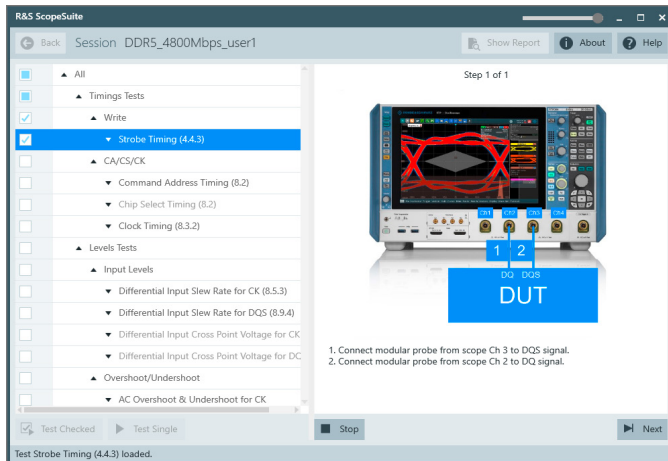
DDR5 compliance test: type and speed selection

The test tree of a test session lists the selectable tests based on the available signals defined in the probe configuration.



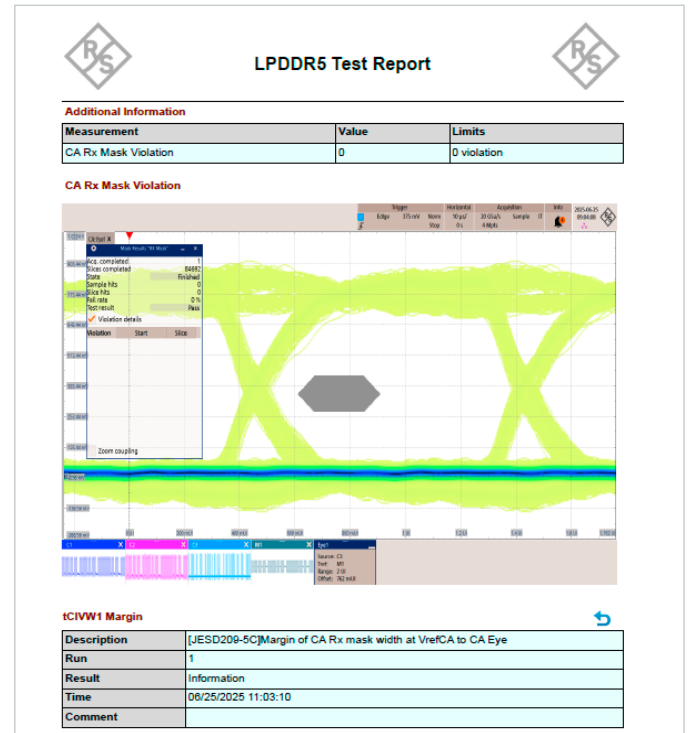
DDR5 test session with test tree and probe configuration

Detailed, image based instructions let users effortlessly and correctly configure setups with an oscilloscope, its accompanying probes, the designated test fixtures and the device under test. This user-friendly approach significantly minimizes the likelihood of setup-related errors.



R&S®ScopeSuite: illustrated step-by-step guidance

All test results are fully documented in a PDF, HTML or DOC report. Depending on user preferences, the report can include specific test cases only, numerical results data or instrument screenshots.



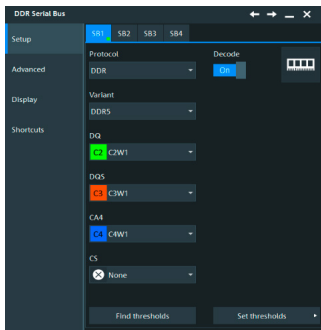
LPDDR5 test report with numerical test results and a screenshot of the worst-case waveform

Debugging methods and options

In addition to the compliance tests, DDR5/LPDDR5 options also include READ/WRITE decoding and data eye functions.

READ/WRITE decoding

The Rohde&Schwarz protocol decoding function offers READ/WRITE decoding for DDR memory interfaces. For DDR5, the CL/CWL READ/WRITE latency parameters from the CA4 signal and the preamble and postamble on the DQS signal are used to achieve reliable READ/WRITE separation. For LPDDR5, the RDQS signal is the key enabler to detect the WRITE cycles.



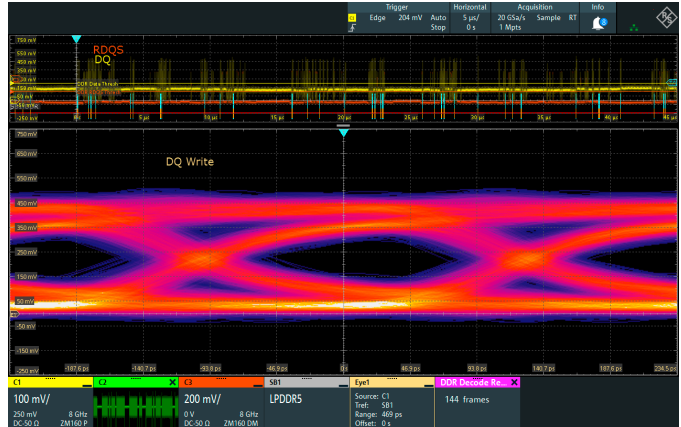
DDR5 READ/WRITE decoding: setup dialog



DDR5 READ/WRITE decoding: decoding results

Data eye

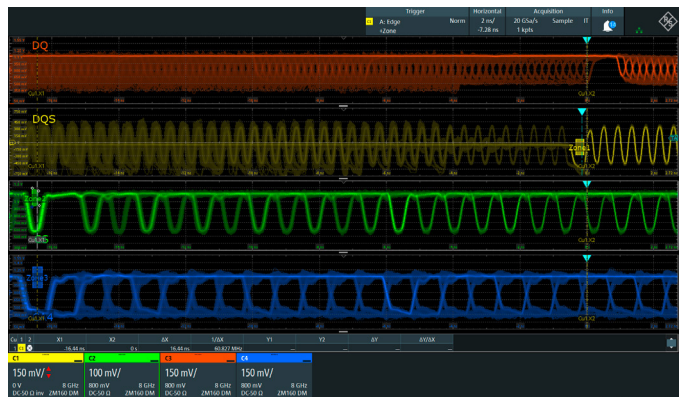
The Rohde&Schwarz oscilloscopes' eye diagram tool can utilize the READ/WRITE decoding to filter dedicated READ and WRITE sequences. All additional tools and functions such as mask testing, histogram and automated eye measurements can be applied for further analysis.



LPDDR5 data eye based on DDR protocol and WRITE filter

Powerful debugging with zone trigger

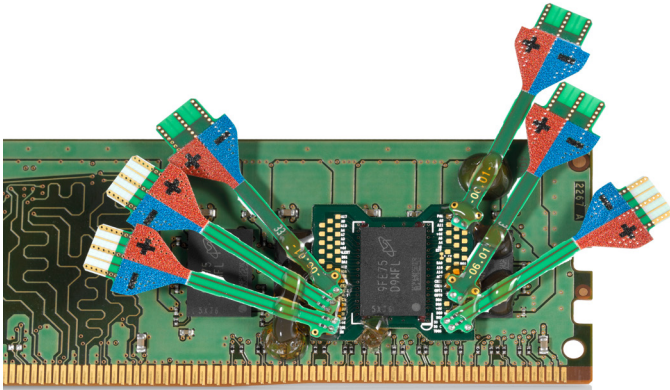
With the R&S®RTP-K19 zone trigger option, users can mark areas on the diagram where waveforms must intersect or exclude a certain area in order to trigger. This helps focus waveform acquisition on dedicated READ or WRITE cycles or to investigate detailed device characteristics such as WRITE CL or detect signal faults.



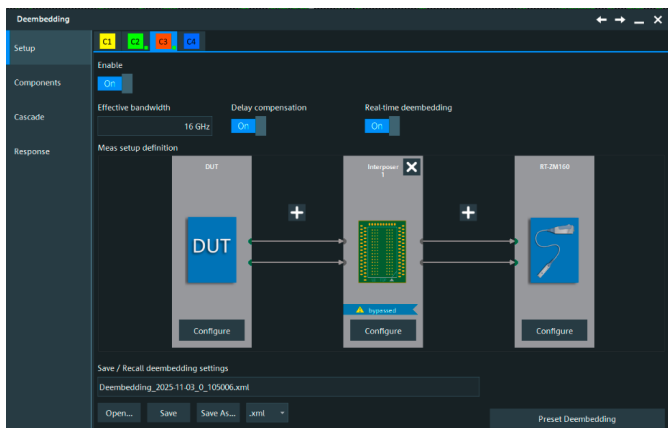
Zone trigger on DQS WRITE burst and CA4 for CWL evaluation

Deembedding interposer

To contact the DDR memory interface signals with probes may require an interposer placed between the PCB and the memory device. The R&S®RTP-K121 deembedding option can import s2p or s3p and s4p or s6p to calculate a correction filter, in order to compensate for the transmission loss of the interposer.



DDR5 DIMM with interposer and R&S®RT-ZMA14 solder-in probe tips



Deembedding setup dialog with interposer and probe

Specifications

	DDR5 (R&S®RTP-K94 option)	LPDDR5 (R&S®RTP-K95 option)
Compliance tests		
	JESD79-5B v1.20	JESD209-5C
Timing tests	strobe timing (4.4.3)	diff clock timing (15.1)
	command address timing (8.2)	single-ended clock timing (12.6)
	clock timing (8.3.2)	diff write clock timing (15.2)
		single-ended write clock timing (12.5)
		WCK to CK phase offset (4.2.5)
Level tests	diff input voltage CK (8.5.2.)	diff input peak voltage CK (12.2.1)
	diff input voltage DQS (8.9.3.)	diff input peak voltage WCK (12.2.2)
	diff input slew rate CK (8.5.3.)	diff input voltage CK (12.2.2.3)
	diff input slew DQS (8.9.4.)	diff input voltage WCK (12.2.1.3)
	diff input cross point CK (8.4.)	diff input slew rate CK (12.2.1.3)
	diff input cross point DQS (8.8.)	diff input slew rate WCK (12.2.2.3)
	diff AC output levels DQS (9.7)	
	diff output slew rate DQS (9.8.)	
Overshoot/undershoot	AC over- and undershoot CK	AC over- and undershoot CK
		AC over- and undershoot WCK
		AC over- and undershoot DQ
		AC over- and undershoot CA
		AC over- and undershoot CS
Single-ended voltage		single-ended input voltage CK
		single-ended input voltage WCK
Protocol decoding		
	READ/WRITE decoding	WRITE decoding
	DQ, DQS, CA4, CS signals	DQ, WCLK, RDQS signals
	based on CL/CWL and preamble	based on RDQS
Eye diagram		
	up to 4	
	timing reference based on parallel channel and DDR protocol	
	READ/WRITE filter based on decoding	WRITE filter based on decoding
	eye stripe function to align mask violations to signal waveform	

Ordering information

Recommended configuration			
	Product	DDR5	LPDDR5
Oscilloscope, 16 GHz bandwidth	R&S®RTP164B	1	1
Probe amplifier module, 16 GHz	R&S®RT-ZM160	2	2
Probe amplifier module, 8 GHz	R&S®RT-ZM90	2	2
Flex connect solder-in probe tip module, up to 16 GHz for R&S®RT-ZM probe amplifier module or Solder-in probe tip module, up to 16 GHz	R&S®RT-ZMA14 R&S®RT-ZMA10	4	4
Signal integrity debugging and compliance test		R&S®RTP-K94	R&S®RTP-K95
Options			
Zone trigger	R&S®RTP-K19	1	1
Deembedding, for interposer compensation	R&S®RTP-K121	1	1
Embedding and equalization, for DFE emulation	R&S®RTP-K126	1	1
Jitter decomposition or Jitter and noise decomposition	R&S®RTP-K133 or R&S®RTP-K134	1	1
Power rail probe, 2.0 GHz or Power rail probe, 4.0 GHz	R&S®RT-ZPR20 or R&S®RT-ZPR40	1	1
Interposer	order from Nexus Technologies or EyeKnowHow	1	1

RELATED SOLUTIONS

ADVANCED PROBING IN DDR3/DDR4 MEMORY DESIGNS

Step-by-step guide
Version 01.00

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ZONE TRIGGER FOR DDR READ/WRITE SEPARATION

Debugging and verifying the DDR DRAM memory interface in a system design can be challenging. The R&S®RTP high-performance oscilloscope zone trigger is ideal for READ/WRITE separation as a basis for analyzing signal integrity.



R&S®RTP high-performance oscilloscope with high-speed modular probes connected to the DDR memory interface for signal integrity debugging and verification

Your task
Integrating a DDR memory interface gets harder as data rates and design density increase. Developers must maintain appropriate signal integrity for a reliable data exchange between the controller and the DDR DRAM memory.

An oscilloscope is important when verifying signal integrity and identifying error sources. Data (DQ) and data strobe (DQS) signals work bidirectionally, making them a real challenge. Differentiating between READ (memory sends data to processor) and WRITE (processor sends data to the memory) bursts for DQ and DQS signals is difficult. Signal integrity analysis demands seamless processing of READ/WRITE signals.

Rohde & Schwarz solution

Example configuration
In this example, a PC system uses DDR4 DRAM DIMM. The data transfer is stimulated with the MemTest86 memory test software. The RANCOM test mode issues a good mix of READ/WRITE bursts.

For testing, high-speed probes are typically soldered to the clock signal and to selected DQ signals with their relevant DQS signals, as well as to command/address signals such as CS.



DDR4 DQ and DQS signals with READ and WRITE bursts. In this example, a read detection between READ/WRITE bursts is possible based on the analysis of RANCOM test mode.

Zone trigger
Rohde & Schwarz oscilloscopes have a zone trigger to define areas on the waveform diagram that MUST or MUST NOT be interacted to trigger a signal acquisition. Such zones can be used to focus signal acquisition on dedicated signal characteristics.

Application Card | Version 01.00

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