

Effective debugging of USB 3.1 and PCIe interfaces



The 6 GHz R&S®RTO oscilloscope measures fast digital interfaces, including USB 3.1 Gen1 and PCIe 2.0, at data rates of up to 5 Gbit/s. This makes it ideal for testing the signal integrity of high-speed data lines as well as for debugging at the protocol level.

Clear trend: integration of fast communications interfaces

Growing data volumes and continually increasing processing and transmission speeds represent major challenges for board designers. The most widely used fast data interfaces are the DDR memory interfaces (DDR2, DDR3 and DDR4, including the low-power variants) and the USB and PCI Express (PCIe) serial communications interfaces.

USB is now used everywhere, with applications ranging from standard PC and consumer electronics to automotive, industrial and medical technology. The USB interface not only offers higher data rates of 5 Gbit/s for the USB 3.1 Gen 1 (SuperSpeed) standard and 10 Gbit/s for the Gen 2 (SuperSpeed+) standard, it also has improved power supply and charging functionality thanks to the USB Power Delivery specification. Another key innovation is the uniform connector. The USB Type-C™ slim plug can be connected in any orientation and is suitable for mobile devices. It features fast data rates, handles up to 100 W (5 A and 20 V power delivery modes) and even supports DisplayPort and Thunderbolt.

The PCIe interface is also enjoying more widespread use. Originally developed for the computer industry, it is now found in many embedded applications for connecting auxiliary devices and components to the CPU or for converting from USB or UART to PCIe. The powerful PCIe 4.0 (Gen 4) is nearly ready for introduction and offers a maximum data rate of 16 GT/s. However, embedded applications are adequately served by the first and second generation interfaces, which operate at 2.5 GT/s and 5 GT/s respectively. Each new interface generation generally supports the operating modes of earlier generations. That is why devices frequently boast Gen 2 or Gen 3 interfaces yet operate at the first generation's maximum data rate of only 2.5 GT/s during dedicated operation and must be tested accordingly.

Challenge: signal integrity

Secure data transmission via a digital serial interface such as USB or PCIe relies on error-free transmission of binary signals in the physical layer. The key components in the transmission chain are the transmitters, transmission line and receivers. Developers must ensure that signals in these components comply with the relevant interface standards.

In practice, the challenge lies primarily in the board design. On the one hand, the signal integrity of the transmission line has to be considered because the plugs, vias and relays, for example, could affect the transmission of signals over PCB lines or cables. On the other hand, the fast data interface must be protected against interference from nearby components. Adjacent signal lines that lie too closely together, for example, could result in crosstalk even though USB and PCIe use differential signaling.

In most cases, transmitters and receivers are standard components whose specifications have been tested by the manufacturer. However, this does not rule out faults in the wiring or problems with the quality and stability of the reference clock or the power supply, which is why these must also be tested during board development.

Using eye diagrams and histograms to ensure signal integrity

Displaying the digital signal in an eye diagram is an effective way of assessing the signal quality. The signal bits are written separately on top of each other and accumulated into a diagram. A typical eye diagram is a result of the many bit transitions from 0 to 1 and 1 to 0 (Fig. 1). A number of quality parameters for a signal transmission can be determined from the diagram. For example, the horizontal axis shows the eye opening over time and the jitter at the sides of the eye (bit transitions) while the vertical axis shows the vertical eye opening and noise.

USB and PCIe interface standards define masks for eye diagram tests that make it easy to assess whether the minimum required eye opening for reliable data transmission is provided. Fig. 2 shows an example from the PCIe CEM Gen 2 specification at a data rate of 2.5 Gbit/s.

Histograms enable circuit designers to identify valuable details about jitter distribution and amplitude noise by observing the bit transitions horizontally and the eye center vertically. An example measurement using the 6 GHz R&S®RTO oscilloscope is shown in Fig. 3. The test signal comes from a PC plug-in board with a PCIe Gen 2 interface (2.5 GT/s mode). The R&S®RTO acquires waveforms much faster than other instruments on the market. It can acquire several million bits

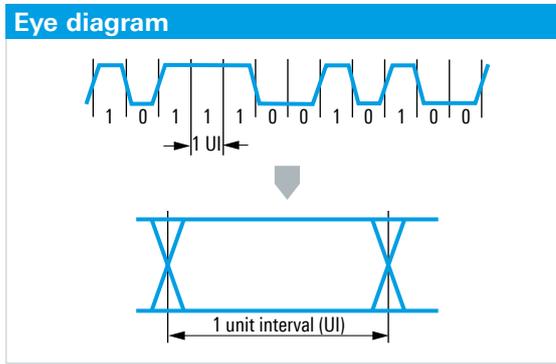


Fig. 1: Eye diagram of a data signal (UI = 1/data rate).

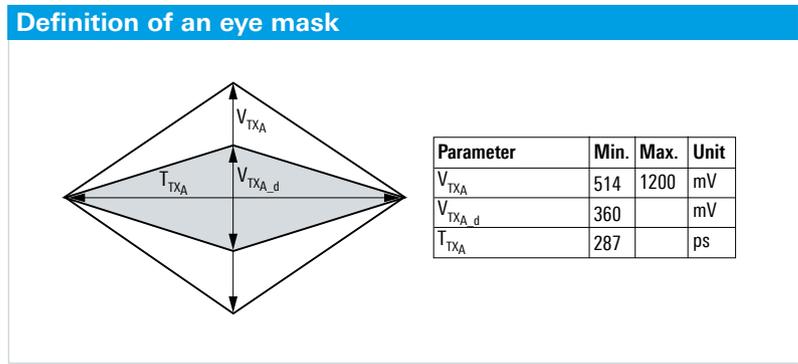


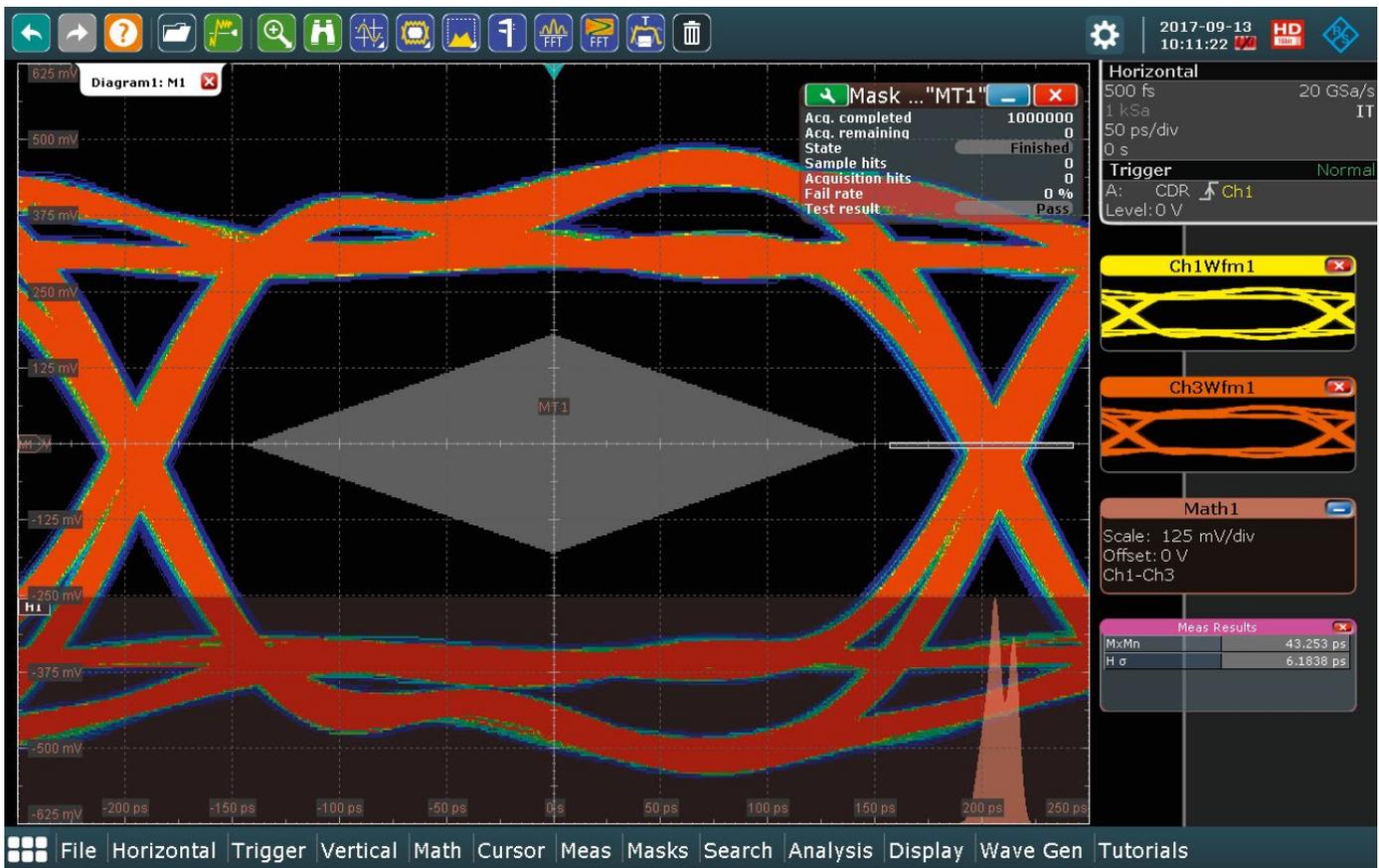
Fig. 2: Eye mask from the PCIe 2.0 specification (2.5 GT/s mode).

within seconds and use them to display the eye diagram. The color coding for persistence makes it possible to see both frequent and rare signal sequences. A mask is positioned at the center of the eye as defined in the PCIe specification. The software acquires violations of the eye pattern and shows details such as the number of acquired waveforms, mask violations and error rates. In the histogram, a Gaussian jitter distribution can be seen on the right edge of the eye. The histogram is also good for other measurements such as peak-to-peak jitter (max.-to-min.) and RMS jitter (standard deviation).

CDR trigger for fast eye diagram tests

A time reference is required in order to correctly overlay the bit sequences for the eye diagram. In addition to transmitting data, parallel data interfaces such as the DDR memory interface also transmit a clock signal that defines the precise start and end times for the transmission of each data bit. Serial data buses such as USB or PCIe embed the reference clock in the data signal. The receiver has to use clock data recovery (CDR) to extract the embedded clock. It then uses the extracted clock signal to sample the incoming data stream.

Fig. 3: Eye diagram of a signal as specified in PCIe Gen 2 (2.5 GT/s), including mask test and histogram; measured with an R&S®RTO2064 oscilloscope.



CDR uses a regulating component such as a phase-locked loop (PLL) or delay-locked loop (DLL) to follow frequency variations – typically less than 1 MHz up to 10 MHz. While this ability to flatten out frequency variations is excellent for stable data transmission, it makes testing more difficult. The traditional approach of using the test instrument’s clock as the reference reduces the test margin and can even make testing impossible. Some standards also use frequency modulation, such as the spread spectrum clocking used by PCIe (~30 kHz triangular modulation), to reduce electrical emissions.

For all of these reasons, it is necessary to take the behavior of the receiver’s CDR into consideration in order to successfully test embedded clock signals. R&S®RTO users are a step ahead here because the oscilloscope uses the R&S®RTO-K13 hardware CDR option to display the eye diagram. Its behavior with respect to PLL order, bandwidth and damping can be configured to test in line with different protocol specifications that describe the receiver’s CDR in detail (Fig. 4). With this hardware CDR option, the clock signal extracted from the CDR is used as the trigger source (Fig. 5), effectively ensuring that the data bits are synchronized with the embedded clock signals. With a UI offset of 0.5, the trigger point in the center of the eye is configurable (Fig. 4).

Thanks to the R&S®RTO oscilloscope’s high acquisition rate of up to 1 million waveforms per second, the hardware CDR can

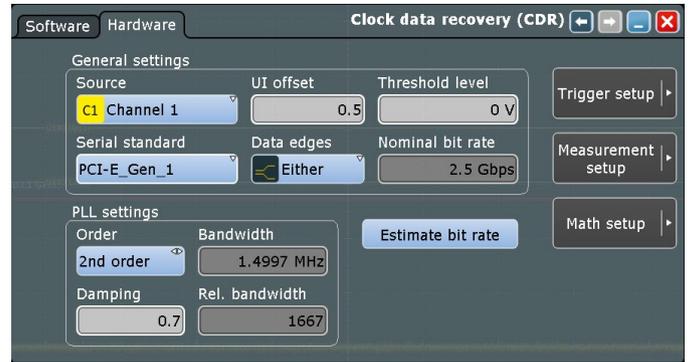


Fig. 4: The R&S®RTO oscilloscope’s configurable hardware CDR.

very quickly overlay a large number of data bits to produce an eye diagram so that the results have a high statistical reliability. Traditional software CDR analysis is performed during postprocessing of the individual waveforms and is therefore more time-consuming. Another advantage of the R&S®RTO solution is that its hardware CDR runs continuously with consistent behavior across all waveform acquisitions. In contrast, the PLL algorithm of a software CDR must restart with each acquisition, rendering the samples at the start of the waveform unusable.

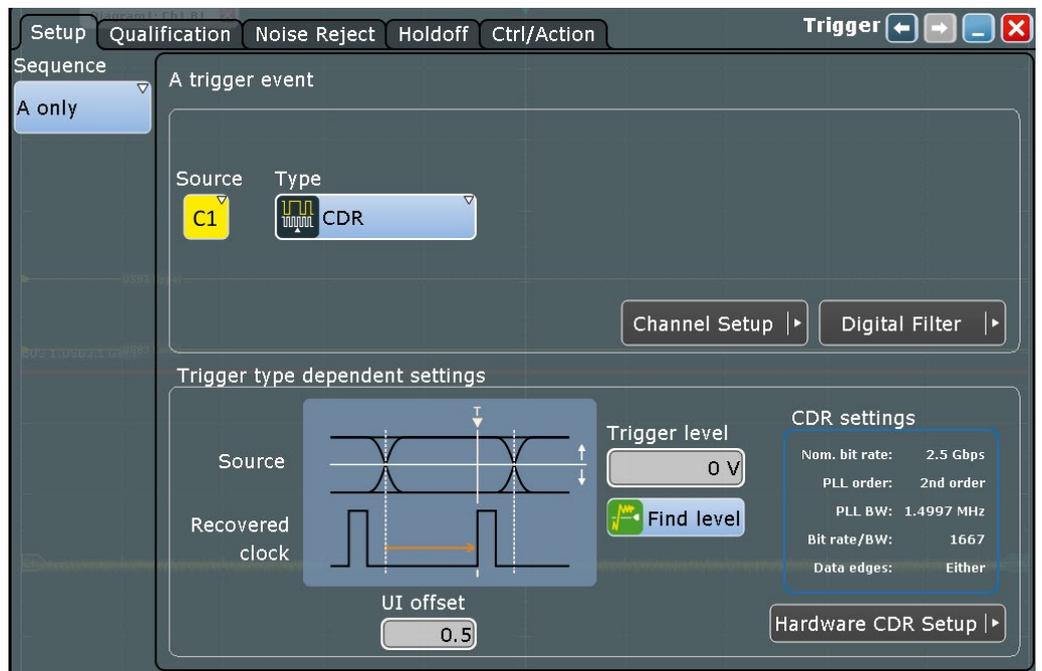


Fig. 5: Selecting the CDR as the trigger source when using the R&S®RTO-K13 hardware CDR option.

Preventing contacting errors

Correct probe contacting is key to obtaining reliable results when measuring fast signals. The modular probes from Rohde&Schwarz, such as the R&S®RT-ZM broadband probe, provide a variety of tip modules to support different contacting methods (Fig. 6). The most common method is to solder-in a tip module (Fig. 7). For all methods, the contacts should be kept as short as possible to minimize additional inductance and capacitance. This also applies for soldered connections; the solder contacts should not exceed two to three millimeters in length.

Fast data interfaces primarily use differential lines for signal transmission. A differential probe is used to tap the two V_P and V_N signals. An additional ground connection is highly recommended to ensure a stable and reliable test environment with minimal parasitic effects and a good common mode rejection ratio (CMRR) [*].

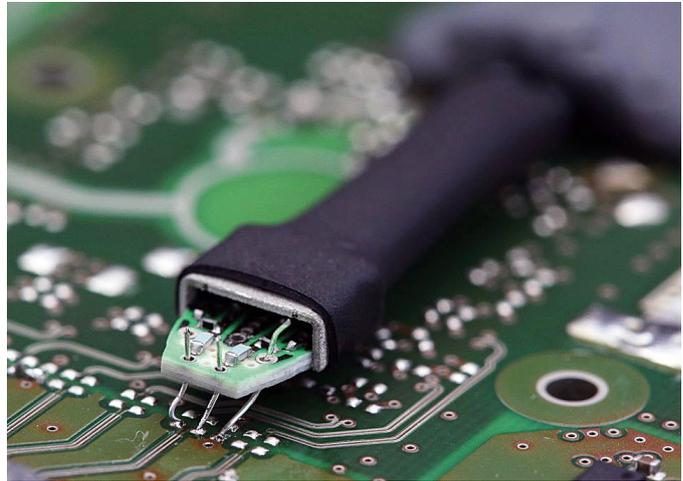
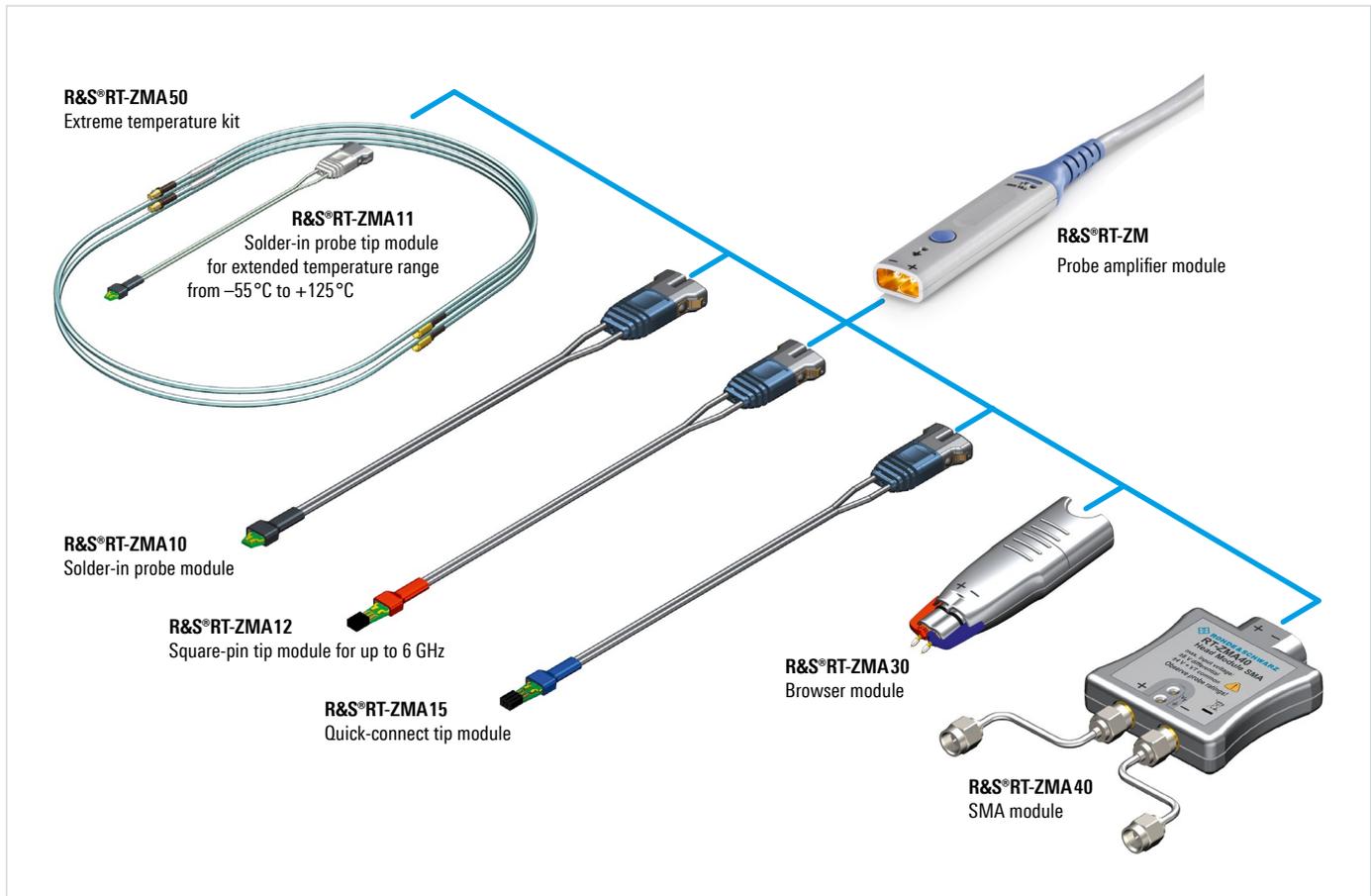


Fig. 7: Using the R&S®RT-ZMA10 solder-in tip module to contact a high-speed interface.

Fig. 6: Selection of tip modules for the R&S®RT-ZM modular broadband probe.



If the R&S®RT-ZM broadband probe is connected to the V_P and V_N signals and also to ground, the oscilloscope's multi-mode functionality allows users to easily switch from a differential measurement to a single-ended measurement at V_P and V_N or to directly measure the common mode voltage without having to change the connection (Fig. 8).

Compliance tests for USB and PCIe

Standardization committees such as the USB Implementers Forum (USB-IF) and PCI-Sig define compliance tests for their data interfaces. For signal integrity measurements, these tests typically require that the oscilloscope bandwidth cover the fifth harmonic of the data signal. In the case of a high-speed USB data signal at a data rate of 480 Mbit/s, for example, a suitable oscilloscope would need a minimum bandwidth of 1.2 GHz (480 Mbit/s is equivalent to 240 MHz, which is multiplied by 5). The R&S®RTO with 6 GHz bandwidth supports compliance tests up to a maximum data rate of 2.5 Gbit/s. For such tests, Rohde&Schwarz offers software options that guide users through the measurements and then output the results in a report (Fig. 9). The R&S®RTO-K24 option is available for USB 2.0. The R&S®RTO-K81 option covers PCIe compliance tests for interface generations 1 and 2 up to a maximum data rate of 2.5 Gbit/s.

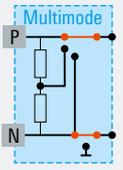
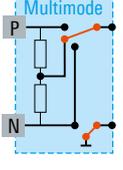
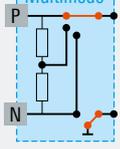
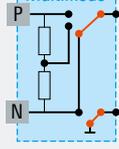
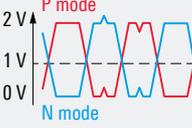
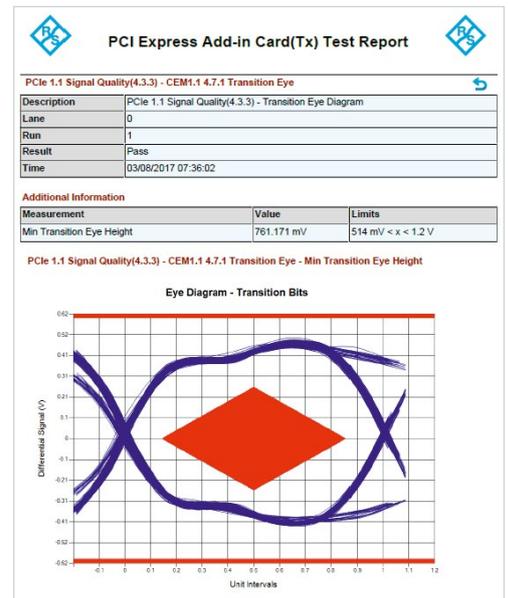
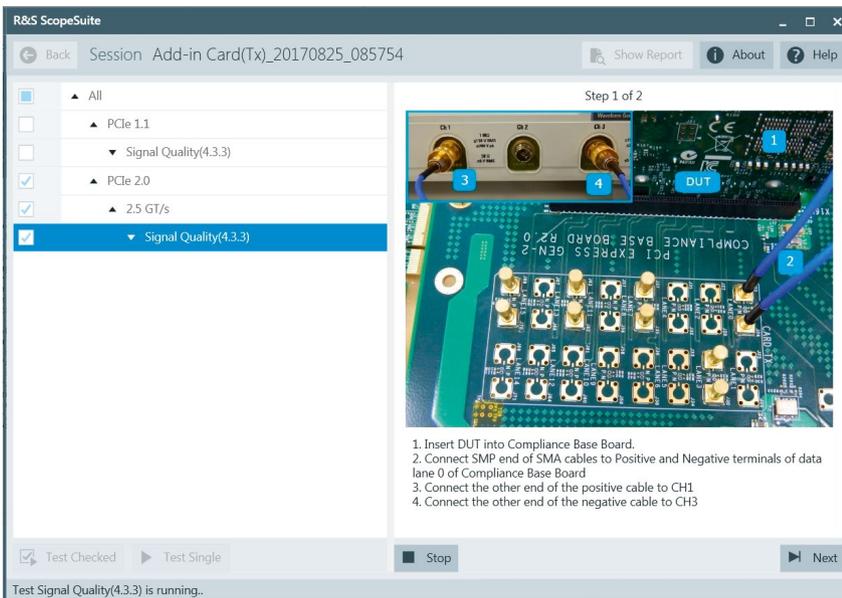
Measurement mode		Description
Differential mode (DM)		Voltage between P pin and N pin: $V_{DM} = V_P - V_N$ 
Common mode (CM)		Average signal voltage between P and N pins and ground: $V_{CM} = \frac{V_P + V_N}{2}$ 
Single-ended mode	<div style="display: flex; justify-content: space-around;"> <div></div> <div></div> </div>	Voltage between P pin or N pin and ground 

Fig. 8: The R&S®RT-ZM broadband probe's multimode configurations.

Fig. 9: Example of a guided PCIe compliance test (left) and the detailed report.



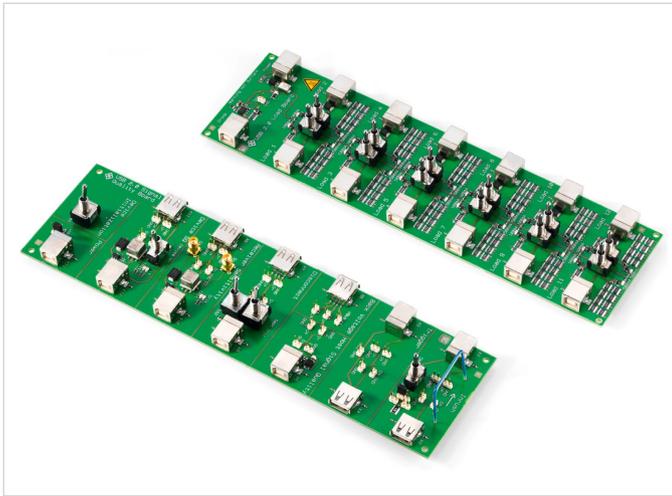


Fig. 10: USB 2.0 test fixture set from Rohde&Schwarz.

During compliance testing, test fixtures are used to contact the DUT. For USB 2.0 tests, Rohde&Schwarz offers the R&S®RT-ZF1 test fixture set (Fig. 10) which supports the various test environments and provides suitable contacting for high-speed and legacy tests for USB devices, hubs and hosts. The high-speed signal quality test additionally requires the “USB 2.0 hi-speed signal quality test fixture” set, which is available only from USB.org.

Certified test fixtures for PCIe are generally available only from the PCISig consortium, both for testing PCIe motherboards (PCI Express compliance load board – CLB) and testing add-in cards (PCI Express compliance base board – CBB). The CLB/CBB test fixtures are available for each PCIe generation. The later generation fixtures support the earlier generations.

Using protocol triggering and decoding to debug during startup

For circuits with USB or PCIe interfaces, it is important to check the signal integrity and analyze the protocol data. Typically, errors often occur when establishing the interface connection between the transmitter and receiver and when receiving faulty data. Serial interfaces such as USB and PCIe run through a handshake procedure when establishing the connection. During this procedure, the two transmission partners report their capabilities regarding data rate, etc. and agree upon suitable transfer functions.

A protocol decoding option for the R&S®RTO oscilloscope allows developers to acquire and assess these sequences in detail. Targeted triggering on individual protocol elements

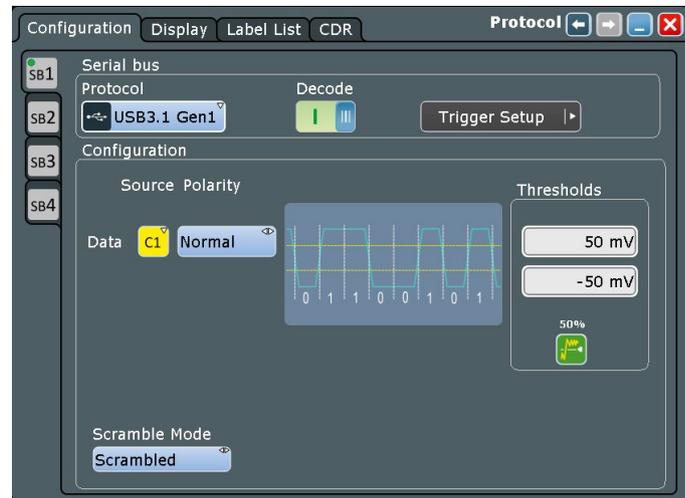


Fig. 11: Configuration dialog when using the R&S®RTO-K61 option to decode USB 3.1 Gen1.

makes it possible to acquire data from other interfaces and function blocks and to analyze their timing.

An example is a protocol analysis of a USB 3.1 Gen1 interface using the R&S®RTO-K61 trigger and decoding option. Fig. 11 illustrates how easy it is to configure the decoding. The user selects the channel and polarity of the differential signal (very important if the signal needs to be inverted because the probe was soldered in backwards) and then simply ensures that the switching thresholds for the logical one and zero lie correctly in the center of the data signal in order to provide reliable decoding results. The software defines the PLL configuration for the CDR based on the relevant USB standard. Using the extracted embedded clock signal as the reference clock, the software defines the bit and word boundaries for each waveform acquisition in order to decode the data.

An example result is shown in Fig. 13. The top of the screenshot shows data bursts with zoomed details. The decoding is shown in the center of the screenshot with zoomed protocol details. The individual protocol elements are color-coded for easier readability. Protocol data can also be listed in a table. Additional protocol details are available for each data frame.

It is also possible to trigger on protocol details. As shown in Fig. 12, the user can select many different protocol elements, including frame start, frame contents and frame errors, as the trigger type. Through targeted triggering on individual protocol elements, data from other interfaces and function blocks can be acquired time-correlated and then analyzed. This is how cross-interference from other functional units such as serial interfaces, analog sensors, radio interfaces, power

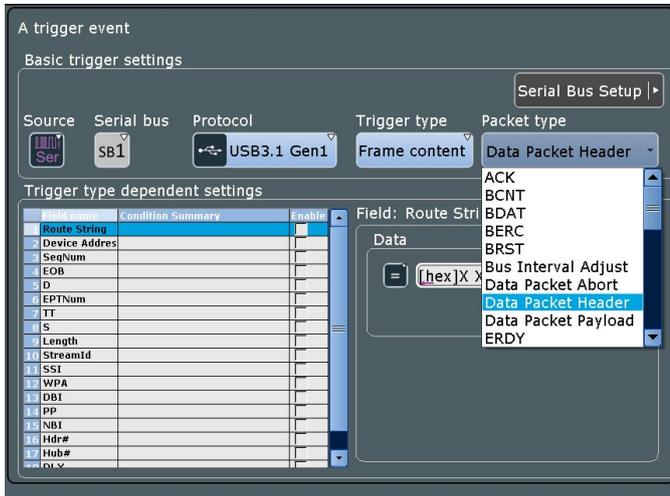


Fig. 12: Configuring the trigger type to be a data packet header in line with USB 3.1 Gen 1.

combined with additional protocol, logic and spectrum analysis functions and even function and pattern generators – all in a single instrument.

Summary

The integration of fast data buses presents new challenges for circuit developers during design and testing. Rohde & Schwarz offers a compact test solution consisting of the 6 GHz R&S®RTO and modular broadband probes to support users when debugging signal integrity problems and analyzing protocol data. The high acquisition rate combined with powerful analysis tools such as mask tests and histograms plus a variety of options such as hardware CDR and protocol triggering/decoding lead to fast results.

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supplies, etc. can be detected in densely packed embedded designs. Rohde & Schwarz oscilloscopes support this type of complex debugging with their multi-domain capability. The oscilloscope's traditional time domain analysis functionality is

References

* Application Card "Optimized differential measurements on high-speed interfaces".

Fig. 13: Example of data decoding in line with USB 3.1 Gen 1.

