



EFFICIENT FILTER CONNECTION

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Senior Field Application Engineer

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT



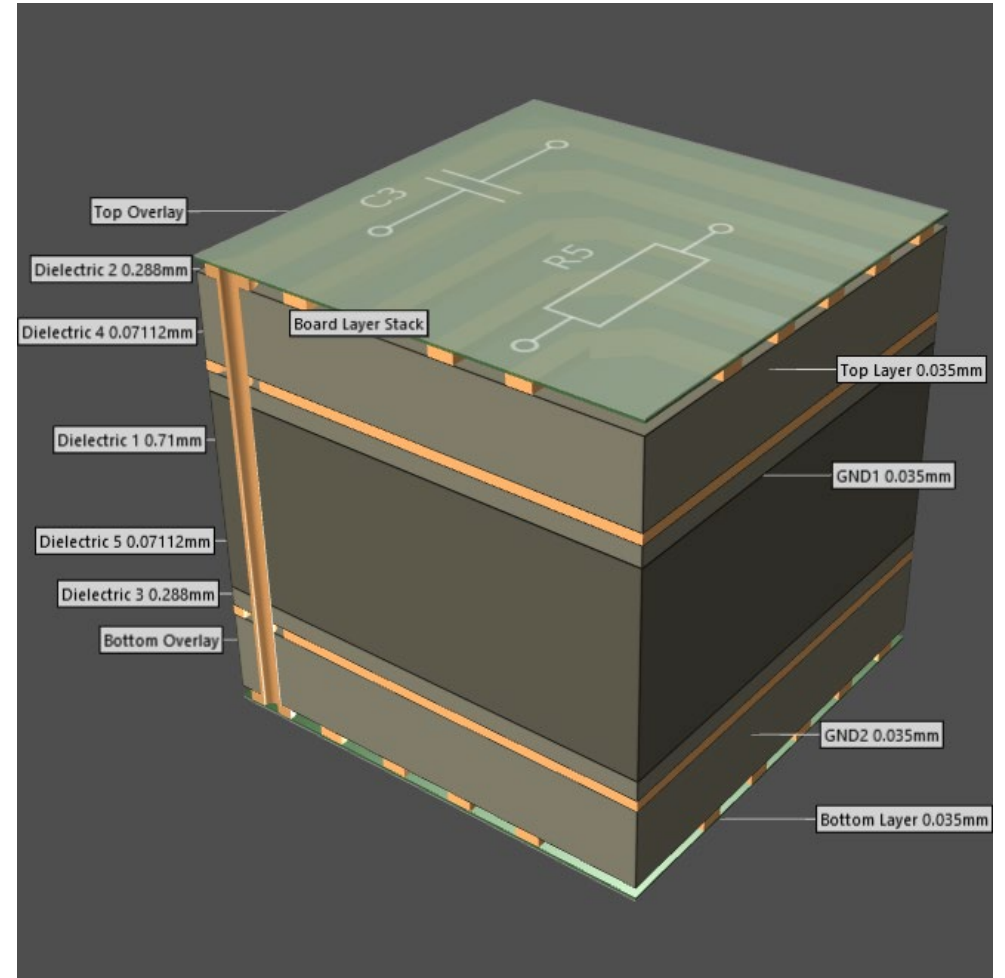
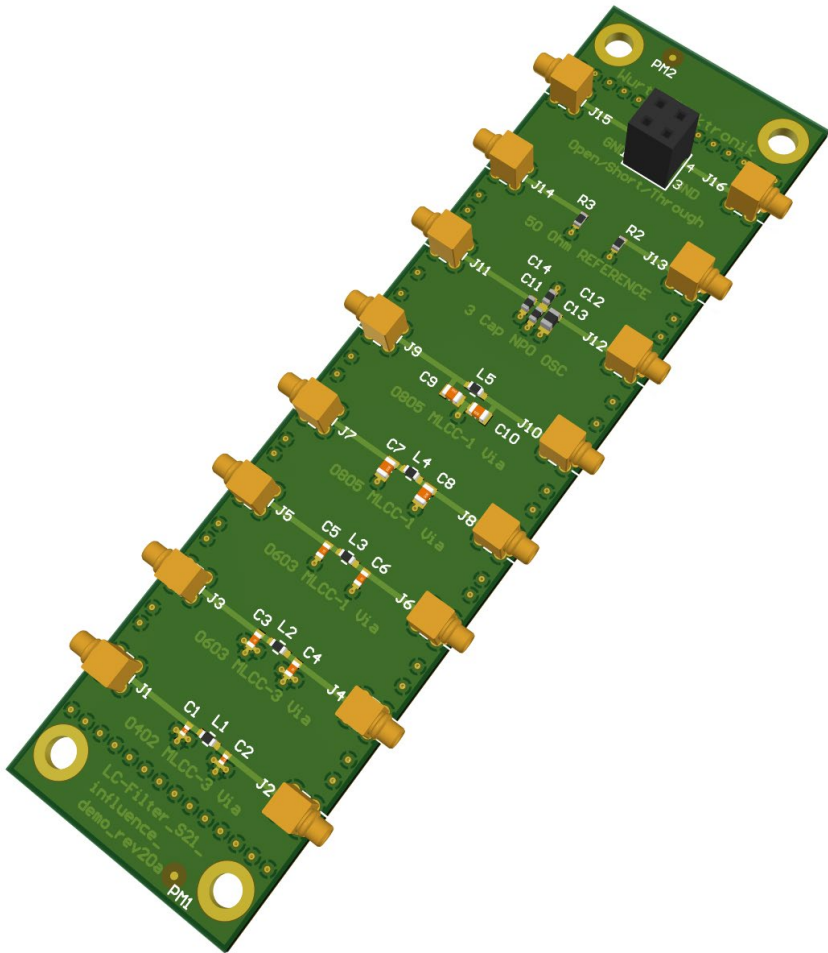
Agenda

- Component parasitics
- Comparison ideal vs. real
- PCB parasitics
- Effects of multiple Vias in relation to their arrangement
- Simulation of real filters with Bias effects and Vias



Overview

PCB and layer stack

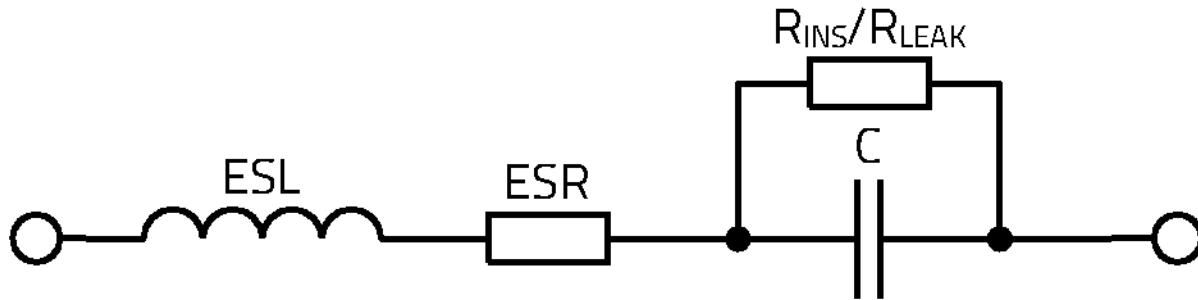


PARASITICS

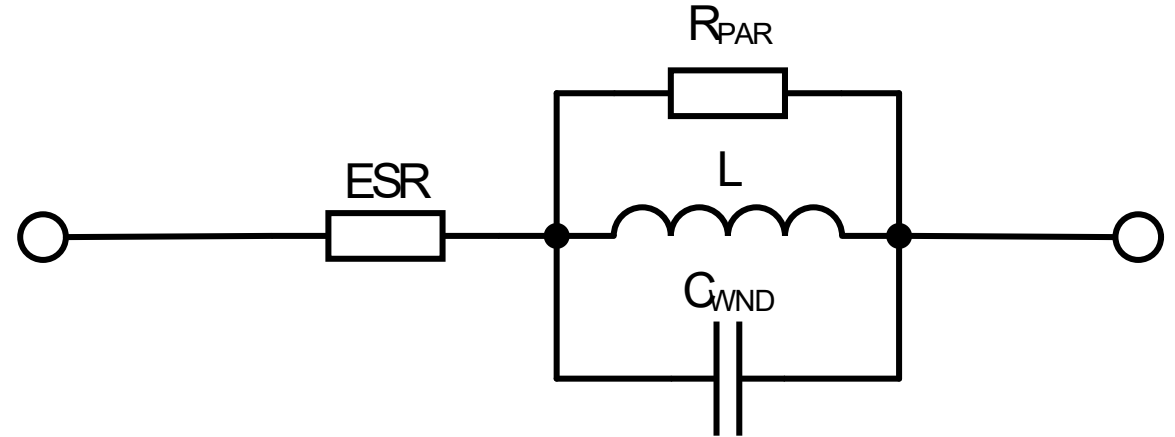


Component parasitics

Capacitor vs. inductor (ferrite)



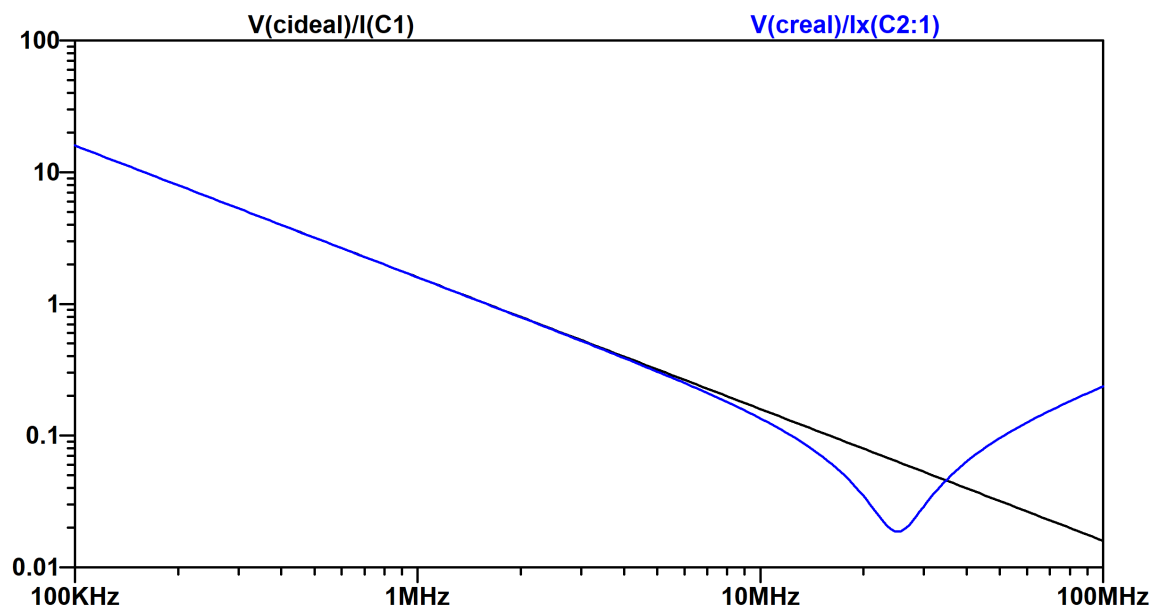
- capacitor
 - ESL
 - ESR
 - R_{LEAK}
 - C



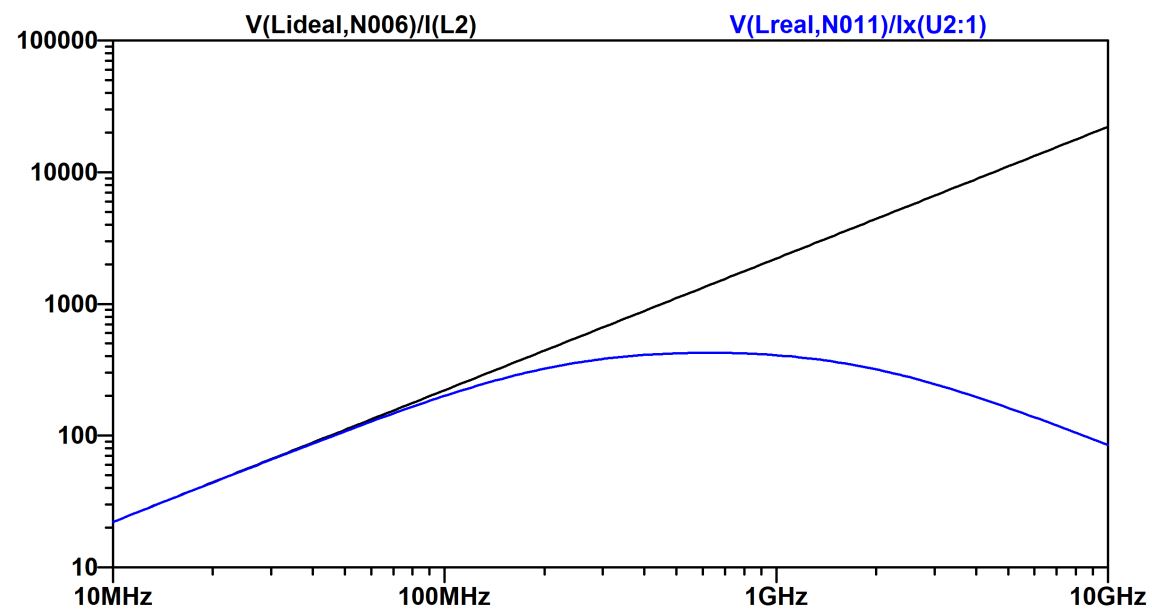
- inductor (ferrite)
 - ESR
 - R_{PAR}
 - C_{WND}
 - L

Comparison Ideal vs. real

Capacitor vs. inductor (ferrite)



ideal vs. real capacitor

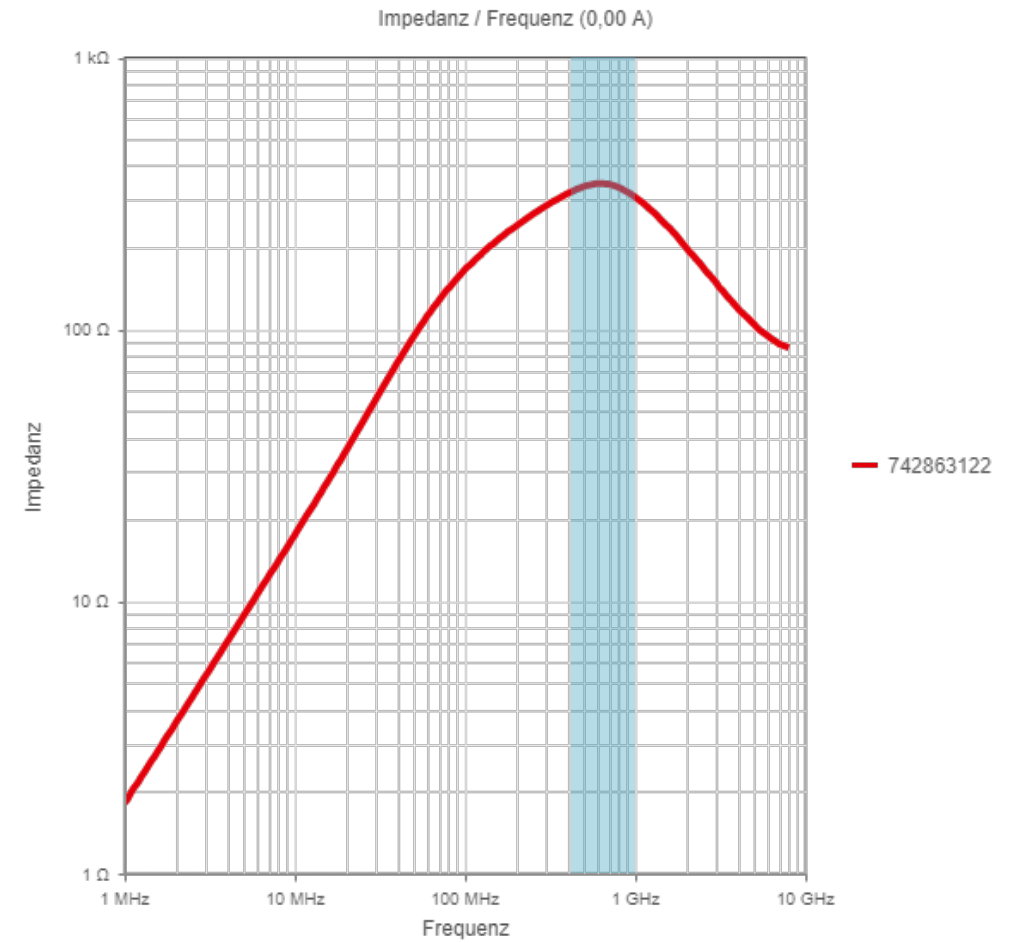
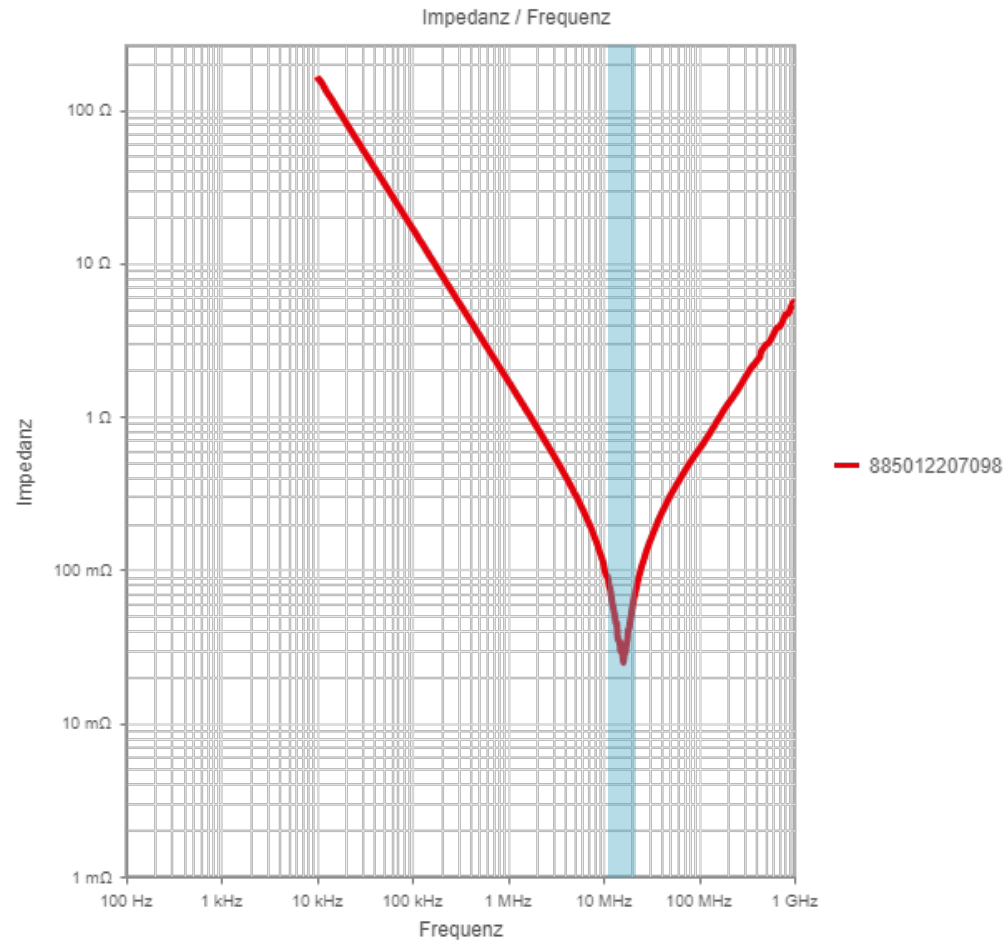


ideal vs. real inductor (ferrite)



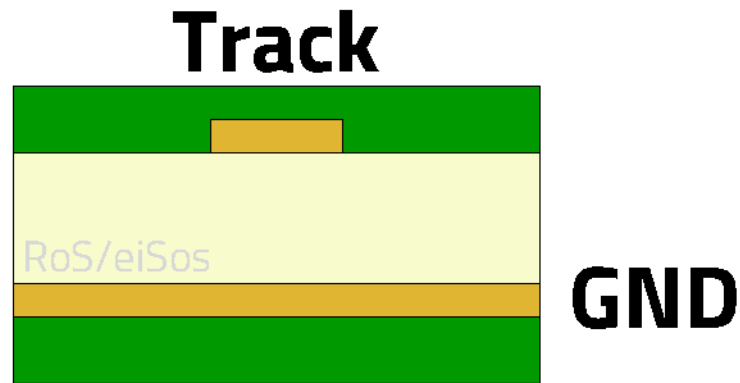
Component parasitics in detail

Capacitor vs. inductor (ferrite)



PCB parasitics

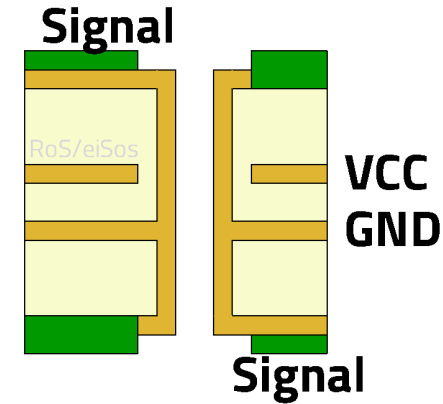
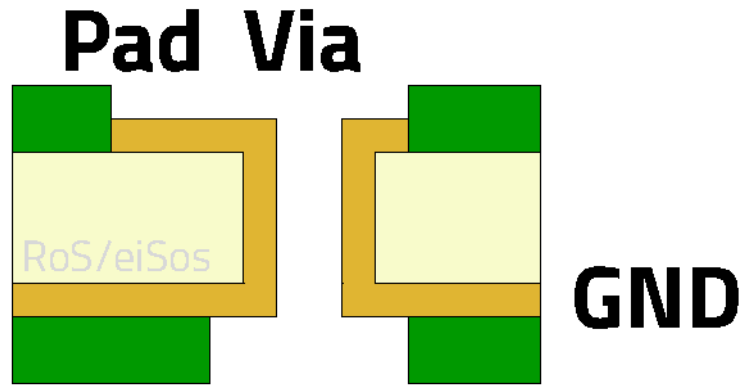
Tracks



w [mm]	h [mm]	ind [nH/mm]	cap [pF/mm]	ϵ_r
0.4	1.6	~0.7	~0.05	4.6
0.2	1.6	~0.8	~0.04	4.6
0.4	0.288	~0.35	~0.1	4.6
0.2	0.288	~0.45	~0.07	4.6

PCB parasitics

Vias

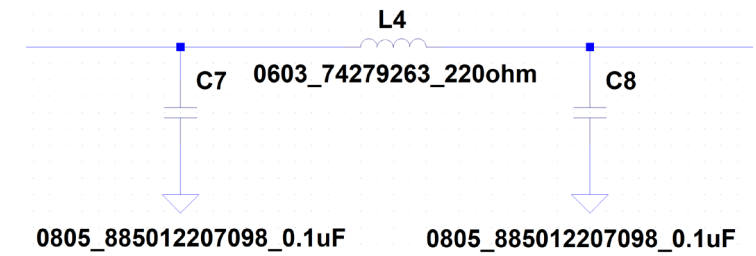


- Via {d=0.3mm; h=1.6mm; 25 μ plating}
 - inductance: 1.3nH
- Via {d=0.3mm; h=0.288mm; 25 μ plating}
 - inductance: 0.14nH

- Via {d=0.3mm; h=1.6mm; 25 μ plating}
 - inductance: 1.3nH
 - capacitance: 0.6pF {Pad=0.6mm; opening=1.0mm; $\epsilon_r=4.6$ }

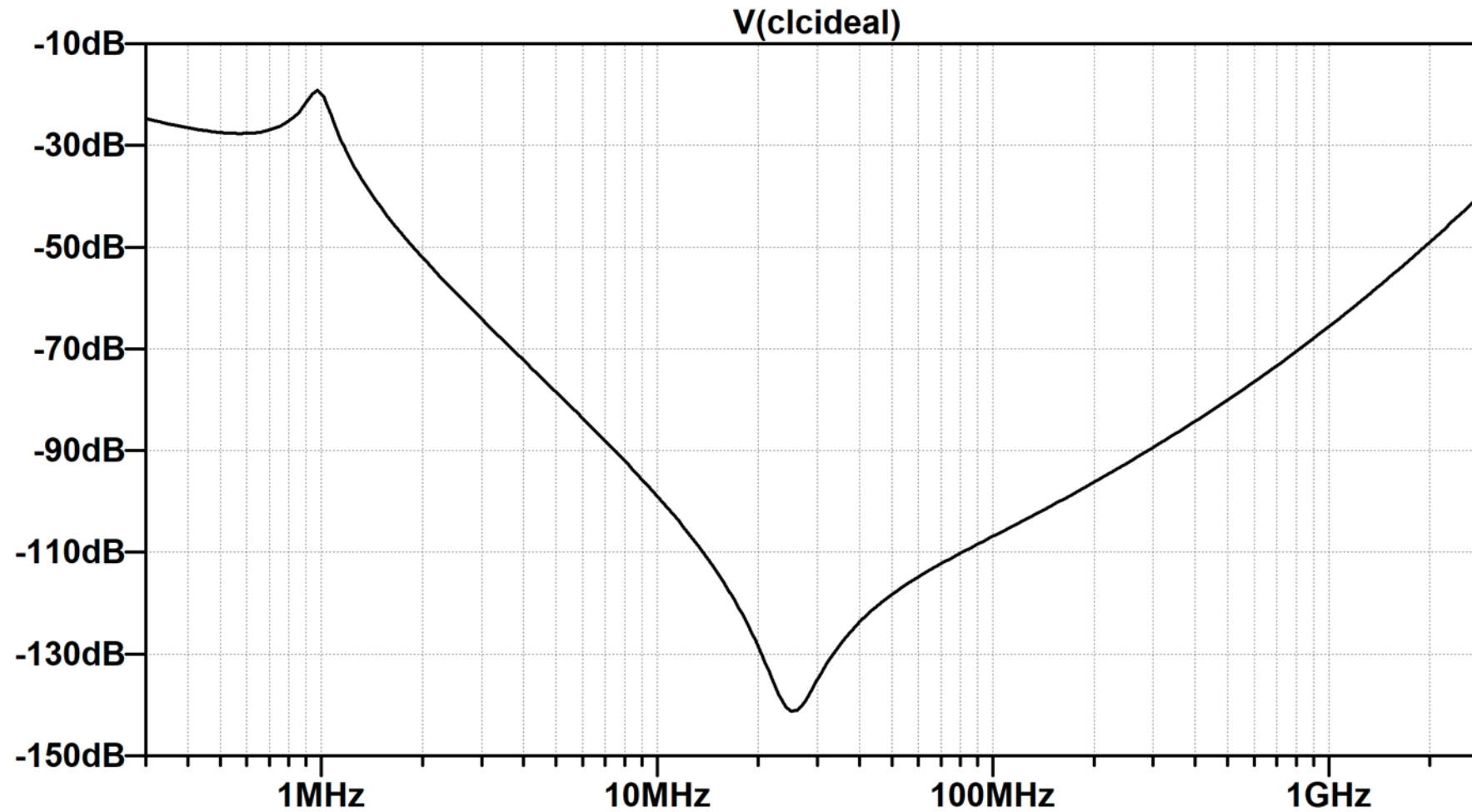
PI filter

Good board realization



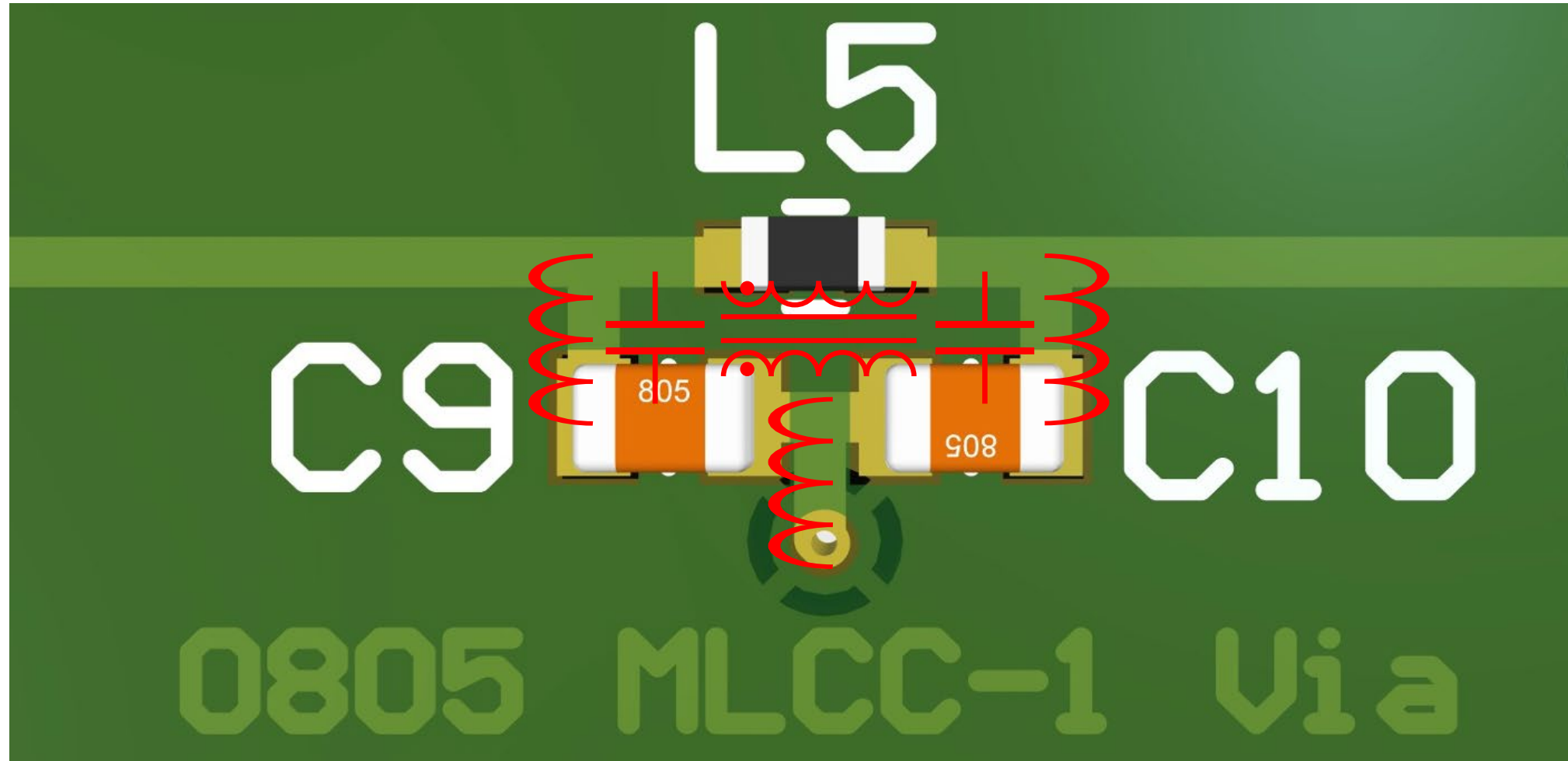
PI filter

Real models **without** layout and placement influence



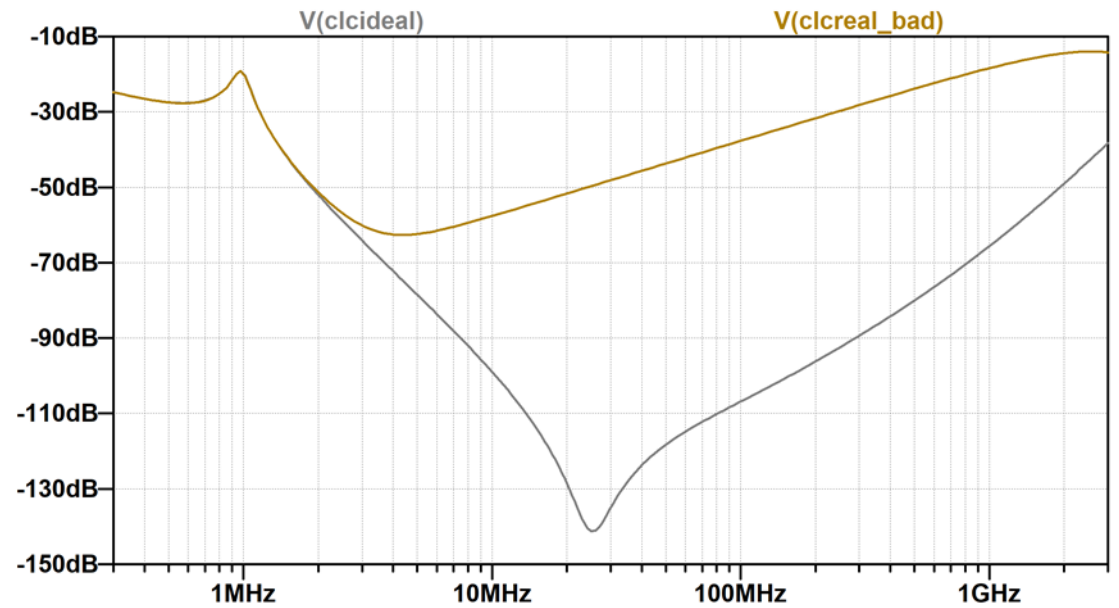
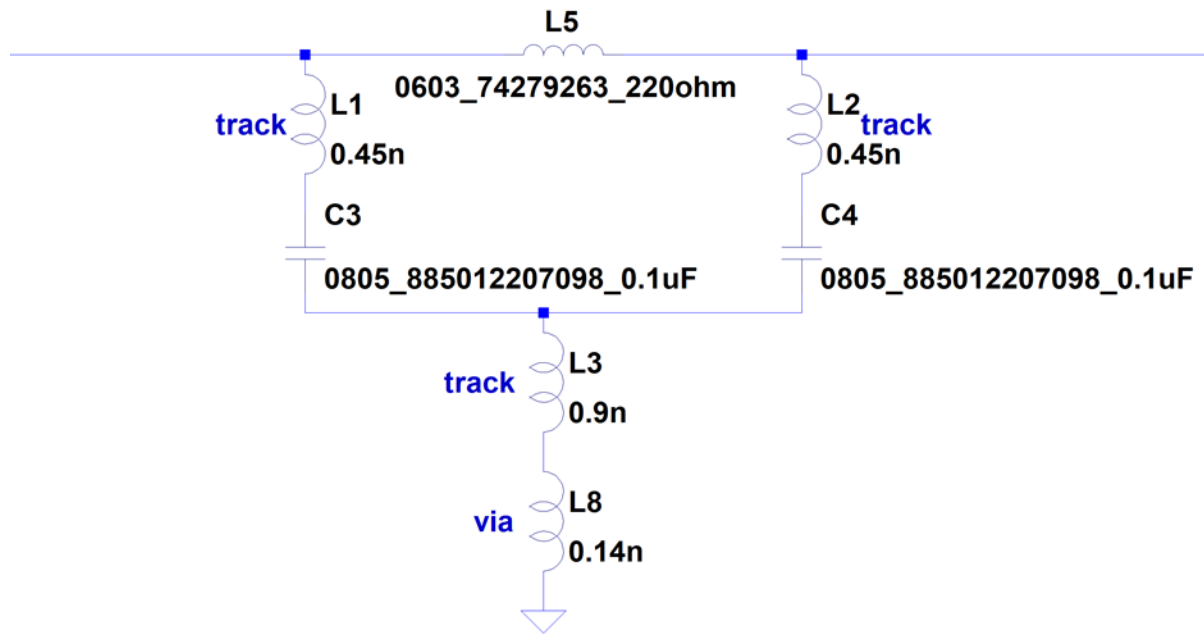
PI filter

Bad board realization – parasitics and couplings



PI filter

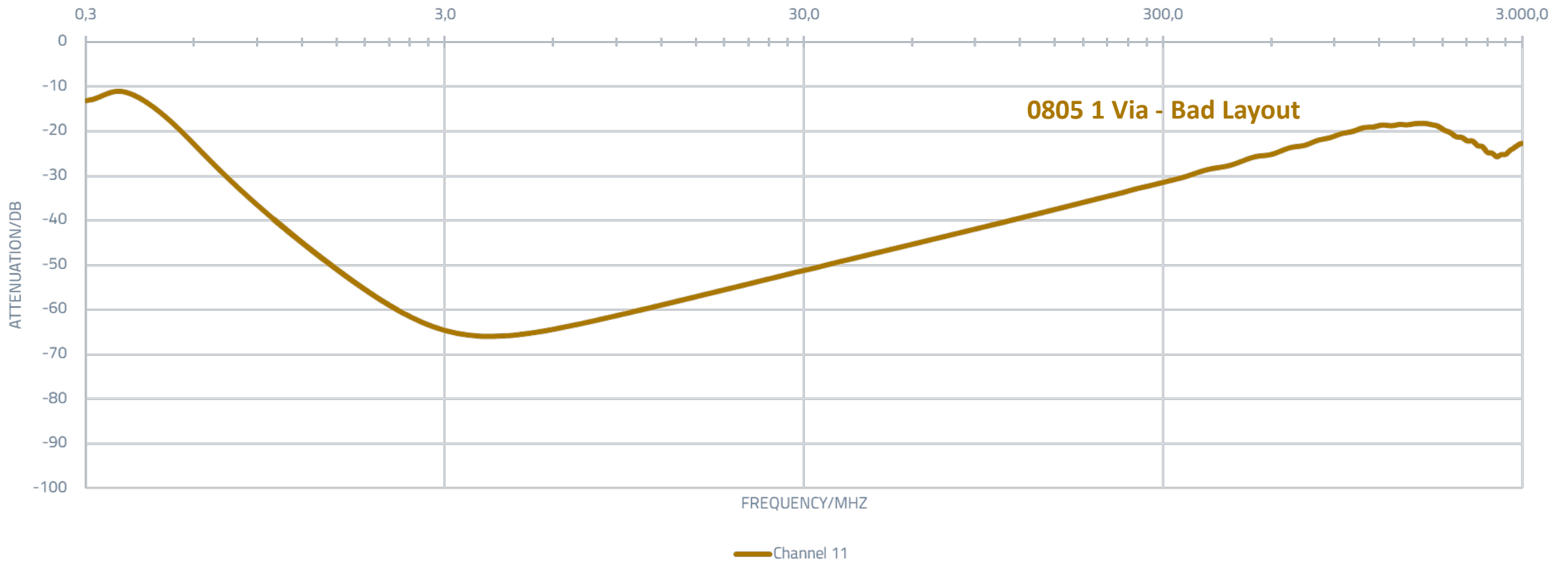
Simulation with parasites but without coupling



PI filter

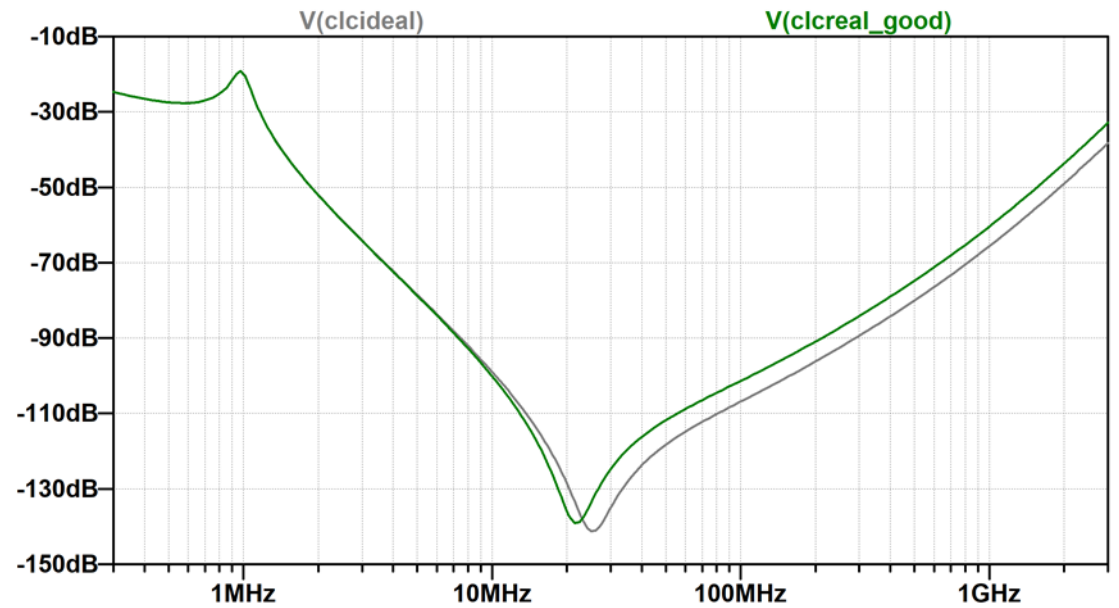
Measuring of insertion loss in parallel PLACEMENT design with coupling effects

S21 Insertion Loss (R&S ZNB20 VNA)



PI filter

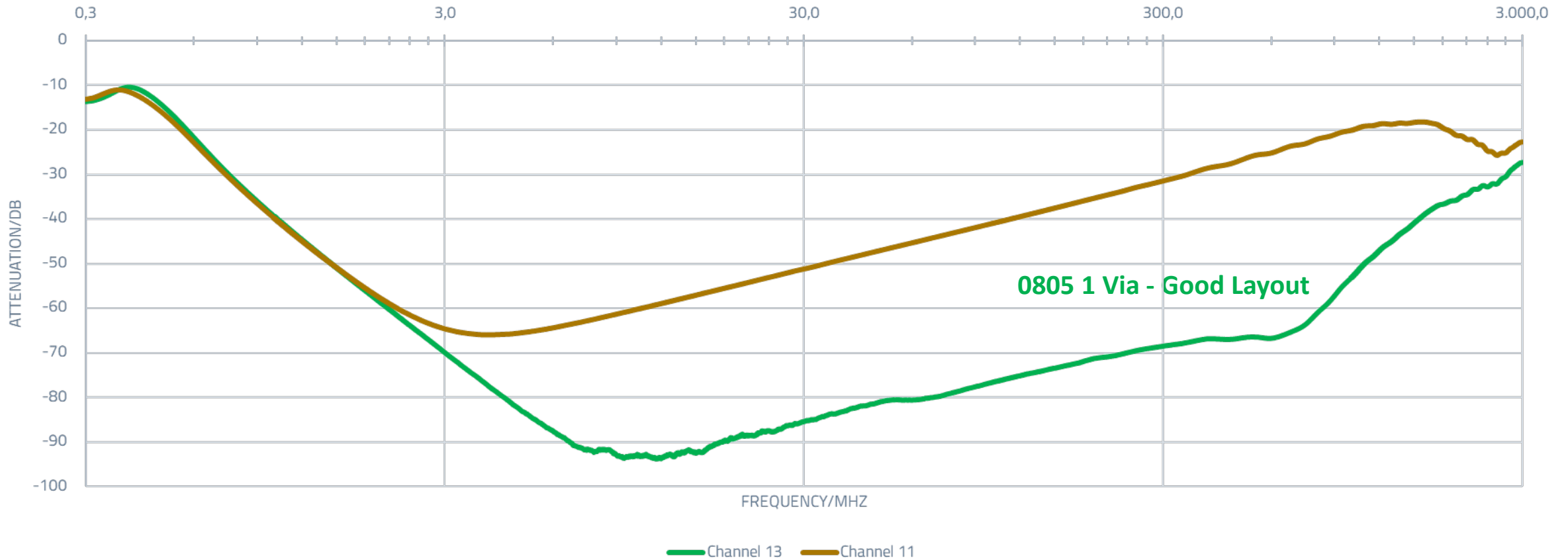
Good board realization



PI filter

Measurement of insertion loss in a 90° PLACEMENT design

S21 Insertion Loss (R&S ZNB20 VNA)



PI filter

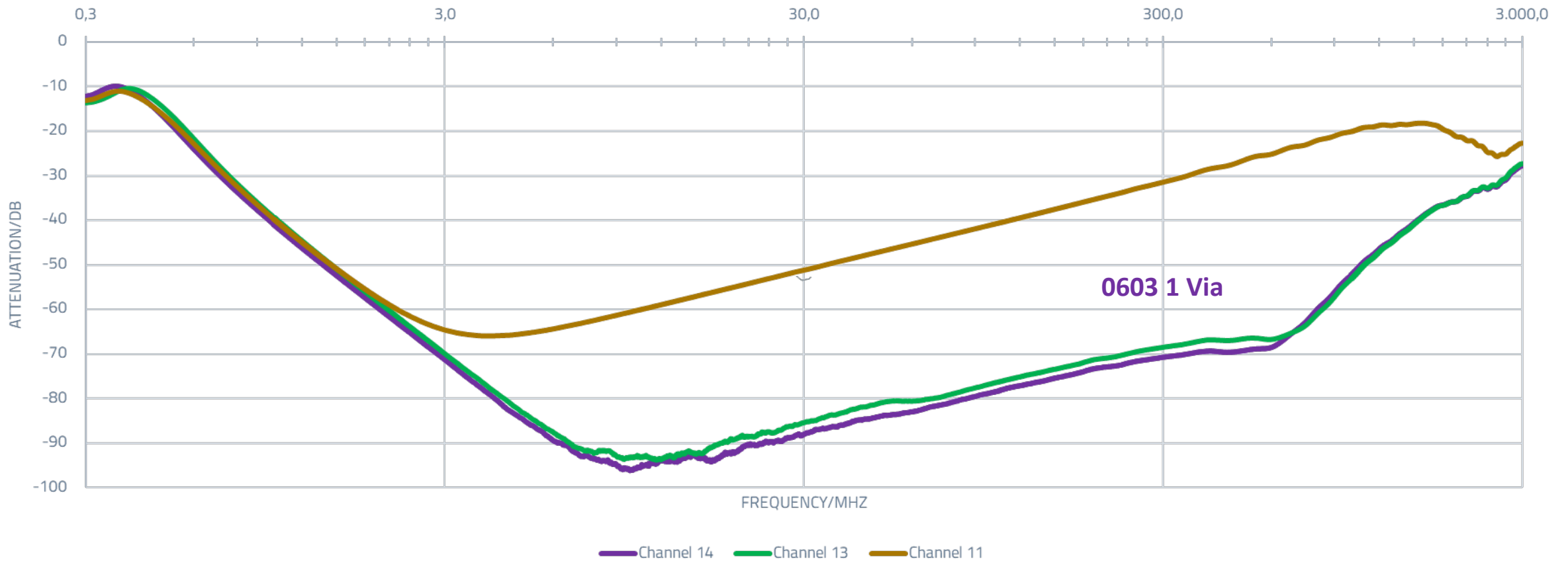
Good board realization with smaller components



PI filter

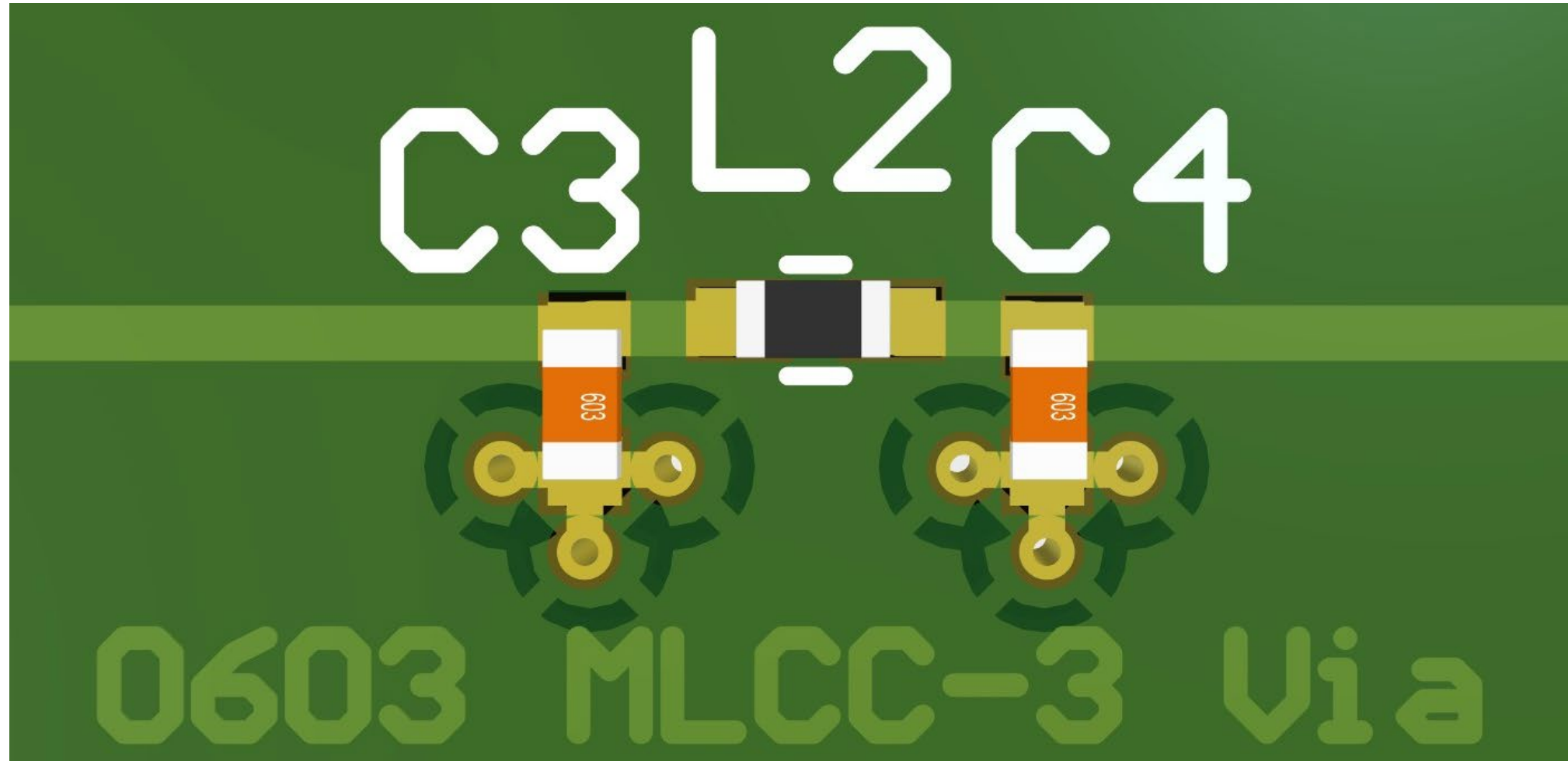
Measurement of insertion loss in a 90° design

S21 Insertion Loss (R&S ZNB20 VNA)



PI filter

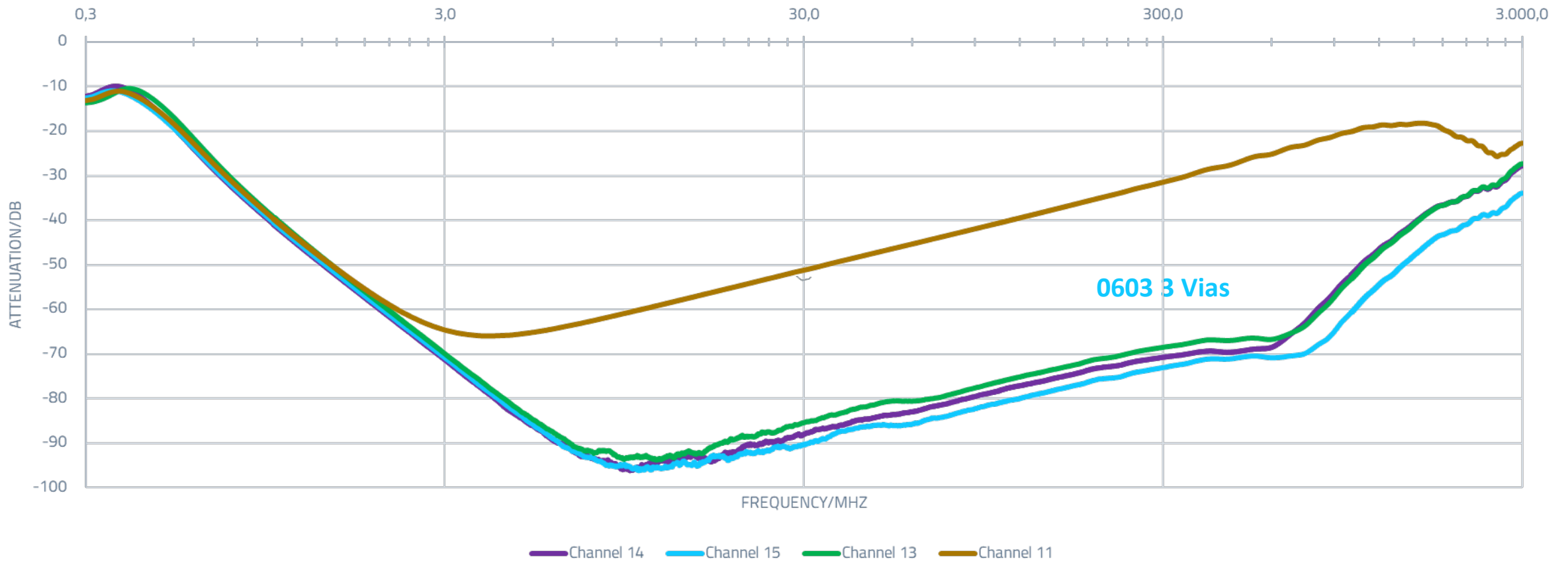
Better board realization with 3 Vias



PI filter

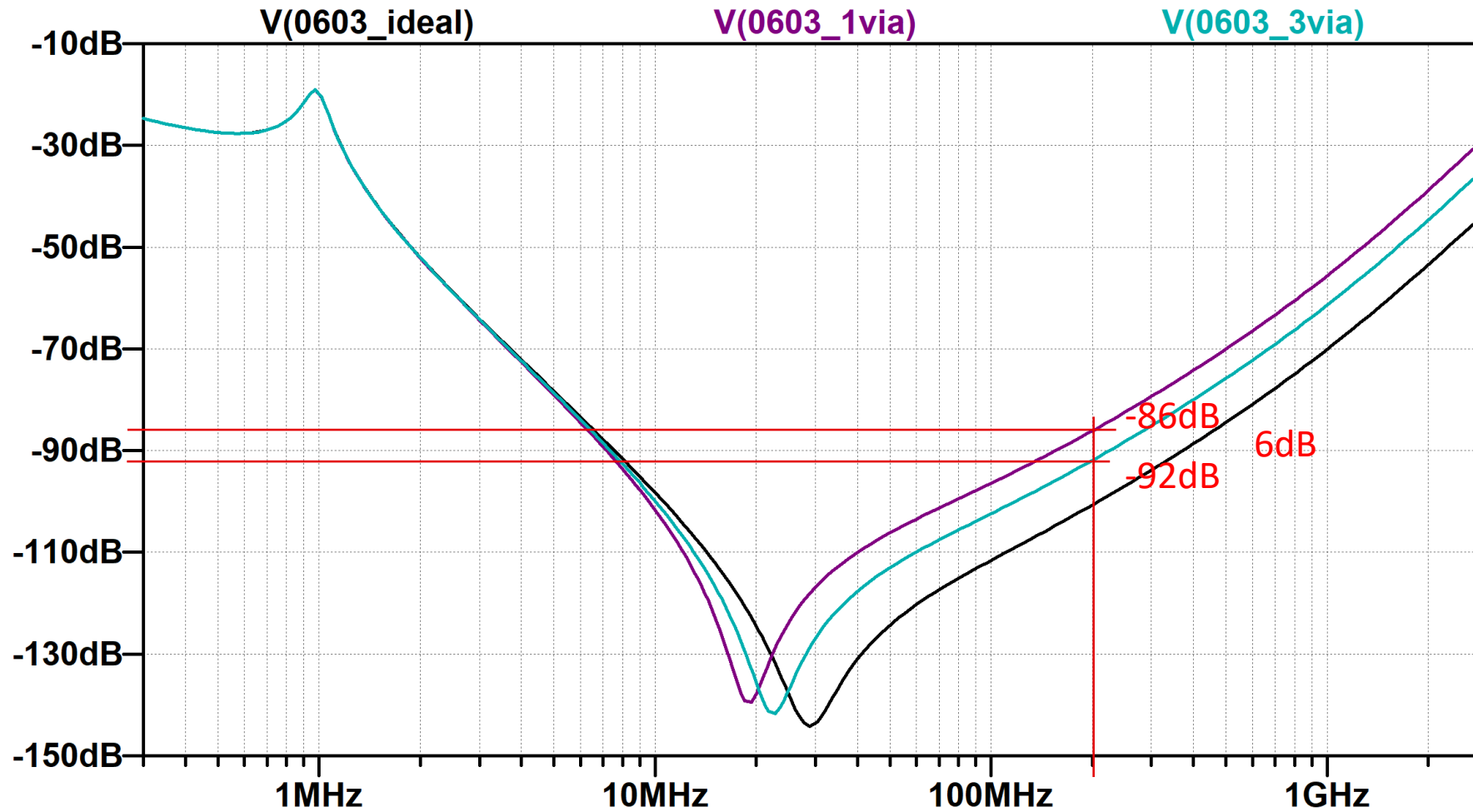
Measurement of insertion loss in a 90° design

S21 Insertion Loss (R&S ZNB20 VNA)

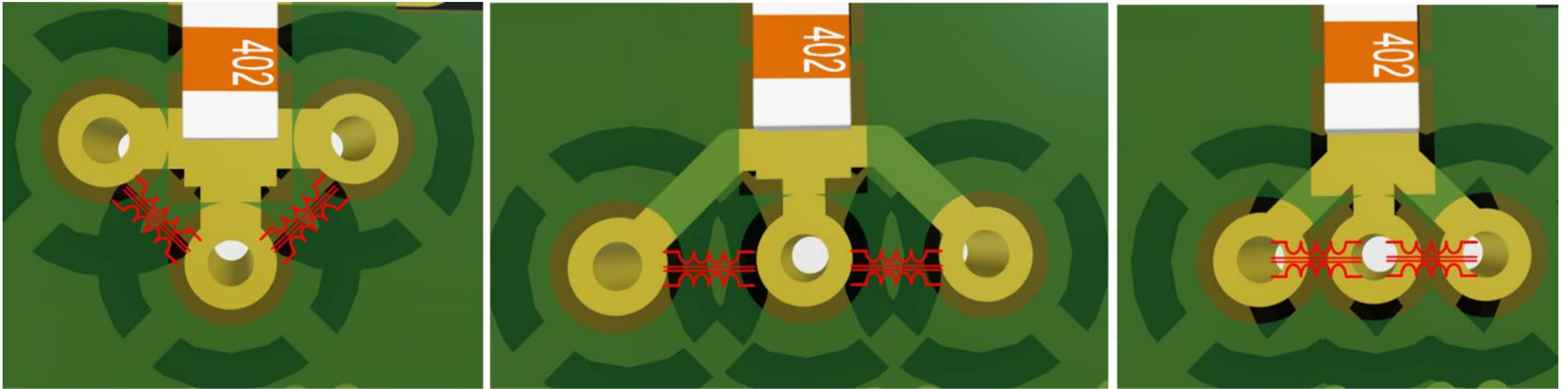


PI filter simulation with LTSpice

Simulation with LTSpice – PI with MLCCs and ferrite, inductances of track/vias

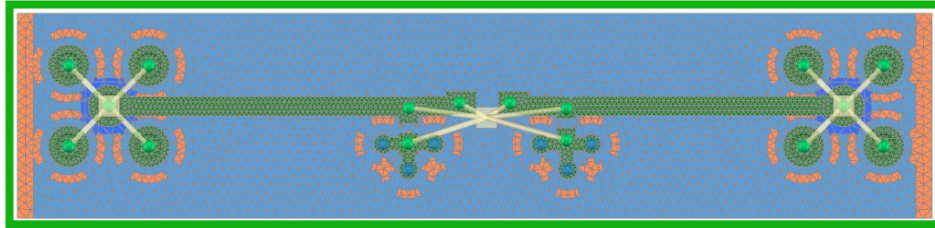


Different GND Via Placement

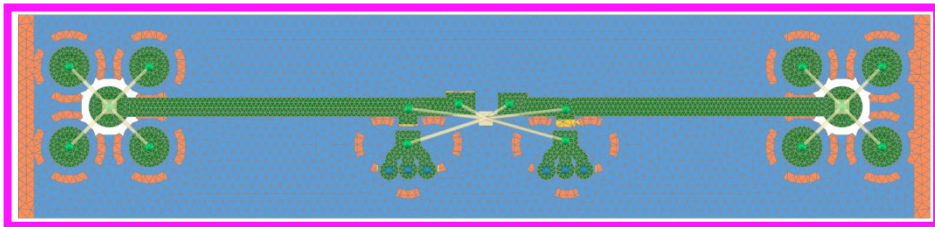


Different GND Via Placement

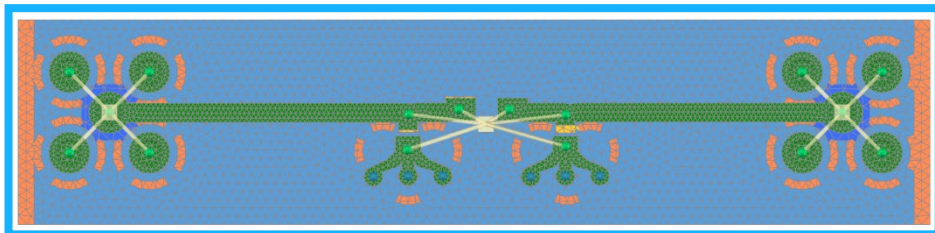
EMCOS Simulation show up to 4dB difference



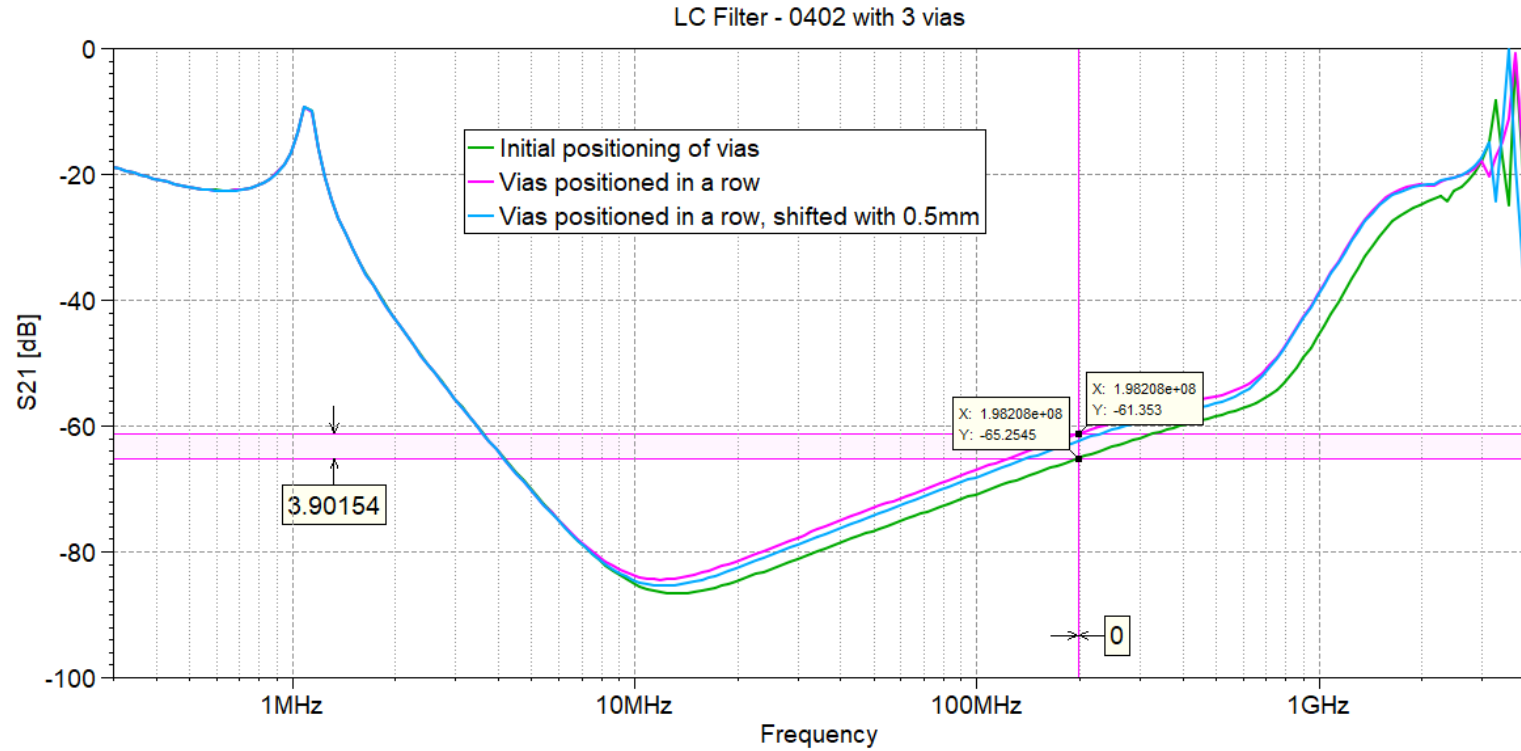
Initial positioning of vias



Vias positioned in a row



Vias positioned in a row, shifted with 0.5mm

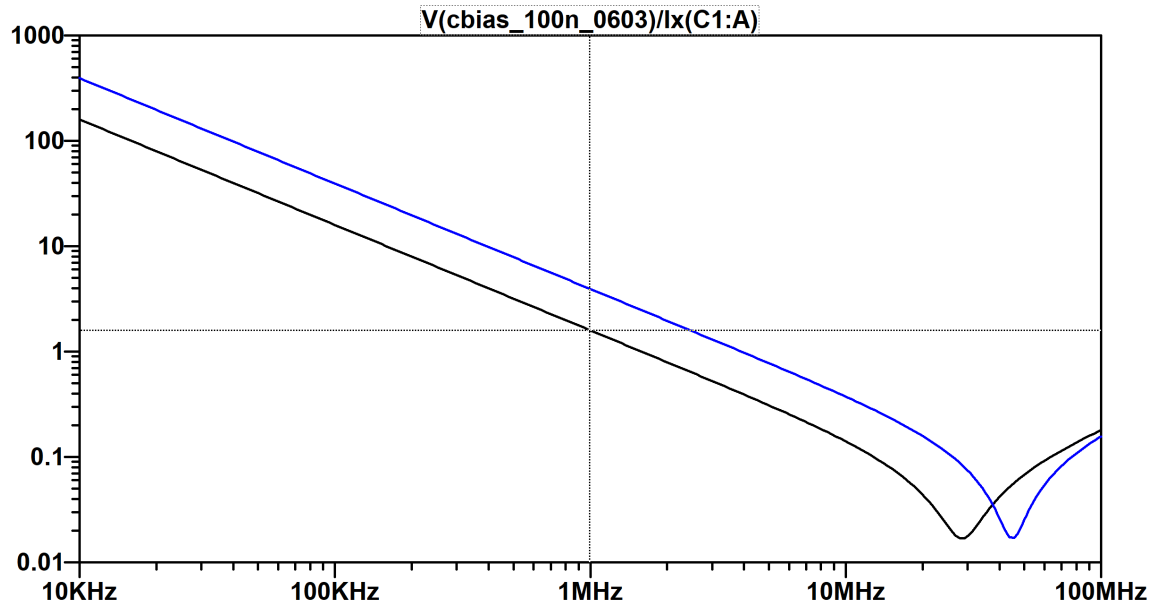


BIAS EFFECTS

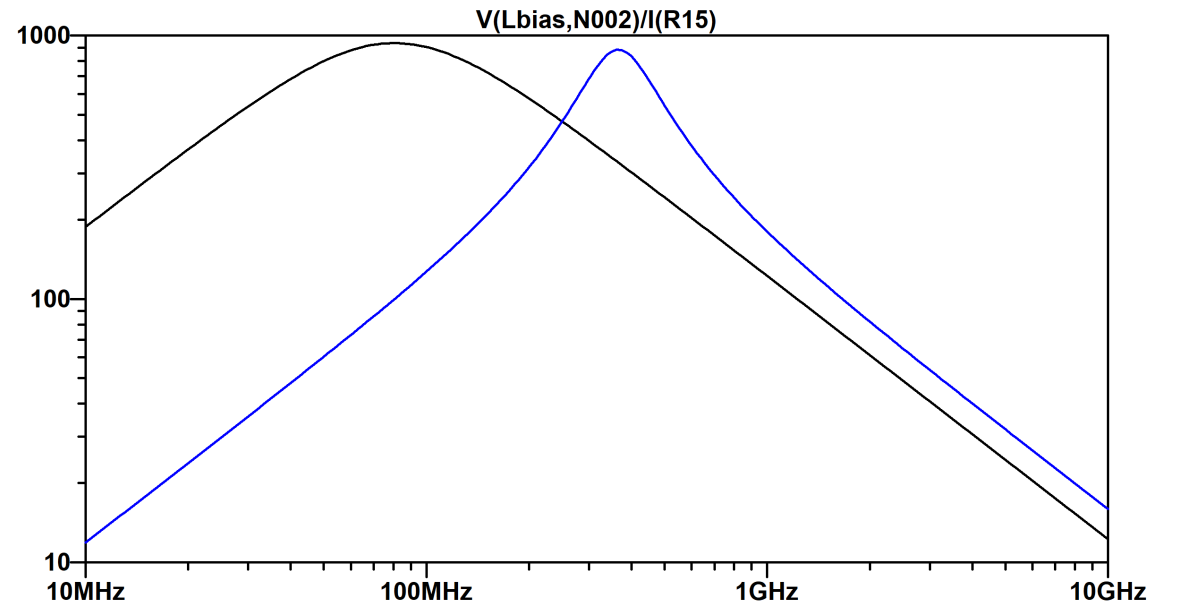


Impact of voltage- and current biasing

Capacitor and ferrite



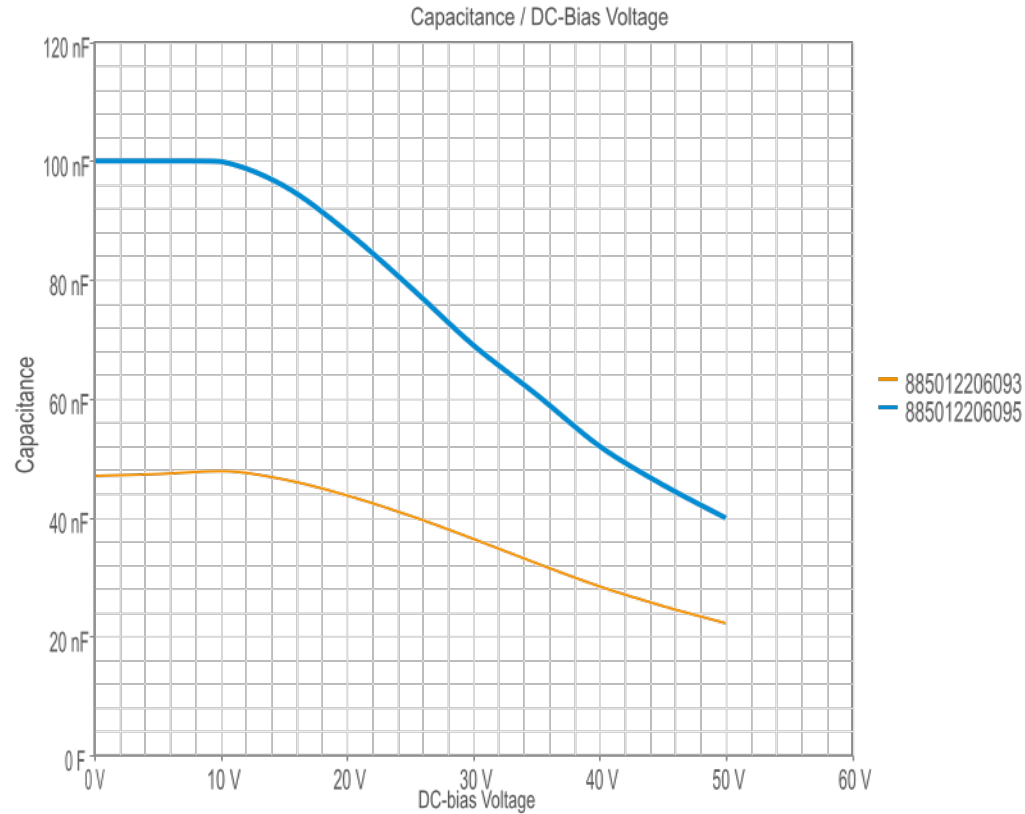
Capacitor Bias effects



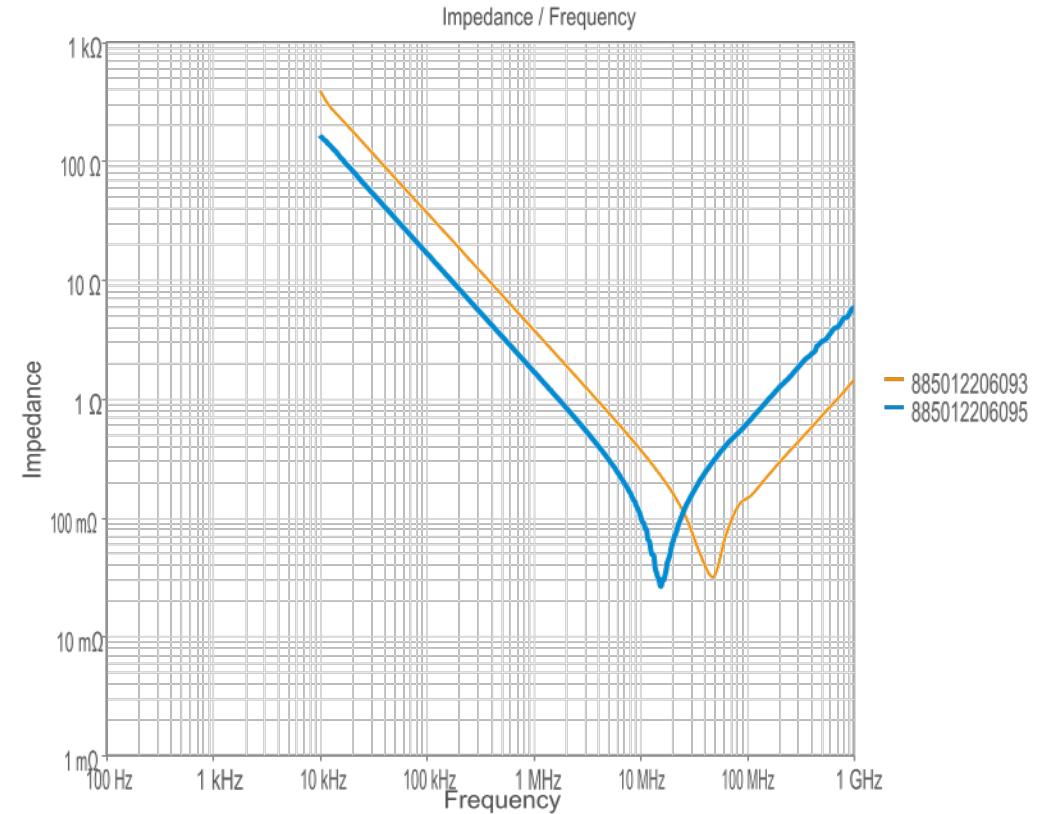
Inductor (ferrite) Bias effects

Impact of voltage- and current biasing

Equivalent capacitor component for simulation



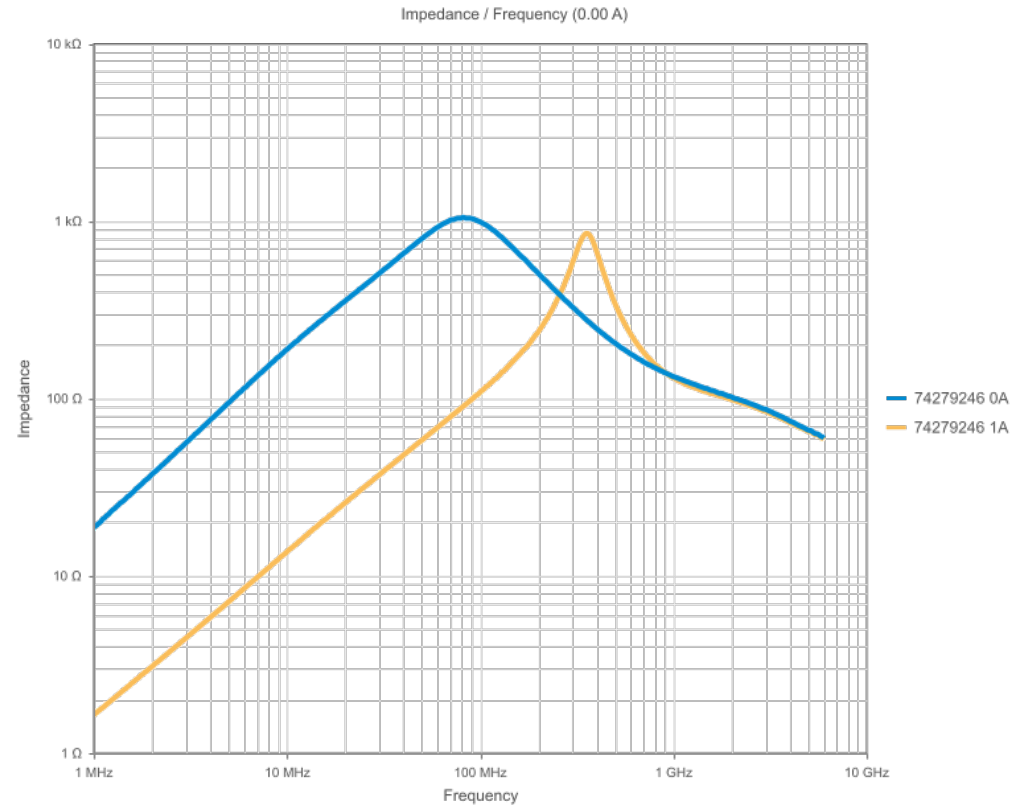
DC-Bias 885012206095 vs. 885012206093



Impedance 885012206095 vs. 885012206093

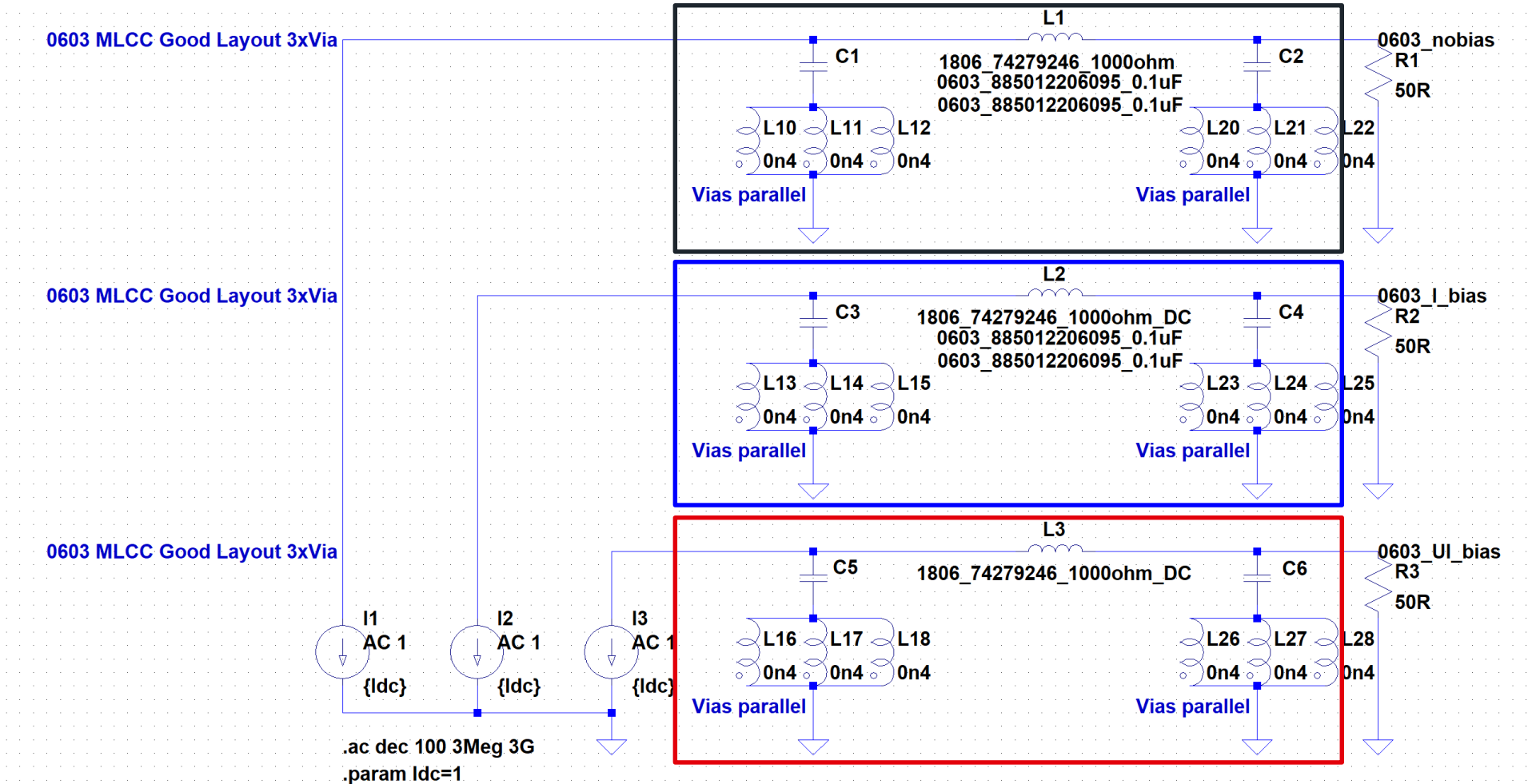
Impact of voltage- and current biasing

Behavior of ferrite



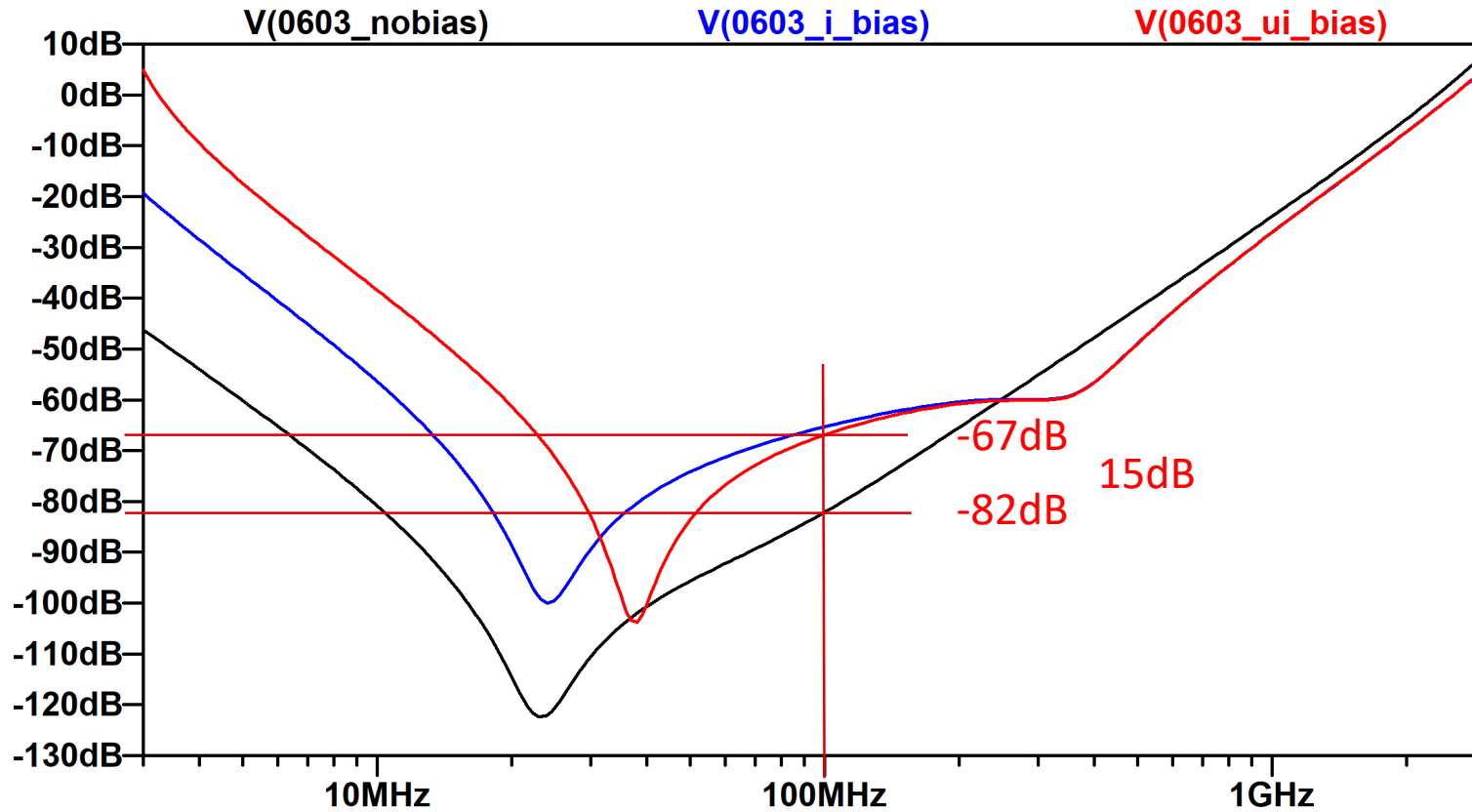
Impact of voltage- and current biasing

Simulation



Impact of voltage- and current biasing

Simulation results



PI-Filter mit Anbindung zu GND

