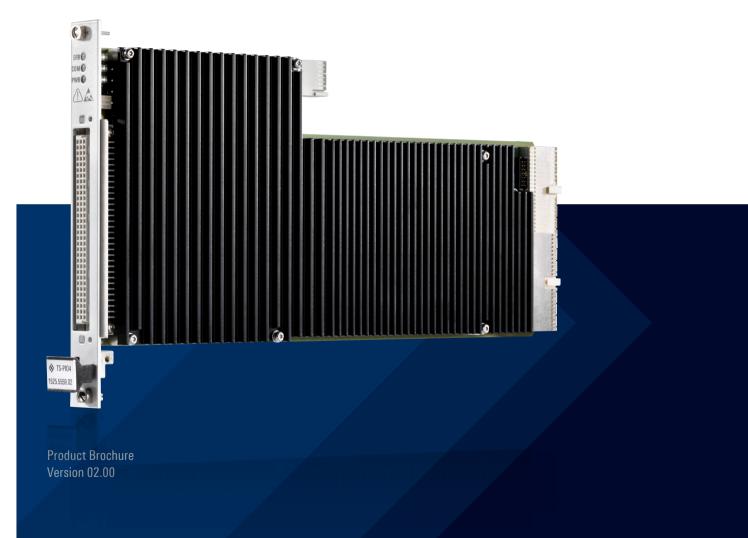
# **R&S®TS-PIO4 DIGITAL FUNCTIONAL TEST MODULE**

### 32-channel programmable digital I/O module





Make ideas real

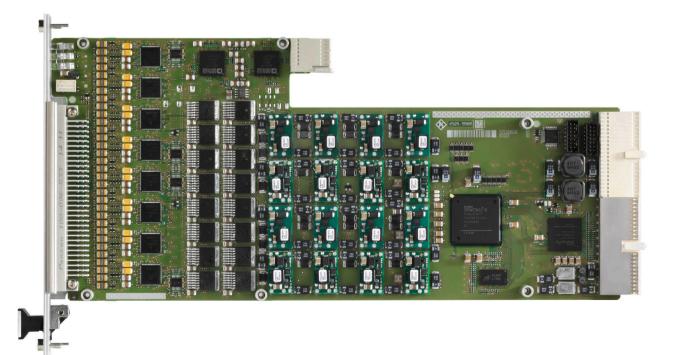


## AT A GLANCE

The R&S<sup>®</sup>TS-PIO4 digital functional test module contains flexibly programmable 32 bit digital inputs and 32 bit digital outputs that are able to acquire and stimulate static or dynamic digital patterns.

#### **Key facts**

- 32 digital input and 32 digital output channels
- ► 40 MHz sample rate, depending on levels and number of channels
- 12.5 ns resolution
- ► Eight groups of four channels each: -6 V to +10 V
- Tristate control for every output channel in dynamic mode
- Programmable DIO level (high and low) per group with 14 bit resolution
- > Two programmable input threshold levels per group for hysteresis mode or level monitoring in compare mode
- ► High output current with 150 mA per channel
- > FPGA based flexibility and realtime task execution independent of operating system used
- Synchronization/triggering (bidirectional) via PXI trigger bus or XTI (TTL)
- External clock input via EXT\_CLK input pin (TTL)
- Self-test software
- Soft front panels for immediate use
- LabWindows/CVI device driver support
- R&S<sup>®</sup>GTSL generic test software library in DLL format



### PRODUCT INTRODUCTION

The R&S<sup>®</sup>TS-PIO4 digital functional test module is a PXI module that takes up only one slot on the R&S<sup>®</sup>TSVP test system versatile platform. The characteristics of the digital lines can be configured with 14 bit resolution levels per port. In addition, the levels of the output ports can be programmed to meet application requirements.

The input ports have a programmable threshold and hysteresis to match the specifications of common digital logic families.

Synchronization to digital communications, handshake signals and analog measurement procedures is provided via trigger lines accessible at the front panel connector or via the PXI trigger lines. Additionally, the module can generate trigger pulses derived from digital pattern comparisons and detect changes at the input ports to interact with other modular instruments within the chassis.

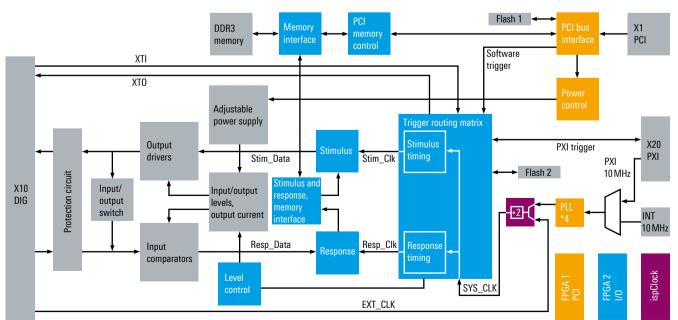
The digital channels are equipped with protection circuits and signal conditioning features, making the R&S®TS-PIO4 digital functional test module a robust device for various tasks in automatic test equipment (ATE) applications, which account for a large proportion of measurement and control tasks.

### FLEXIBILITY AND VERSATILE DEPLOYMENT

The module is designed to offer expanded flexibility for various application scenarios and high speed digital I/O patterns. The digital I/O interfaces are programmable, enabling the module to meet a wide variety of requirements regarding data transfer, communications and trigger settings.

The programmable output levels and input threshold levels of the configurable ports ensure compatibility with future generations of digital components. To improve noise immunity in test environments, the hysteresis of the input channels can be configured portwise.

If a higher number of digital I/O lines is required, multiple R&S®TS-PIO4 modules can be used and synchronized within the R&S®TSVP platform or synchronized to other types of measurements via the PXI trigger bus.



#### Functional block diagram

### TEST AND MEASUREMENT SCENARIOS

The R&S<sup>®</sup>TS-PIO4 digital functional test module can be used in all test and measurement scenarios where simple or complex digital circuits have to be tested using static or dynamic digital patterns.

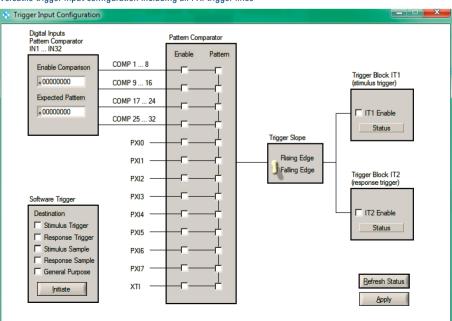
For many applications, realistic simulation of the DUT's environment during testing is most important. The R&S®TS-PIO4 therefore offers simultaneous deterministic generation and acquisition of digital patterns at high data rates. This includes both tristate control and the implementation of bidirectional buses through software-configured connections of data input with data output channels.

Further applications are related to various programming tasks that have to be performed using state-of-the-art board test systems. The R&S<sup>®</sup>TS-PIO4 can handle most of the common programming procedures, supported by software drivers for downloading firmware to flash memories and transferring data streams to onboard memory.

A sophisticated set of trigger setups provides flexible synchronization to DUT signals or to multiple R&S®TS-PIO4 modules, R&S®TSVP measurement modules or commercially available PXI modules via the PXI trigger bus.

### TYPICAL APPLICATIONS

- Digital pattern input to and output from local memory buffer
- Stimulation of realtime digital data streams with variable bus width (up to 2 Msample, 32 bit data)
- Acquisition of realtime digital data streams with variable bus width
- Digital functional tests
- ► Downloads to flash memories, serial and parallel
- Digital control of I/O lines
- ► Simulation of digital bus lines
- FPGA based flexibility and realtime task execution independent of operating system used
- Timer: square wave generation with user-definable duty cycle and frequency
- ► Counter: event or frequency counter, 10 MHz
- Sophisticated, highly flexible trigger input and output configuration



#### Versatile trigger input configuration including all PXI trigger lines

### SOFTWARE SUPPORT

The R&S<sup>®</sup>TS-PIO4 module is supplied with an IVI-C compliant LabWindows/CVI driver. Function panels and online help, which are common features on all R&S<sup>®</sup>TSVP modules, are also provided.

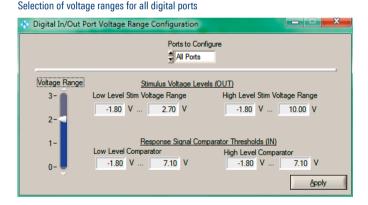
The definition and evaluation of complex digital test scenarios is supported by the R&S<sup>®</sup>GTSL generic test software library, which includes a DIO manager.

A set of soft front panels makes it easy for users to get familiar with the module's various functions. It allows users to verify test setups by simply using test panels rather than by programming. Waveform data can be loaded into and retrieved from the module's onboard memory using the driver functions provided by the DIO manager of the R&S<sup>®</sup>GTSL software package. The driver functions also include the synchronization of multiple modules and pattern sets.

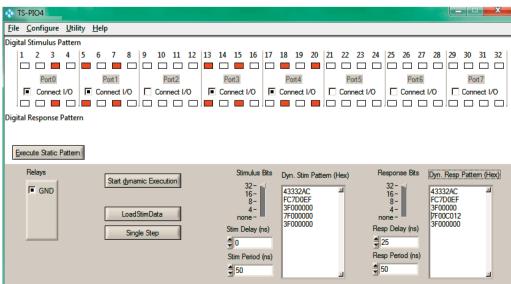
### SELF-TEST AND DIAGNOSTICS FOR RELIABLE OPERATION

The module's built-in self-test capability and the related self-test application offer functionality from fast diagnostics to complete, automated evaluation of output levels, trigger lines and switching paths.

Diagnostic LEDs on the module front panel speed up system integration and let users verify at a glance whether the system is working properly.



Easy manual operation via soft front panels (here: main soft front panel)



# **SPECIFICATIONS**

Specifications		
Use on R&S®TSVP platform		
PXI module		1 slot required
Interfaces		
Control bus		PXI
DUT connector (front)		DIN 41612, 96 pins
Rear I/O connector		CompactPCI connector, 110 pins
Module features		
Data input channels		
Channels	single-ended channels	32, on 8 ports of 4 bit
Input modes 1)		hysteresis, comparator
Input levels <sup>2)</sup>	clamping if outside range	
	range 0	–7.5 V to +10.0 V
	range 1	–5.0 V to +12.0 V
	range 2	–3.3 V to +12.0 V
	range 3	0.0 V to +12.0 V
Input thresholds <sup>2)</sup>	two programmable thresholds, 14 bit	resolution
	range 0	-6.0 V to +5.1 V
	range 1	–3.5 V to +7.1 V
	range 2	–1.8 V to +7.1 V
	range 3	+1.5 V to +7.1 V
Input resistance		1 MΩ
Signal acquisition timing		
Sample rate		0.01 Hz to 40 MHz with 12.5 ns resolution, depending on levels and number of channels
Trigger delay		50 ns to 50 s with 12.5 ns resolution
Data buffer depth/width	programmable	2 Msample at 32 bit (IN 1 to IN 32)
Protection		
Overvoltage protection		±24 V
Data output channels		
Channels	single-ended channels	32, on 8 ports of 4 bit; the number of channels that can be simulta- neously used depends on the level range, fre- quency and load <sup>2)</sup>
Output modes		analog, tristate
Analog output mode <sup>2)</sup>	output voltage	
	range 0	VL = -6.0 V  to  -1.5 V
		VH = -6.0 V  to  +8.0 V
	range 1	VL = -3.5 V to +1.0 V
		VH = -3.5 V  to  +10.0 V
	range 2	VL = -1.8 V to $+2.7 V$
		VH = -1.8 V to +10.0 V
	range 3	VL = +1.5 V to $+6.0 V$
		VH = +1.5 V to +10.0 V
	output current	max. 150 mA per channel, 10 mA to 350 mA per port <sup>1)</sup>
	output resolution	14 bit
Tristate control output mode	output voltage	none
Output resistance		typ. 30 Ω

Specifications		
Realtime stimulation <sup>1)</sup>		
Sample rate		0.01 Hz to 40 MHz at 12.5 ns resolution, depending on levels and number of channels
Trigger delay		50 ns to 50 s at 12.5 ns resolution
Data buffer depth/width Implementation of bidirectional data buses	programmable tristate control	2 Msample at 32 bit (OUT 1 to OUT 32) programmable, per sample; portwise connection of data input with data out-
Protection	short-circuit	put channels via onboard analog switches reverse voltage up to ±24 V at 150 mA
Relay channel	Short-circuit	Teverse voltage up to ±24 v at 150 mA
Ground-relay channel	ground relay to disconnect chassis ground for in-circuit tests (ICT)	SPST, to ground
Maximum switching voltage	DC/AC	30 V/50 V (RMS)
Maximum switching current	DC/AC	2 A/0.5 A (RMS)
Maximum switching power	DC/AC	60 W/62.5 VA
Pattern comparator		
Comparison		32 bit data input channel pattern with 32 bit reference pattern, 32 bit comparison enable mask
Applications		
Frequency measurement <sup>3)</sup>	maximum input frequency	10 MHz at 50% duty cycle
	minimum pulse width	50 ns
	frequency resolution	25 ns
	measurement time	200 ns to 50 s gate time or up to 2 <sup>32</sup> – 1 com- parator matches
	trigger	software trigger
Event counting <sup>3)</sup>	minimum pattern duration	50 ns
	gate time	200 ns to 50 s
	event counts	up to 2 <sup>32</sup> – 1
Trigger generator Synchronization	output to PXI trigger	XTO input to trigger units
Trigger units		2, fully independent hardware trigger logic
Applications		<ul> <li>programmable trigger generator</li> <li>generation of realtime stimulation clock</li> <li>generation of realtime acquisition clock</li> <li>frequency measurement</li> </ul>
Synchronization inputs		<ul> <li>1, local TTL trigger (XTI)</li> <li>8, PXI trigger bus</li> <li>1, pattern comparator</li> </ul>
Trigger unit characteristics <sup>4)</sup>	reference pattern	10 bit, 3 states: high, low, don't care
	slope	positive/negative
	delay	25 ns to 50 s
	output signals	<ul> <li>trigger received signal (25 ns pulse)</li> <li>trigger active signal (start of trigger until end of burst)</li> <li>sample pulse (25 ns pulse for each sample)</li> </ul>
Synchronization outputs		<ul> <li>▶ 1, local TTL trigger (XTO)</li> <li>▶ 8, PXI trigger bus</li> </ul>
Signals		<ul> <li>output, trigger unit 1 (IT1)</li> <li>output, trigger unit 2 (IT2)</li> <li>output, pattern comparator</li> <li>input signal to trigger unit (XTI)</li> </ul>
External clock		
Input voltage		5 V TTL
Frequency range		20 MHz to 40 MHz

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Dimensions $W \times H \times D$ (0.8 in $\times$ 6.8 in $\times$ 12.4 in)	RoHS	hazardous substances in electrical and electronic	
Veight 0.75 kg (1.65 lb)	Dimensions	$W \times H \times D$	
	Weight		0.75 kg (1.65 lb)

<sup>1)</sup> Programmable per group.

<sup>21</sup> For an estimation of the limits in ranges 0 to 3, see R&S®TS-PIO4 user manual, chapter 5.3.7 "Power consumption". If the operating mode to be used exceeds 80% of the maximum allowed power consumption, monitoring of the I/O driver temperature is recommended.

<sup>3)</sup> Uses one trigger unit.

 <sup>4</sup> Programmable per trigger unit.
 <sup>5</sup> Output voltage range 2 with VL = -1.8 V to +2.7 V, VH = -1.8 V to +10.0 V, 16 active outputs, frequency 20 MHz, sample rate 40 Mbps, no load (see user manual, chapter 5.3.7 "Power consumption").

# **ORDERING INFORMATION**

Designation Digital functional test module **Type** R&S<sup>®</sup>TS-PIO4 Order No.

1525.5559.02



TS-PI041525.5559.02



R&S®TS-PIO4 digital functional test module

#### Service that adds value

- ► Worldwide
- Local and personalized
- Customized and flexible
- Uncompromising quality
- Long-term dependability

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