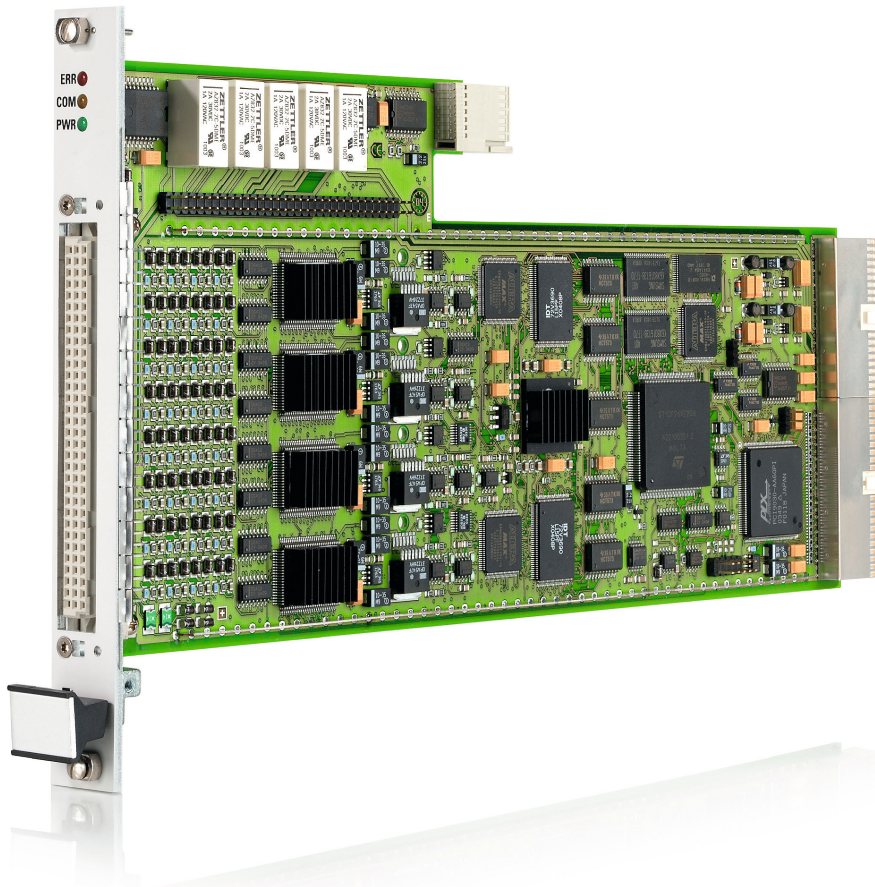


# R&S®TS-PDFT Digital Functional Test Module

High-speed 32-bit  
digital pattern I/O and  
serial communications  
interfaces



# R&S®TS-PDFT

## Digital Functional Test Module

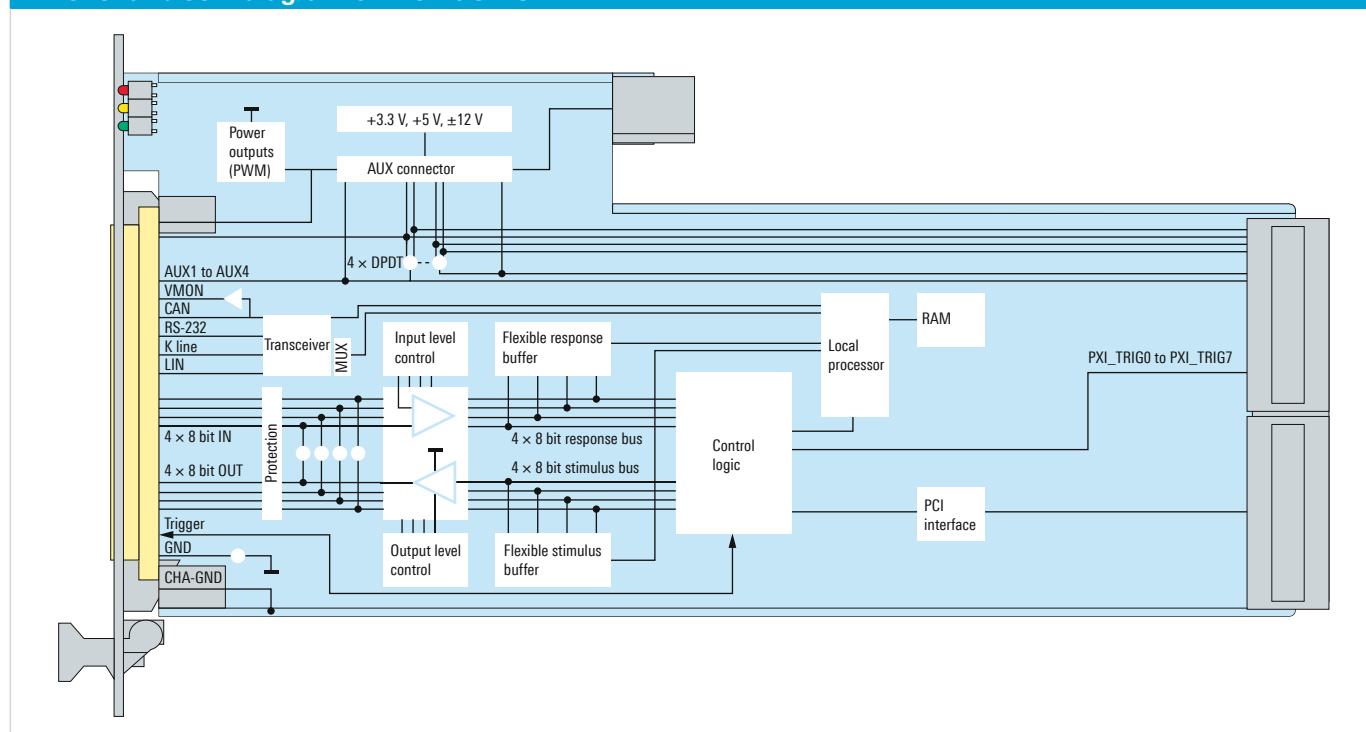
### At a glance

The R&S®TS-PDFT digital functional test module is a CompactPCI/PXI module which takes up only one slot in the R&S®CompactTSVP test system versatile platform.

#### Key facts

- 32 digital output channels in four groups
- 20 MHz pattern rate
- One programmable output level per group
- High output current
- Short-circuit protection
- Stimulation of digital realtime data, streams with variable bus width
- Four high-power open drain channels, fully protected, capable of pulse width modulation
- Five SPST relay channels
- 32 digital input channels in four groups
- Two programmable input threshold levels per group for hysteresis or level monitoring
- Acquisition of digital realtime data streams with variable bus width
- Overvoltage protection
- Serial communications interfaces
  - High-speed CAN 2.0b
  - Low-speed CAN 2.0b, fault-tolerant
  - RS-232/K bus
  - SPI bus emulation (master)
  - I<sup>2</sup>C bus emulation (master)
- Local microprocessor
- For time-critical tasks independent of the operating system used
- Synchronization via PXI trigger bus
- Software front panels for immediate use
- Selftest software
- LabWindows/CVI device driver support
- Test software library GTSL in DLL format

Functional block diagram of the R&S®TS-PDFT



## Product introduction

The R&S®TS-PDFT digital functional test module contains very flexibly programmable 32-bit digital inputs and 32-bit digital outputs which are able to acquire and stimulate static or dynamic digital patterns. The characteristics of the digital lines can be configured in 8-bit ports. In addition, the programmable levels of the output ports can be adjusted to the application requirements, and the input ports have a programmable threshold and hysteresis to match the specifications of common digital logic families.

Synchronization to digital communications, handshake signals and analog measurement tasks is provided via trigger lines accessible at the front connector or via the PXI trigger lines. Additionally, the module can generate trigger pulses derived from digital pattern comparisons and perform change detection at the input ports.

The digital I/O capabilities of the R&S®TS-PDFT are supported by the on-board microprocessor which can provide various communications interfaces especially suited for automotive applications.

Simulation of the DUT's environment is simplified by providing floating relays to switch supply voltages or loads to the DUT. With four additional power-output channels that can be pulse-width-modulated, digital control signals with up to 1 A can be applied to the test setup via open drain switching outputs.

The digital channels are equipped with protection circuits and signal conditioning features making the R&S®TS-PDFT digital functional test module a robust device for various in automatic test equipment (ATE) tasks, effectively covering a wide scope of measurement and control objectives.

## Typical applications

The R&S®TS-PDFT digital functional test module can be used in all test and measurement scenarios where simple or complex digital circuits have to be tested using static or dynamic digital patterns. The feature of DUT programming in production provides a very efficient one-step approach to testing and uploading firmware to the DUTs in the test process.

For many applications, realistic simulation of the DUT's environment during testing is most important.

The R&S®TS-PDFT therefore offers deterministic generation and simultaneous acquisition of digital patterns at high data rates. This includes both tristate control and the implementation of bidirectional buses by configuring port-wise connections of input and output lines by software. These test setups can be even operated in correlation with a realtime communications path based on standardized interfaces.

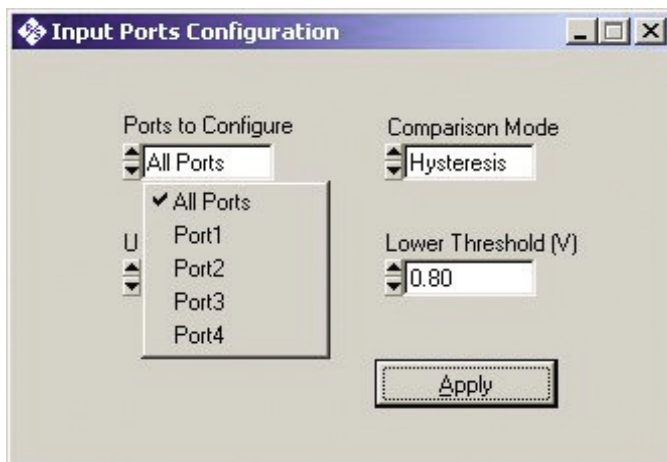
For automotive ATE, the most common interfaces are SPI, I<sup>2</sup>C, CAN, K bus or RS-232 which are supported by the R&S®TS-PDFT.

Further applications are related to various programming tasks that have to be performed by state-of-the-art board test systems. The R&S®TS-PDFT can handle most common programming procedures for downloading to flash memories and transferring data streams to on-board memory.

The on-board computing power provides firmware-implemented communications protocols and supports communications tasks that are time-critical or that need realtime response independently of the operating system that is running on the R&S®CompactTSVP system platform.

A sophisticated set of trigger setups provides flexible synchronization to DUT signals or synchronizes to multiple R&S®TS-PDFT modules, Rohde&Schwarz measurement modules or commercially available PXI modules via the standardized PXI trigger bus.

Configuration of input ports.



Typical applications include:

- Digital functional test
- Interfacing to digital communications
- Downloading to flash memories
- Deterministic stimulation and acquisition of digital data streams
- Digital I/O control
- Simulation of digital bus lines

## Flexibility

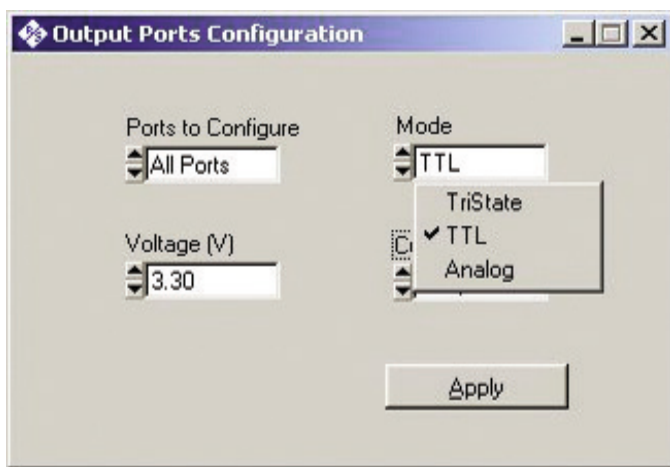
The design of the module offers expanded flexibility for various application scenarios and high-speed pattern I/O. The programmability of the digital I/O interfaces enables the module to meet a wide range of requirements regarding data transfer, communications and trigger settings. The features are contained in the free software front panels and are available for immediate use.

The programmable output levels and input threshold levels of the configurable ports ensure compatibility with future generations of digital components. To improve noise immunity in test environments, the hysteresis of the input channels can be configured groupwise.

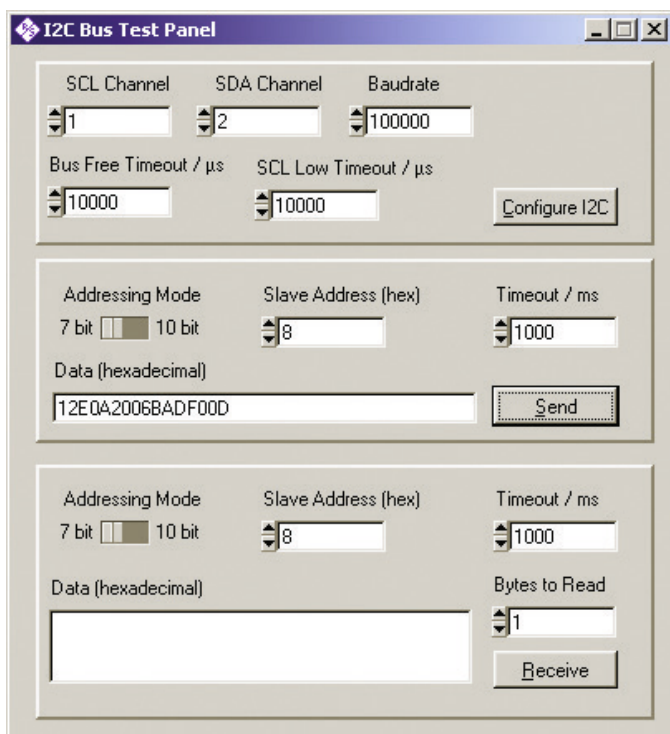
If a higher number of digital I/O lines is required, multiple R&S®TS-PDFT modules can be synchronized within the system or synchronized with other types of measurements via the PXI trigger bus.

To simplify update procedures, the firmware for the microcontroller and the on-board FPGA design can be easily downloaded. This allows the R&S®TS-PDFT firmware to be upgraded with new functionalities or enhancements.

Configuration of output ports.



I<sup>2</sup>C bus test panel.



## Software support

A LabWindows/CVI driver for standardized device operation is available for the R&S®TS-PDFT. Function panels and online help are available as common features for the LabWindows/CVI driver.

The definition and evaluation of complex digital test scenarios are supported by the Rohde&Schwarz generic test software library (GTSL) software including the DIO manager.

A set of software front panels makes it easy for users to learn the module's various functions. The software front panels also include features for evaluating serial communications protocols. This allows users to evaluate test set-ups by simply using test panels rather than by means of programming.

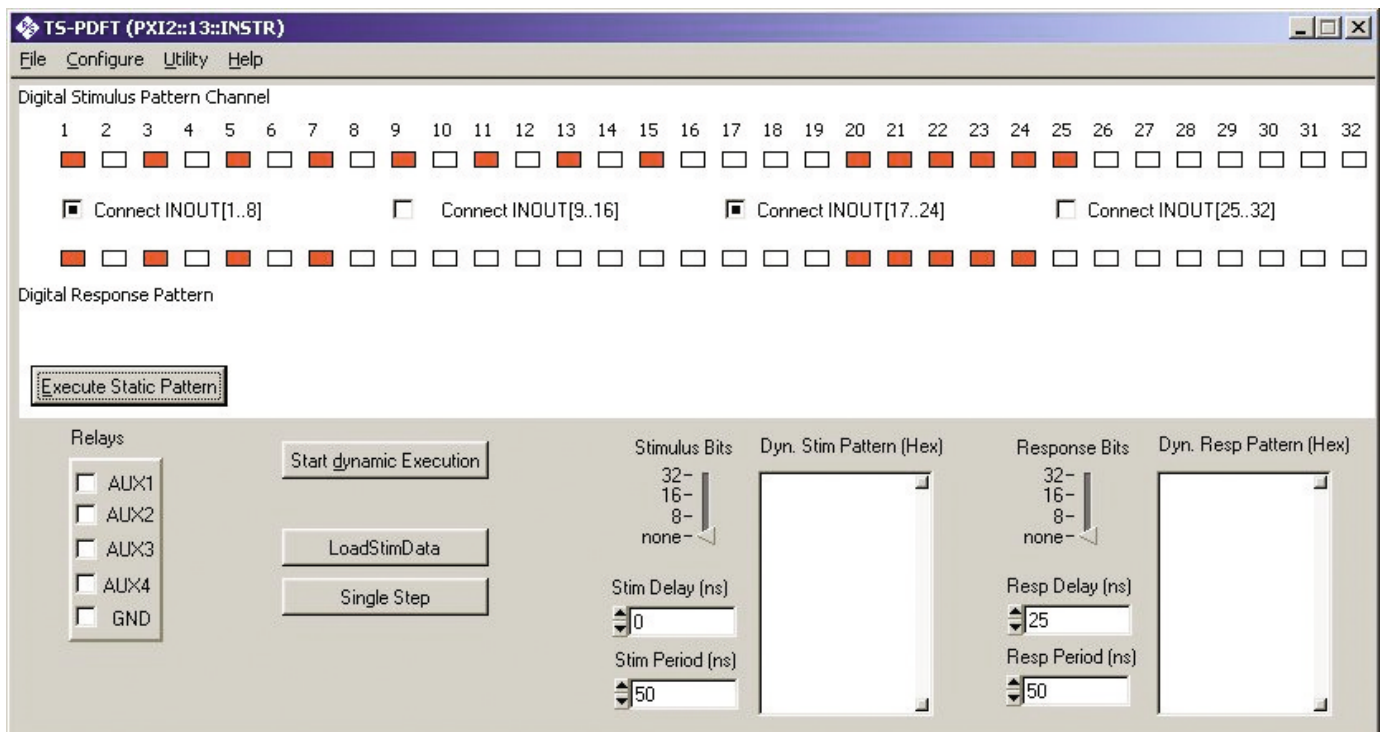
Waveform data can be loaded into and retrieved from the module's on-board memory using the driver functions provided by the DIO manager library, which is part of the Rohde&Schwarz GTSL software package. The driver functionality also includes the synchronization of multiple modules and pattern sets.

## Selftest and diagnostics for reliable operation

The built-in selftest capability of the module and the related selftest application ranges from fast diagnostics to the complete, automated evaluation of output levels, trigger lines and all switching paths.

Diagnostic LEDs on the module front panel speed up system integration and allow proper operation to be determined at a glance.

### Static digital I/O loopback.



# Specifications

| Specifications                              |  |  |
|---|--|--|
| <b>Application in R&amp;S®TSVP platform</b> | R&S®CompactTSVP                        | 1 slot required  |
| Interface                                   |  |  |
| Control bus                                 |  | CompactPCI/PXI   |
| DUT connector (front)                       |  | DIN41612, 96 pins  |
| Rear I/O connector                          |  | CompactPCI, 110 pins   |
| <b>Data input channels</b>                  |  |  |
| Channels                                    |  | 32, in 4 groups of 8 bit   |
| Input modes <sup>1)</sup>                   |  | hysteresis, comparator   |
| Input level                                 | clamping if outside range              | –5 V to +12 V  |
| Input thresholds <sup>1)</sup>              | two programmable thresholds            | 0 V to +9.5 V at 12-bits resolution  |
| Input resistance                            |  | 1 MΩ   |
| Realtime acquisition                        | sample rate                            | 0.01 Hz to 20 MHz with 25 ns resolution  |
|   | trigger delay                          | 0 s to 100 s with 25 ns resolution   |
|   | data buffer depth/width (programmable) | 131071 sample at 8 bits (IN 1 to 8)  |
|   |  | 65535 sample at 16 bits (IN 1 to 16)   |
|   |  | 32768 sample at 32 bits (IN 1 to 32)   |
| Protection                                  | overvoltage protection                 | ±42 V (max. 60 V < 30)   |
| <b>Data output channels</b>                 |  |  |
| Channels                                    |  | 32, in 4 groups of 8 bits  |
| Output modes                                |  | TTL, analog, tristate  |
| TTL output mode <sup>1)</sup>               | output voltage                         | $V_{OH} = +3.3 \text{ V (max.)}$   |
|   |  | $V_{OH} = +2.5 \text{ V at 20 mA (typ.)}$  |
|   |  | $V_{OL} = +0.8 \text{ V at 20 mA (typ.)}$  |
| Analog output mode <sup>1)</sup>            | output current                         | 80 mA (max.)   |
|   | output voltage                         | –3 V to 10 V   |
|   | output current                         | 150 mA per channel (max.),<br>10 mA to 700 mA per group <sup>1)</sup>                    |
|   | output resolution                      | 12-bit   |
| Tristate control output mode                | output voltage                         | none   |
| Output resistance                           |  | 39 Ω (typ.)  |
| Realtime stimulation <sup>1)</sup>          | sample rate                            | 0.01 Hz to 20 MHz at 25 ns resolution  |
|   | trigger delay                          | 100 ns to 100 s at 25 ns resolution  |
|   | data buffer depth/width (programmable) | 131071 sample at 8 bits (OUT 1 to 8)   |
|   |  | 65535 sample at 16 bits (OUT 1 to 16)  |
|   |  | 32768 sample at 32 bits (OUT 1 to 32)  |
|   | tristate control                       | programmable, per sample   |
| Implementation of bidirectional data buses  |  | portwise connection of data output with data input channels via on-board analog switches |
| Protection                                  | short-circuit                          | reverse voltage up to ±42 V at 150 mA  |
| <b>Power output channels</b>                |  |  |
| Channels                                    |  | 4, open drain  |
| Maximum switching voltage                   |  | +45 V  |
| Maximum switching current                   |  | 1 A per channel  |
| Pulse width modulation (PWM)                |  | 1 Hz to 40 kHz at 0% to 100%<br>duty cycle   |
| Protection                                  |  | short-circuit, overvoltage, overtemperature  |
| <b>Relay channels</b>                       |  |  |
| Channels                                    |  | 4, SPST, floating  |
|   |  | 1, SPST, to ground   |
| Maximum switching voltage                   | DC/AC                                  | 60 V/42 V (RMS)  |
| Maximum switching current                   | DC/AC                                  | 1.5 A/1.5 A (RMS)  |
| Maximum switching power                     | DC/AC                                  | 100 W/100 VA   |

| Specifications                      |                          |  |
|-------------------------------------|--------------------------|--|
| Communications interfaces           |                          |  |
| CAN interface                       | channels                 | 1 (microprocessor, full CAN) CAN 2.0B active, 11/29-bit identifier   |
|                                     | modes                    | low-speed, fault-tolerant (ISO 11519-2) up to 125 kBd, transceiver TJA1054 high-speed (ISO 11898) up to 1 MBd, transceiver PCA82C251 |
|                                     | termination              | programmable   |
|                                     | TX objects               | 4, software-FIFO-buffered  |
|                                     | RX objects               | 11, programmable filters, software-FIFO-buffered   |
|                                     | cyclic TX messages       | 2, independent frame bursts, software-FIFO-buffered, programmable cycle time   |
| Asynchronous serial interface       | channels                 | 1 (microprocessor, UART)   |
|                                     | modes                    | RS-232, K bus, TTL (uses XTI and XTO)  |
|                                     | transfer rates           | 110 bit/s to 115 bit/s   |
|                                     | data formats             | 1 start bits   |
|                                     |                          | 7 data bits with even/odd parity   |
|                                     |                          | 8 data bits with/without even/odd parity   |
|                                     |                          | 9 data bits  |
|                                     |                          | 1 or 2 stop bits   |
| SPI interface                       | channels                 | emulation of bus master via data channels<br>used outputs: 3 (CLK, MOSI, CS)<br>used inputs: 1 (MISO)                                |
|                                     | modes                    | 4  |
|                                     | transfer rate            | 100 bit/s to 300 kbit/s  |
|                                     | data formats             | 1 bit to 32 bit  |
|                                     |                          |  |
| I <sup>2</sup> C interface          | channels                 | emulation of bus master via data channels <sup>2)</sup>  |
|                                     | modes                    | outputs used: 2 (I <sup>2</sup> C_SCL, I <sup>2</sup> C_SDA)   |
|                                     |                          | inputs used: 2 (I <sup>2</sup> C_SCL, I <sup>2</sup> C_SDA)  |
|                                     |                          | 7-bit and 10-bit addressing  |
|                                     | transfer rate            | 50 bit/s to 300 kbit/s   |
| Pattern comparator                  |                          |  |
| Comparison                          |                          | 32-bit data input channels with 32-bit reference pattern<br>32-bit comparison enable mask  |
| Application                         |                          |  |
| Frequency measurement <sup>3)</sup> | maximum input frequency  | 12.5 MHz at 50% duty cycle   |
|                                     | minimum pulse width      | 40 ns  |
|                                     | frequency resolution     | 25 ns  |
|                                     | measurement time         | 100 s to 160 ns gate time or up to 65534 comparator matches  |
|                                     | trigger                  | software trigger   |
| Application                         |                          |  |
| Event counting <sup>3)</sup>        | minimum pattern duration | 40 ns  |
|                                     | gate time                | 100 s to 160 ns  |
|                                     | event counts             | up to 65534  |
| Application trigger generator       | output to PXI trigger    | XTO input to trigger units   |
| Realtime control unit               |                          |  |
| Local microprocessor                |                          | ST10F269   |
|                                     |                          | 16-bit   |
|                                     |                          | 40 MHz   |
|                                     |                          | 2 Mbyte RAM  |
| Synchronization                     |                          |  |
| Trigger units                       |                          | 2, fully independent hardware trigger logic  |
|                                     | applications             | programmable trigger generator   |
|                                     |                          | generation of realtime stimulation clock   |
|                                     |                          | generation of realtime acquisition clock   |
|                                     |                          | frequency measurement  |

## Specifications

### Synchronization

|  |                       |  |
|--|-----------------------|--|
| Trigger unit characteristics <sup>4)</sup> |                       | 2, fully independent hardware trigger logic              |
|  | input signals         | 1, local TTL trigger (XTI)                               |
|  |                       | 8, PXI trigger bus                                       |
|  |                       | 1, pattern comparator                                    |
|  | reference pattern     | 10-bit, 3 states: high, low, don't care                  |
|  | slope                 | positive/negative  |
|  | delay                 | 40 ns to 100 s   |
|  | output signals        | trigger received signal (25 ns pulse)                    |
|  |                       | trigger active signal (start of trigger until burst end) |
|  |                       | sample pulse (25 ns pulse for each sample)               |
| Synchronization outputs                    | channels              | 1, local TTL trigger (XTO)                               |
|  |                       | 8, PXI trigger bus                                       |
|  | signals <sup>5)</sup> | output trigger unit 1 (IT1)                              |
|  |                       | output trigger unit 2 (IT2)                              |
|  |                       | output pattern comparator                                |
|  |                       | input signal (XTI)                                       |

### General data

|                               |   |  |
|-------------------------------|---|--|
| Power consumption             |   | +3.3 V/0.5 A, +5 V/1.6 A, +12 V/0.4 to 2.4 A, -12 V/0.1 A  |
| Environmental conditions      |   |  |
| Temperature                   | operating temperature range                       | +5°C to +40°C  |
|                               | storage temperature range                         | -10°C to +60°C   |
| Damp heat                     |   | +40°C, 80% rel. humidity, steady state, in line with EN60068-2-30  |
| Mechanical resistance         |   |  |
| Vibration                     | sinusoidal  | 5 Hz to 55 Hz, 0.15 mm amplitude const., 55 Hz to 150 Hz, 0.5 g const., in line with EN60068-2-6                           |
|                               | random  | 10 Hz to 300 Hz, acceleration 1.2 g (RMS), in line with EN60068-2-64   |
| Shock                         |   | 40 g shock spectrum, in line with MIL-STD-810E, method 516.4, procedure I  |
| Product conformity            |   |  |
| Electromagnetic compatibility | EU: in line with EMC Directive 2004/108/EC        | applied harmonized standards: EN61326-1 (industrial environment), EN61326-2-1, EN55011 (class A), EN61000-3-2, EN61000-3-3 |
| Electrical safety             | EU: in line with Low Voltage Directive 2006/95/EC | applied harmonized standard: EN61010-1   |
| Dimensions                    | W × H × D   | 316 mm × 174 mm × 20 mm (12.4 in × 6.8 in × 0.8 in)  |
| Weight                        | R&S®TS-PSU power module                           | 0.8 kg (1.76 lb)   |
|                               | R&S®TS-PSU RIO module                             | 0.12 kg (0.27 lb)  |
|                               | R&S®TS-PSU AC/DC converter                        | 1.2 kg (2.65 lb)   |

<sup>1)</sup> Programmable per group.

<sup>2)</sup> External diodes and pull-up resistors required.

<sup>3)</sup> Uses one trigger unit.

<sup>4)</sup> Programmable per trigger unit.

<sup>5)</sup> Selectable per synchronization channel.

# Ordering information

| Designation                                  | Type        | Order No.    |
|--|-------------|--------------|
| Digital Functional Test Module               | R&S®TS-PDFT | 1143.0080.02 |
| R&S®CompactTSVP Test and Measurement Chassis | R&S®TS-PCA3 | 1152.2518.02 |

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R&S®TS-PDFT

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