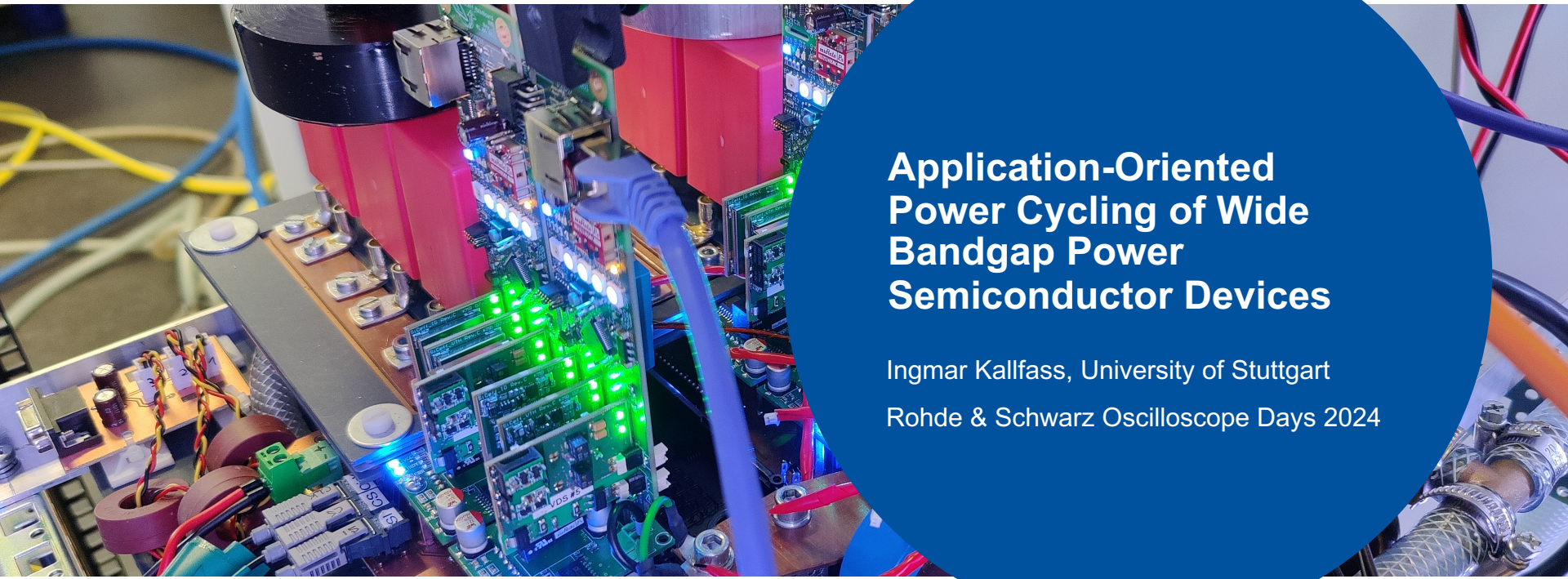
Universität Stuttgart
Institut für Robuste Leistungshalbleitersysteme



Application-Oriented Power Cycling of Wide Bandgap Power Semiconductor Devices

Ingmar Kallfass, University of Stuttgart

Rohde & Schwarz Oscilloscope Days 2024

Overview

- Motivation
- Principles of Dynamic Active Power Cycling
- Acquisition of Temperature-Sensitive Electrical Parameters (TSEP)
  - µC on Device Potential / Power Ground
  - µC on Isolated Potential / Signal Ground
- TSEP Measurements
- Multiple TSEP Sensor Fusion
- Outlook

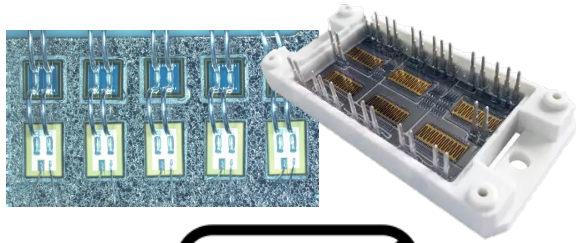
Motivation

accelerated lifetime testing

intelligent control

predictive maintenance

condition monitoring of power semiconductor devices and modules



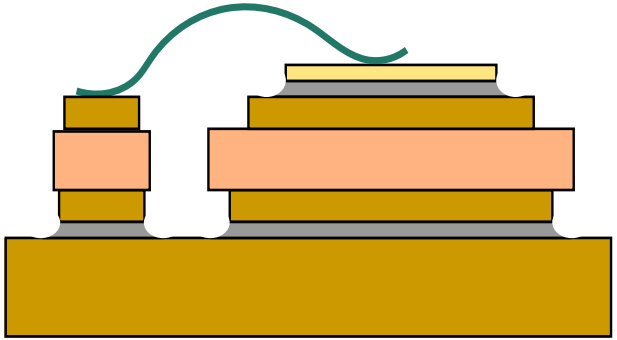
Temperature as a Key Factor in Reliability of Power Electronics

Extended LESIT study – bond wire and solder fatigure

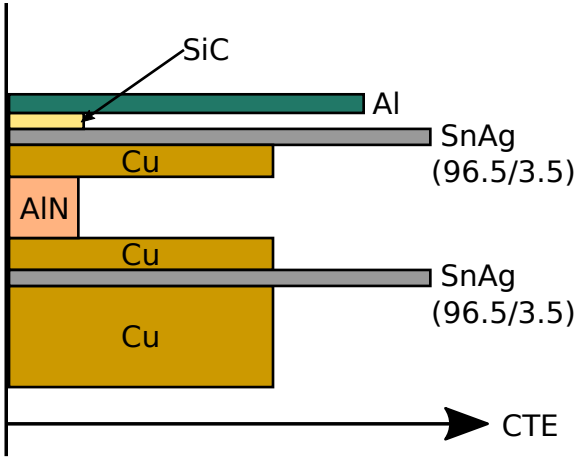
$$N_{\text{failure}} = K \cdot \Delta T_{\text{j}}^{\beta_1} \cdot e^{\frac{\beta_2}{T_{\text{j}}}} \cdot t_{\text{on}}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6}$$

Bayerer et.al. CIPS 2008

$N_{failure}$	number of cycles to failure
ΔT_j	temperature swing
T_j	mean temperature
t_{on}	on-time
I	current per bondwire
V	blocking voltage
D	bondwire diameter



bondwire
semiconductor die
solder
DBC
solder
baseplate
...
TIM
heat sink



Wide Bandgap Semiconductor Power Devices
SiC MOSFET and GaN HEMT

Johnson FOM: $\mathrm{FOM}_{\mathrm{Johnson}} = \frac{v_{sat} E_c}{2\pi}$

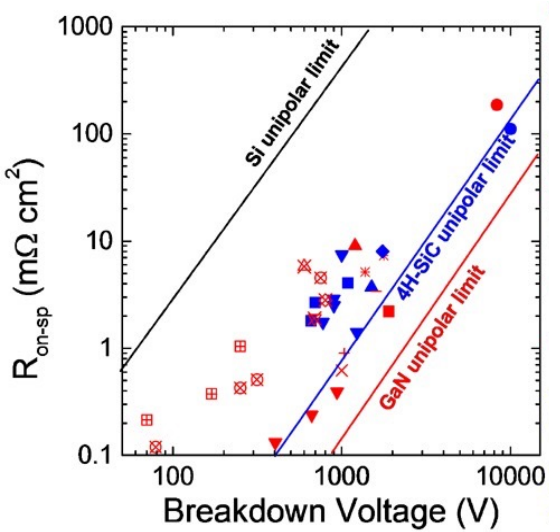
Baliga FOM: $\mathrm{FOM}_{\mathrm{Baliga}} = \varepsilon \mu_e E_g^3$

Hard switching loss FOM: $R_{on} Q = \frac{2}{\mu \cdot E_c^2} V_{bd}^2$

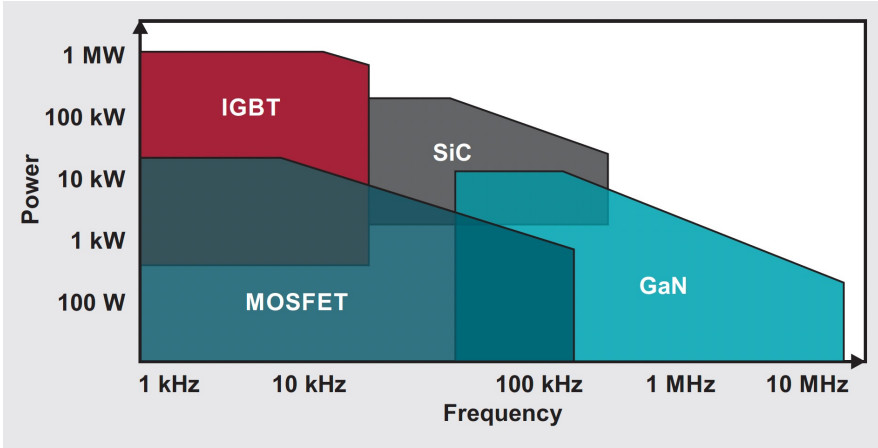
Power Density

High Temperature Operation

Reliability



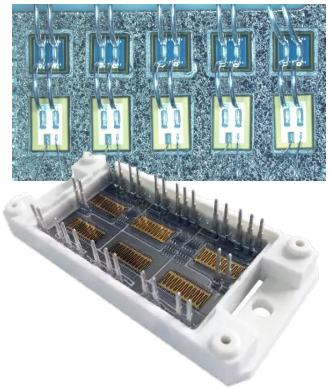
Physica Status Solidi (a)



Analog Design Journal

Condition Monitoring of Power Semiconductor Devices and Modules

control & drivers



sensing & readout electronics

- Temperature sensor
- R_{th}
- TSEPs
  - R_{on}
  - V_{sd}
  - $V_{th,\ on/off}$
  - $t_{on/off}$
  - $I_{g,peak}$

Indirect

Non-invasive

conventional

new

parameter acquisition & data processing

- Degradation
- Temperature estimation
- Combined TSEPs sensor fusion

PRINCIPLES OF DYNAMIC ACTIVE POWER CYCLING

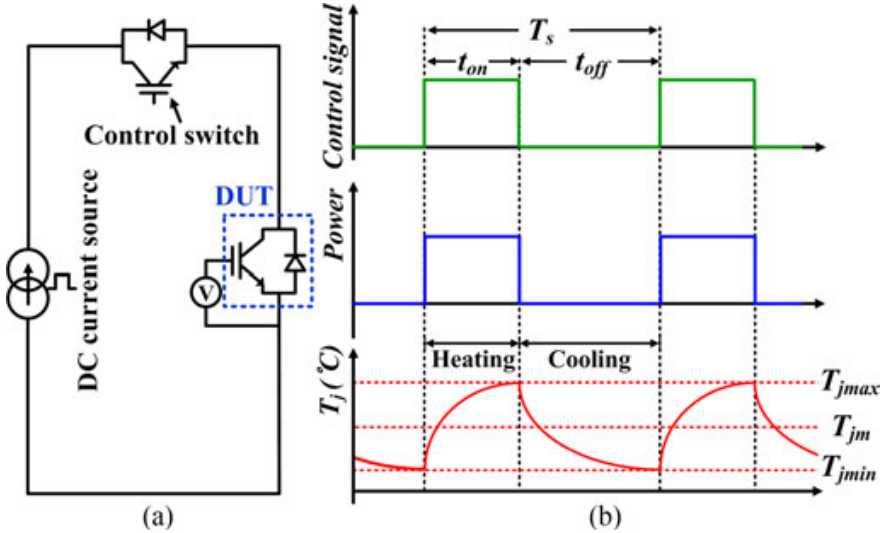
Active Power Cycling Tests
Static Active Power Cycling (sAPC)

Conventional method ("DC power cycling")

- Energization of the device under test (DUT) via a current source
- Cyclic heating and cooling phases induce temperature swing
- DUT does not actively switch, resulting in different power losses compared to normal operation

TSEP Acquisition

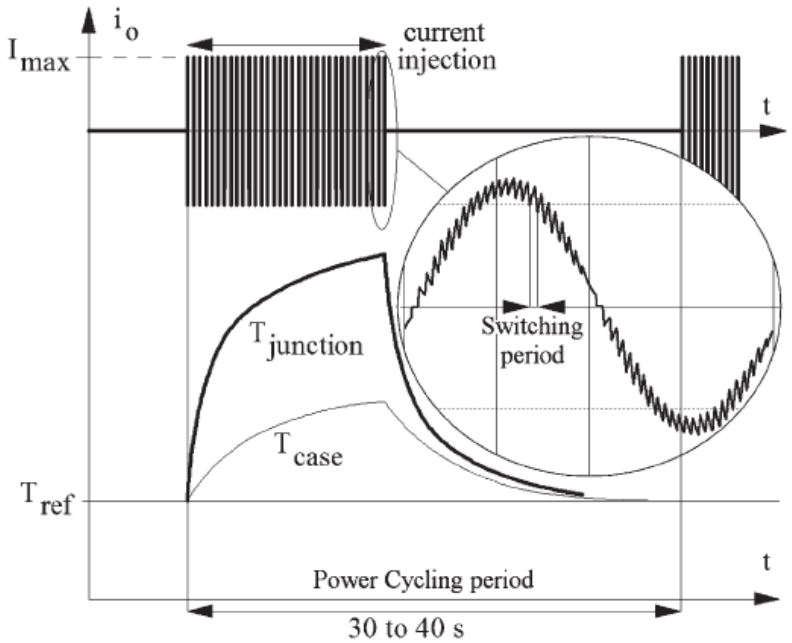
- "V_{SD}-method" ➔ voltage drop over body diode under application of a small (mA) measurement current



Choi, Ui-Min & Blaabjerg, F & Jorgensen, Soren. (2017). Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress. IEEE Transactions on Power Electronics. PP. 1-1. 10.1109/TPEL.2017.2690500.

Active Power Cycling Tests
Dynamic Active Power Cycling Tests (dAPC)

- Device heating through pulsed active power cycle
- Operation under realistic operating conditions incl. switching loss
- Voltage range adjustable up to the maximum blocking voltage of the modules
- Parameter acquisition more challenging due to realistic operating conditions



Choi, Ui-Min & Blaabjerg, F & Jorgensen, Soren. (2017). Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress. IEEE Transactions on Power Electronics. PP. 1-1. 10.1109/TPEL.2017.2690500.

Dynamic Active Power Cycling

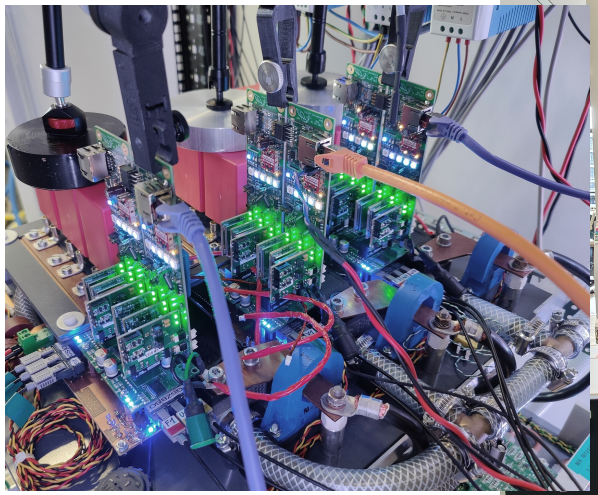
Methodology for dynamic power cycling pursued at the University of Stuttgart:

Approach

- Operation of the inverter in three-phase converter mode

Characteristics

- Load similar to the application
- Aging of the entire module
- Real-time online multi-TSEP acquisition in every switching period



Dynamic Active Power Cycling
System Overview

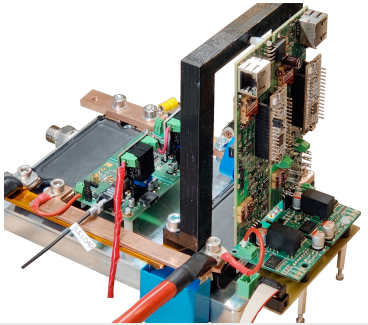
Rapid Control Prototyping System (dSPACE Microlabbox)

max. 1.2 kV / 132 A (SiC) power modules

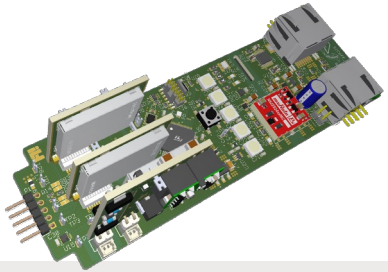
Temperature Control Unit 20°C – 150 °C

400 V / 800 V DC-link

Dynamic AC PCT



Back-To-Back Converter

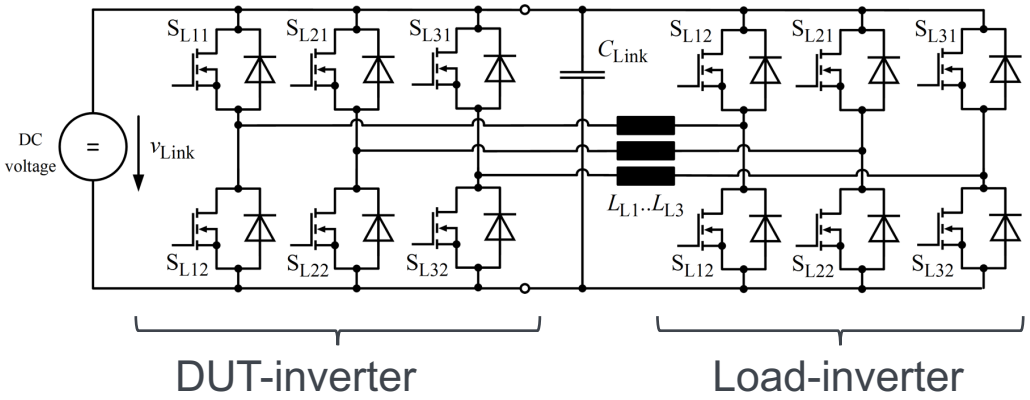


Parameter Acquisition

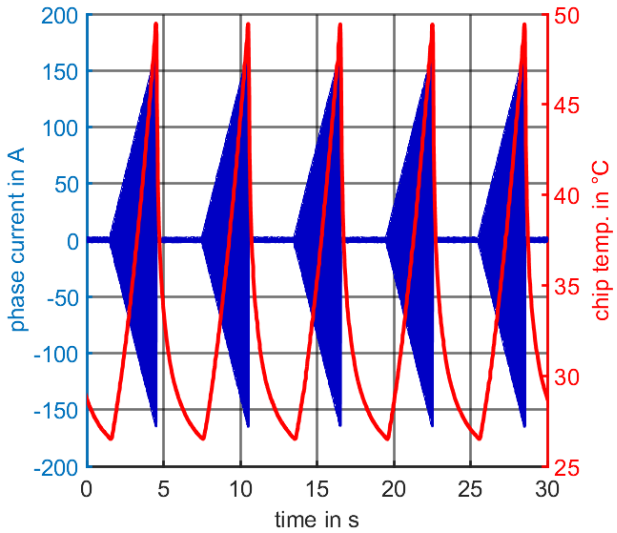
R_{on} / V_{sd}
$V_{th,\ on/off}$
$t_{on/off}$
$I_{g,peak}$

Dynamic Active Power Cycling
Three Phase inverters

- Control of two input- and output-side coupled inverters



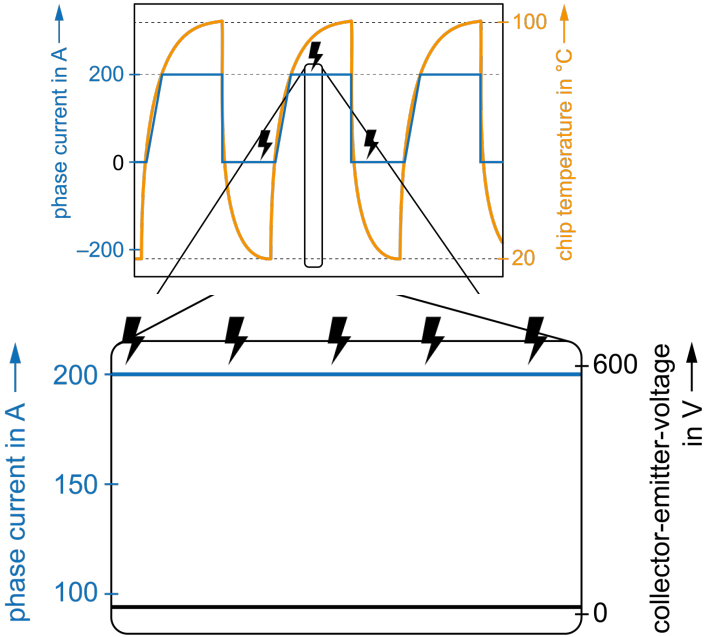
- Versatility of load current profiles
  - Trapezoidal
  - Sinusoidal
  - Drive profile
  - …



TSEP ACQUISTION

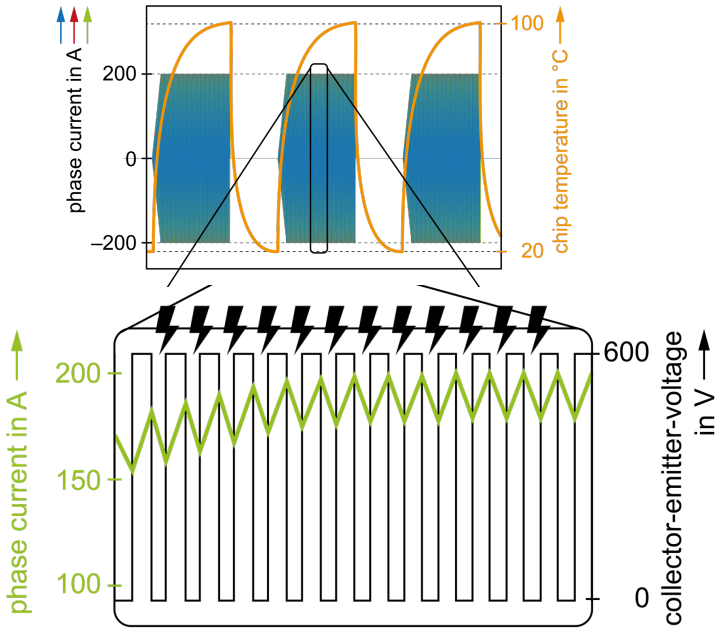
Challenge: AD-Conversion

STATIC POWER CYCLING



➔ AD-conversion possible at arbitrary time instances

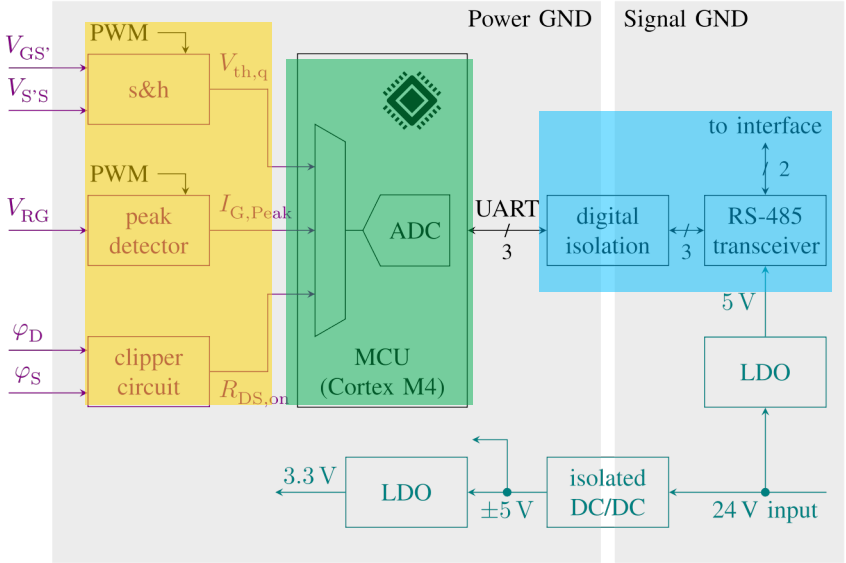
DYNAMIC POWER CYCLING



➔ AD-conversion dependent on switching state

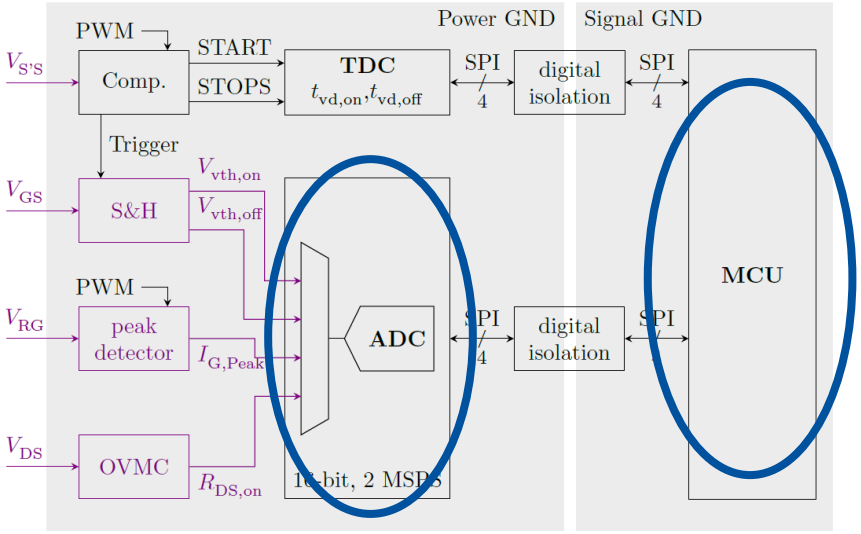
Acquisition Concepts – System Overview
Processing Unit On…

MCU ON POWER GROUND / ON DEVICE POTENTIAL



- 1 MCU per DUT + 1 main MCU
- Free choice of communication protocol
- Slow (half-duplex) but robust

MCU ON ISOLATED POTENTIAL / ON SIGNAL GROUND

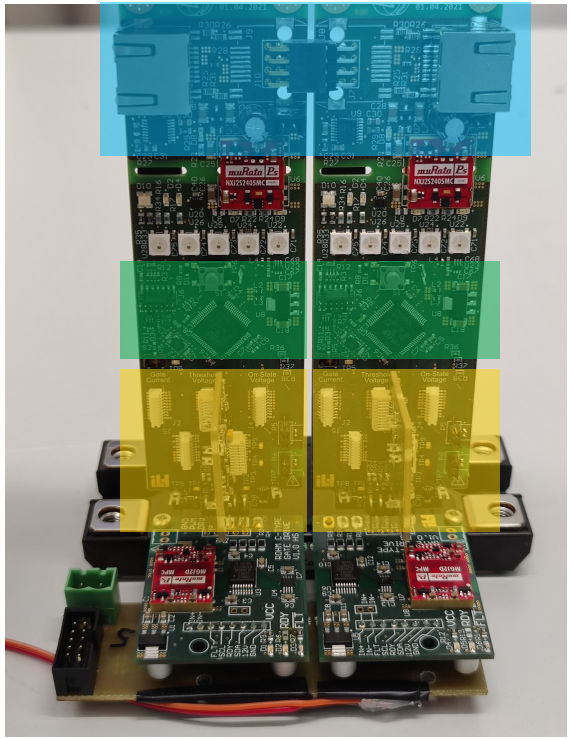


- 1 MCU for multiple DUTs
- Communication protocol dictated by ADC
- Challenge: synchronisation of isolated SPI bus

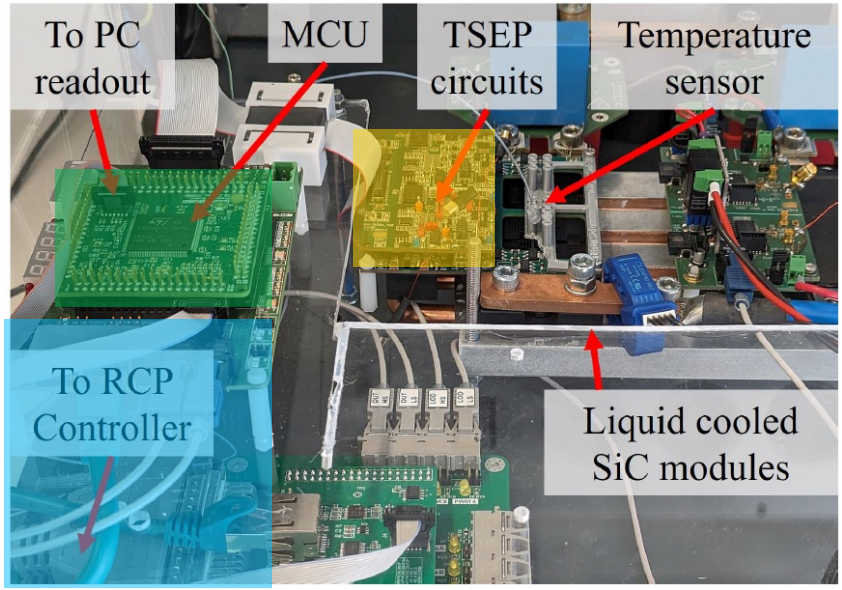
Acquisition Concepts – System Overview
Processing Unit On…

MCU ON POWER GROUND / ON DEVICE POTENTIAL

interface

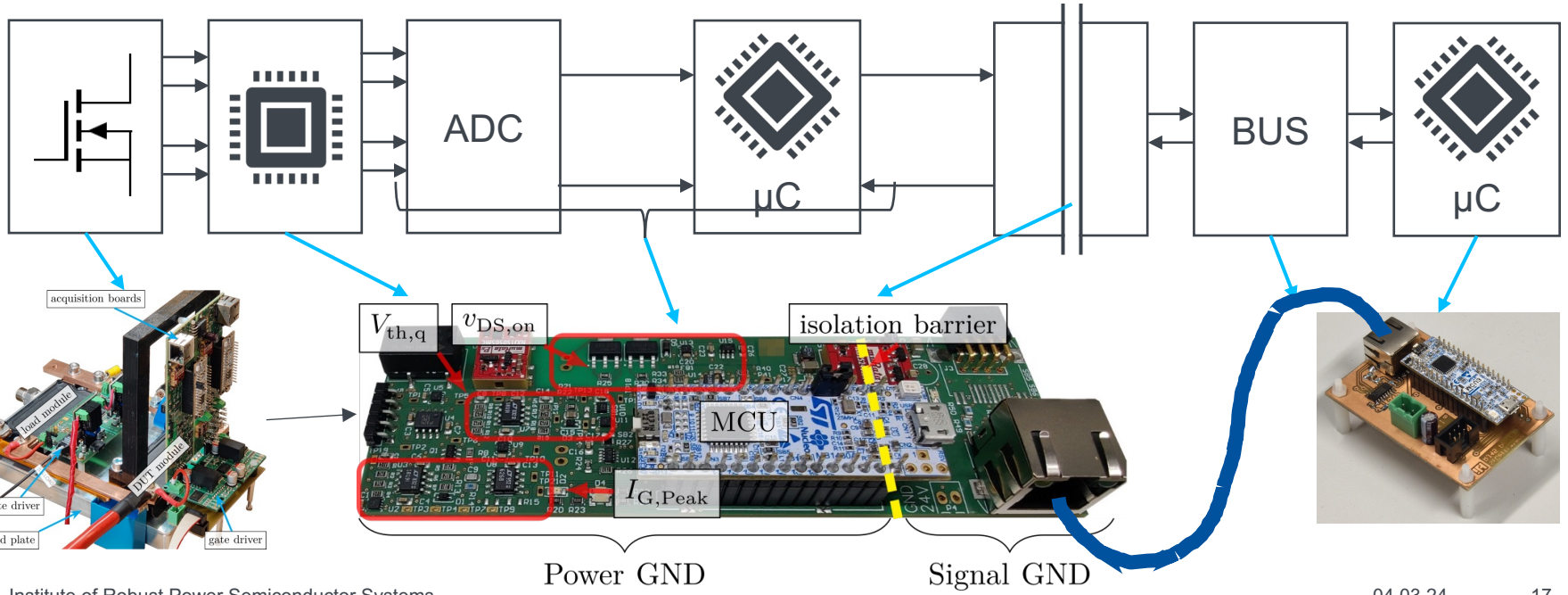


MCU ON ISOLATED POTENTIAL / ON SIGNAL GROUND

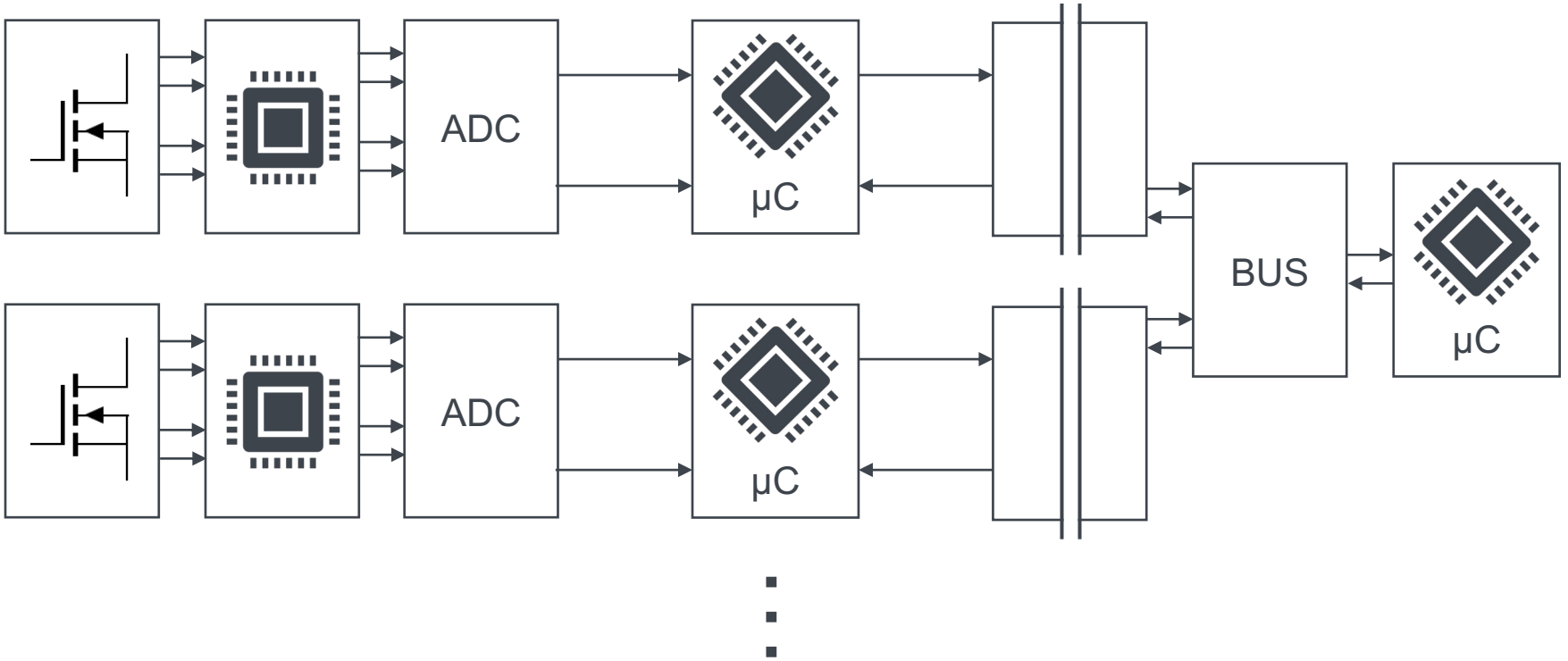


MCU on Power Ground / on Device Potential
Parameter Acquisition

- Connection of TSEP circuits to readout system with isolated supply and communication
- Acquisition of $V_{\mathrm{th,q}}$, $I_{\mathrm{G,Peak}}$ and $R_{\mathrm{DS,on}}$ through multiplexed ADC

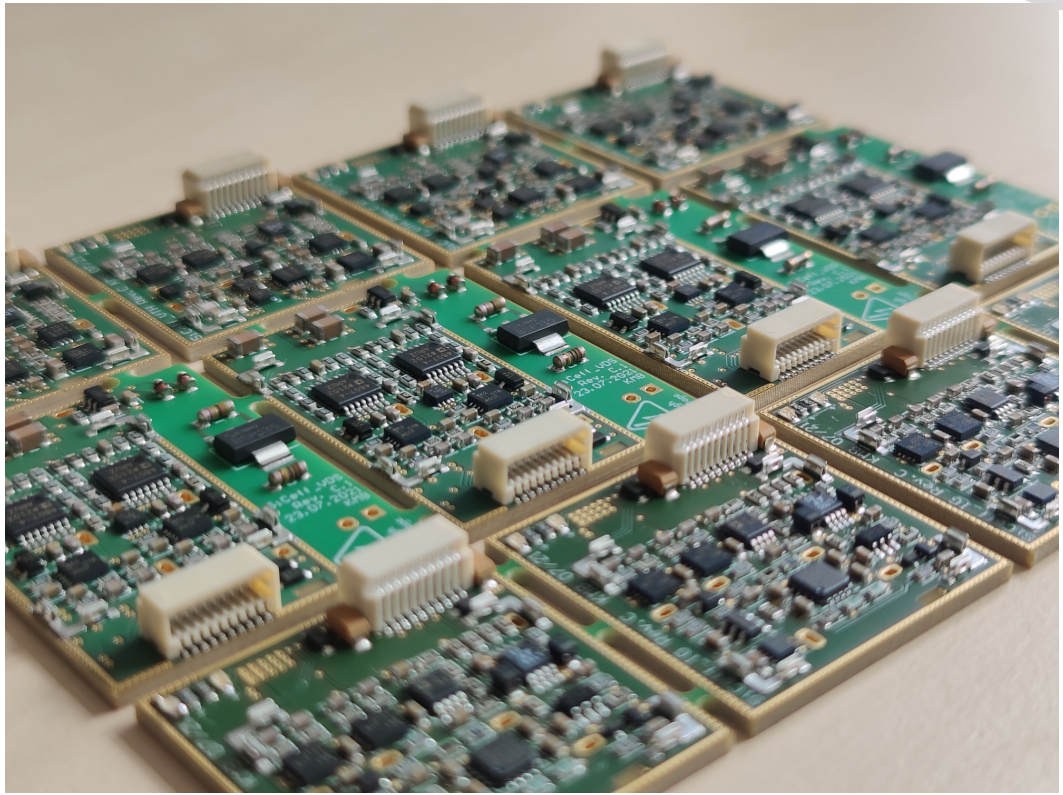


MCU on Power Ground / on Device Potential
Multiple DUTs



MCU on Power Ground / on Device Potential
TSEP Acquisition PCBs

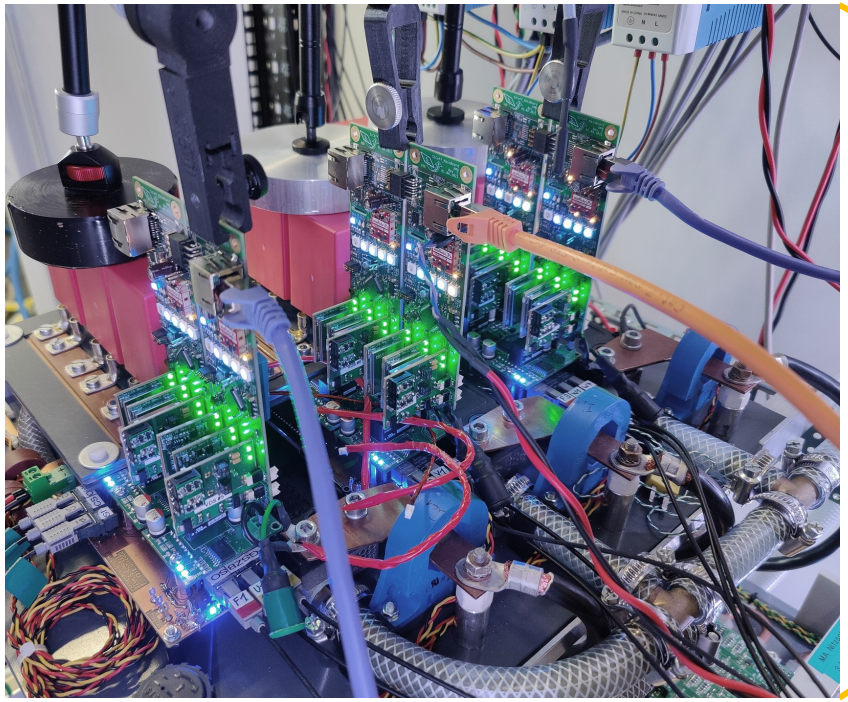
- 6x complete set
- modularity: 3x acquisition boards per transistor

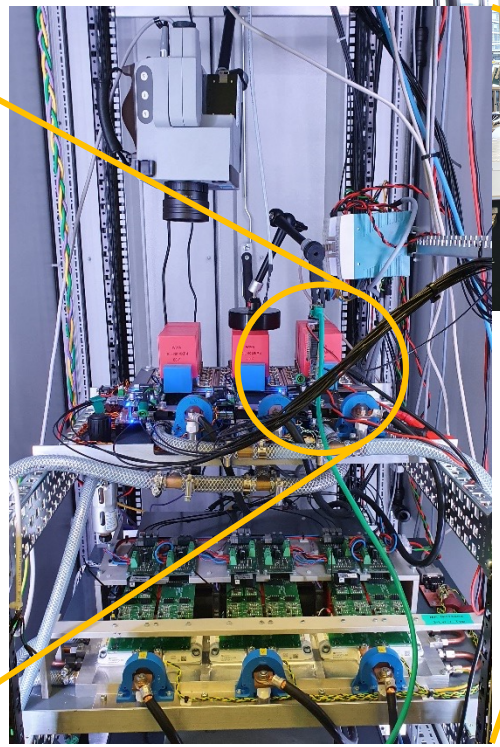


Total

- 18 acquisition boards:
  - 6x $V_{\mathrm{th,q}}$
  - 6x $I_{\mathrm{G,Peak}}$
  - 6x $R_{\mathrm{DS,on}}$
- 6x main board (with µC)

MCU on Power Ground / on Device Potential
Dynamic Active Power Cycler



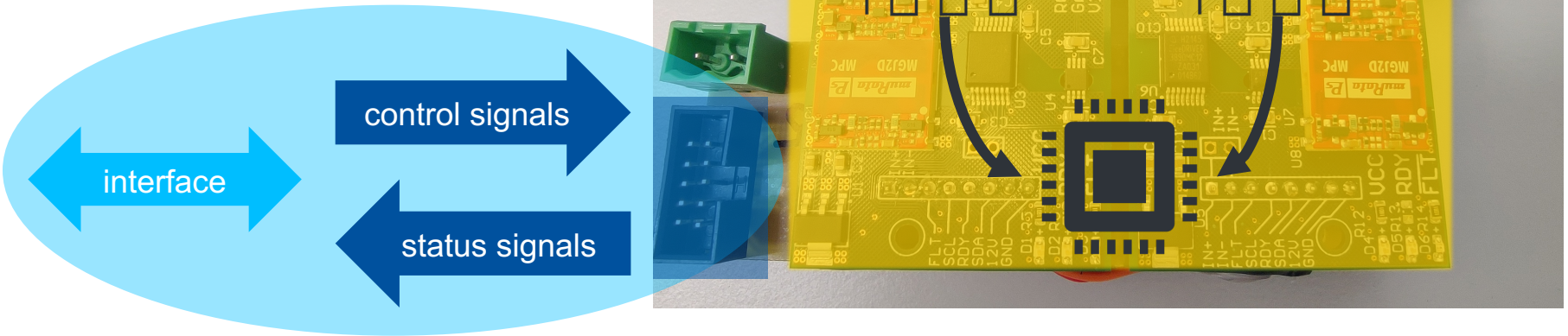


DUT-Inverter

Load Inverter

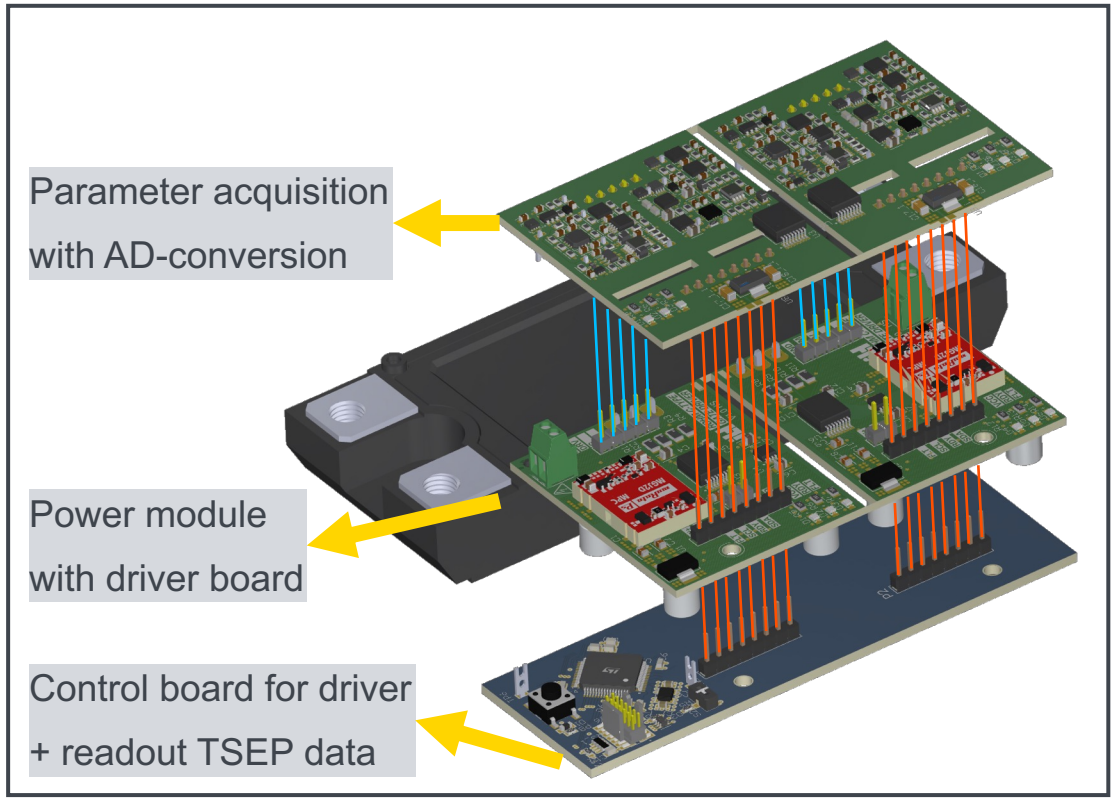
MCU on Signal Ground / on Isolated Potential

- Enables miniaturisation
- Enables stacking of power module – driver board – TSEP board
- 1 MCU per half-bridge
  - ➢ „control center“ with condition monitoring of a power module



MCU on Signal Ground / on Isolated Potential
PCB Stacking

- Plugin-board for parameter acquistion
- Connection to…
  - Device side
  - Signal side
- Control board
  - Sensor data readout
  - If desired, can be replaced by FPGA/MLBX



TSEP Measurements

Measurement of TSEP On-State Resistance

- On-state resistance as an indicator of device aging
- Direct measurement difficult due to high V_{DC}

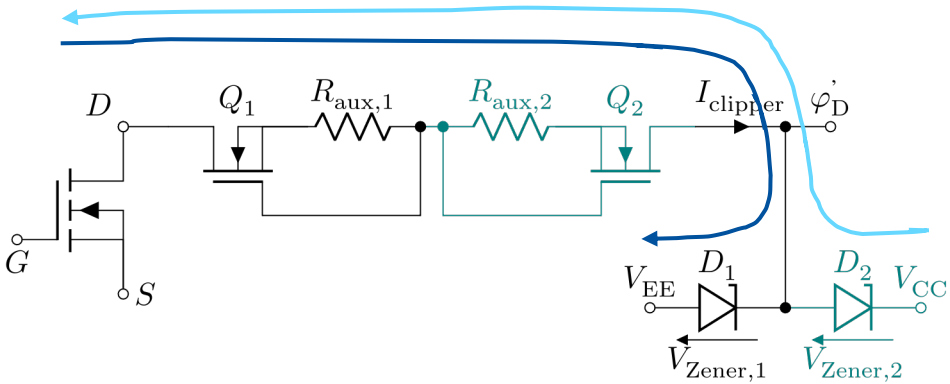
Approach

- Depletion-mode MOSFET based clipper circuit

$$I_{clipper} \approx \frac{V_{th,Q2}}{R_{aux,2}} \quad \text{for } V_{IN} < V_{CC} - V_{Zener,2}$$

$$I_{clipper} \approx \frac{V_{th,Q1}}{R_{aux,1}} \quad \text{for } V_{IN} > V_{Zener,1} + V_{EE}$$

$$\varphi_{D'} \approx \varphi_D \quad \text{otherwise}$$

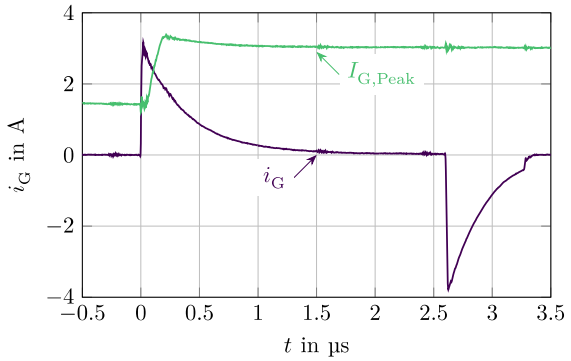


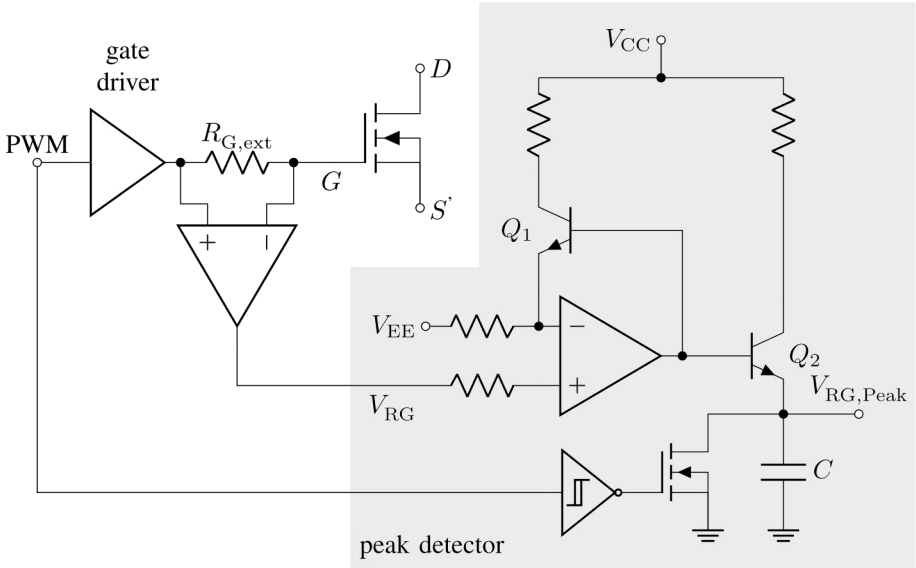
Measurement of TSEP Peak Gate Current

- Indicator of deterioration in the gate path, typically on chip-level

Approach

- Measurement of $V_{\mathrm{RG,Peak}}$





Measurement of TSEP Quasi-Threshold Voltage

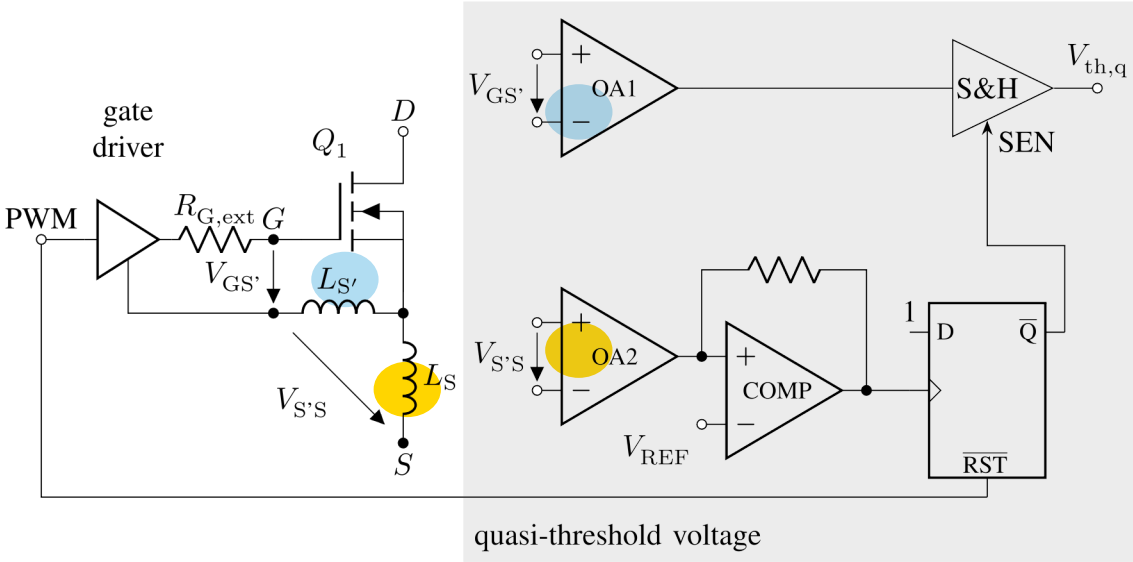
- Indicator of chip-level deterioration
- measurement with conventional methods impractical during operation

Approach

- acquisition of “quasi-threshold“ voltage $V_{\mathrm{th,q}}$

$$V_{\mathrm{TH,q}} \sim \frac{\mathrm{d}I_S}{\mathrm{d}t}$$

- Voltage drop over parasitic inductance as trigger



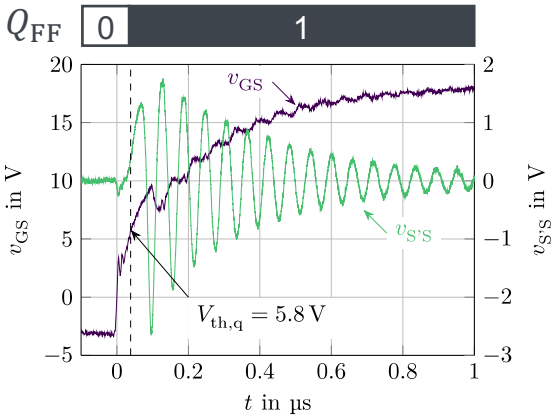
Measurement Results in Inverter Operation

Sweep range
0 – 600 V
10 – 100 A

$V_{\mathrm{GS,on}} = 18\ \mathrm{V}$, $V_{\mathrm{GS,off}} = -3\ \mathrm{V}$, $R_{\mathrm{G,ext}} = 4.7\ \Omega$
$V_{\mathrm{DC}} = 800\ \mathrm{V}$, $I_{\mathrm{D}} = 50\ \mathrm{A}$

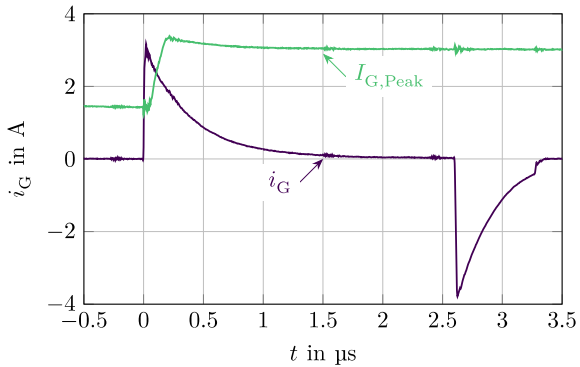
Threshold Voltage

- acquisition during turn-on
- $V_{\mathrm{th,q}} = 5.8\ \mathrm{V}$



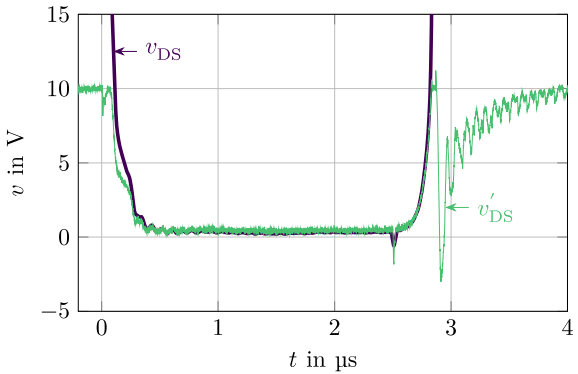
Gate Current Peak

- acquisition during on-state
- limited bandwidth due to low offset output amplifier
- $I_{\mathrm{G,Peak}} = 3\ \mathrm{A}$



On-State Resistance

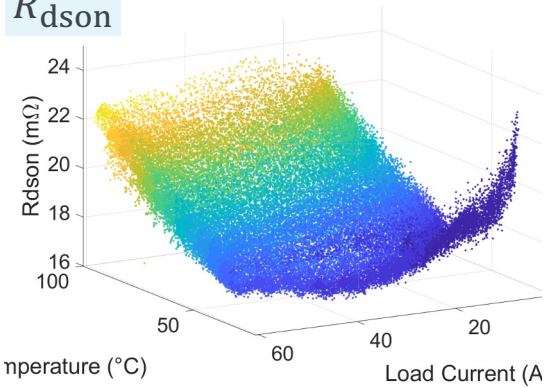
- acquisition during on-state
- < 1 µs after turn-on
- $V_{\mathrm{DS,on}} = 1.3\ \mathrm{V}$



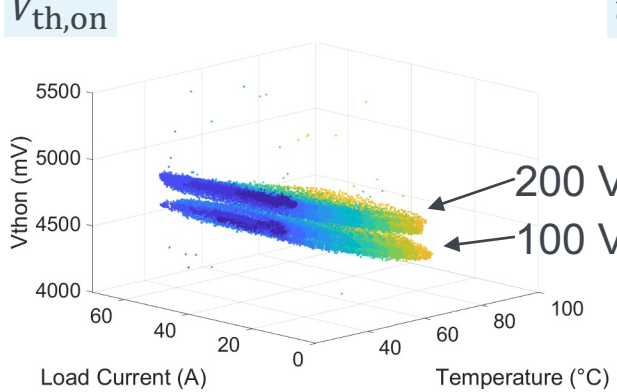
MULTIPLE TSEP SENSOR FUSION

Multiple TSEP Measurements
50000 data points within approx. 1h

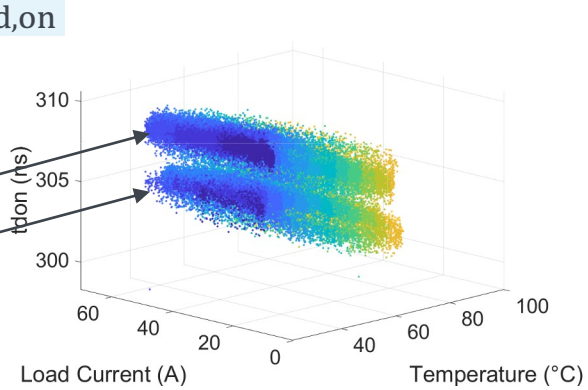
R_{dson}



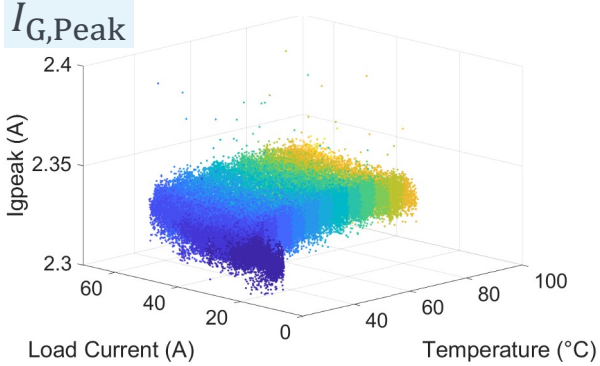
$V_{\mathrm{th,on}}$



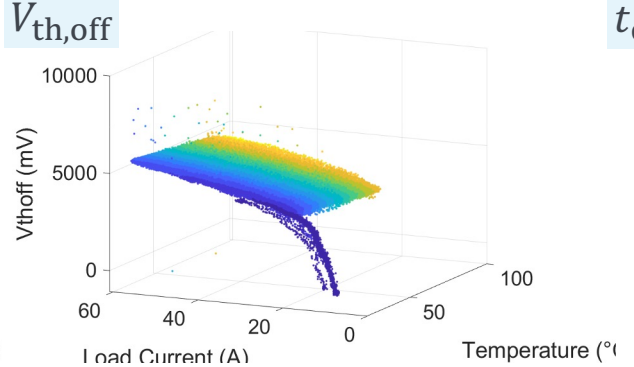
$t_{\mathrm{d,on}}$



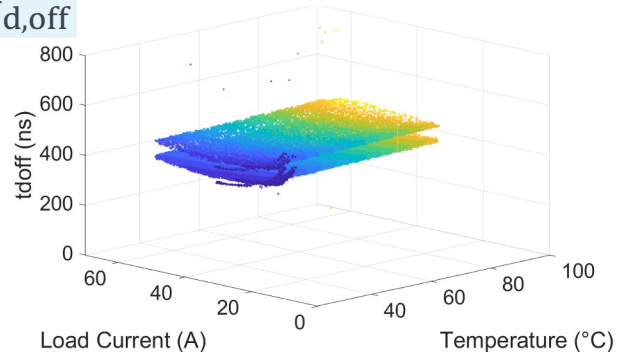
$I_{\mathrm{G,Peak}}$



$V_{\mathrm{th,off}}$

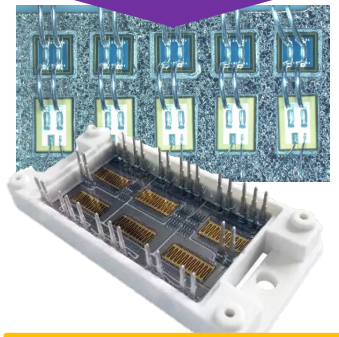


$t_{\mathrm{d,off}}$



Condition Monitoring of Power Semiconductor Devices and Modules
Motivation for Machine Learning

control & drivers



sensing & readout electronics

- Temperature sensor
- R_{th}
- TSEPs
  - R_{on}
  - V_{sd}
  - $V_{th,\ on/off}$
  - $t_{on/off}$
  - $I_{g,peak}$

parameter acquisition & data processing

- Degradation
- Temperature estimation
- Combined TSEPs sensor fusion

TSEPs carry information on temperature and degradation

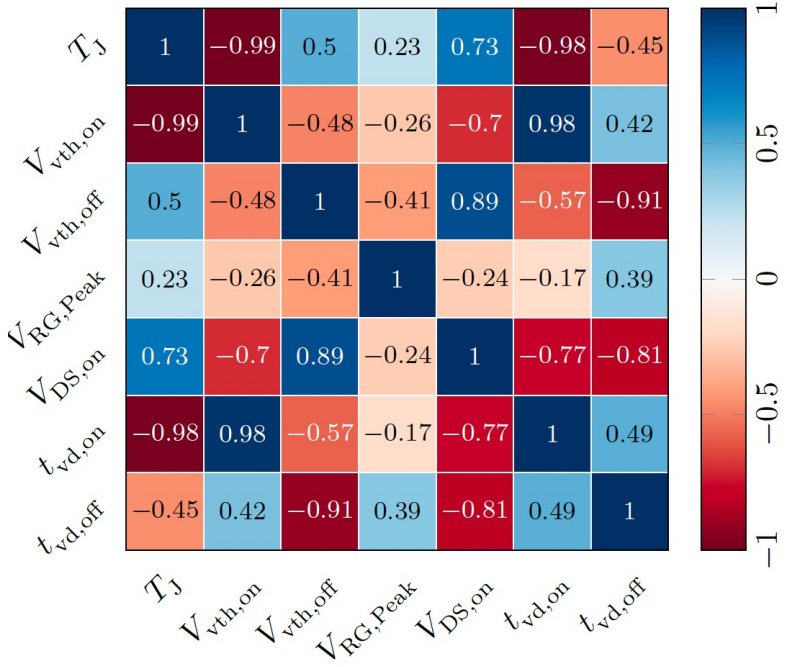
- are correlated
- have multiple dependencies (current, voltage, temperature)
- are degradation sensitive (DSEP)
- require frequent calibration

ML and AI

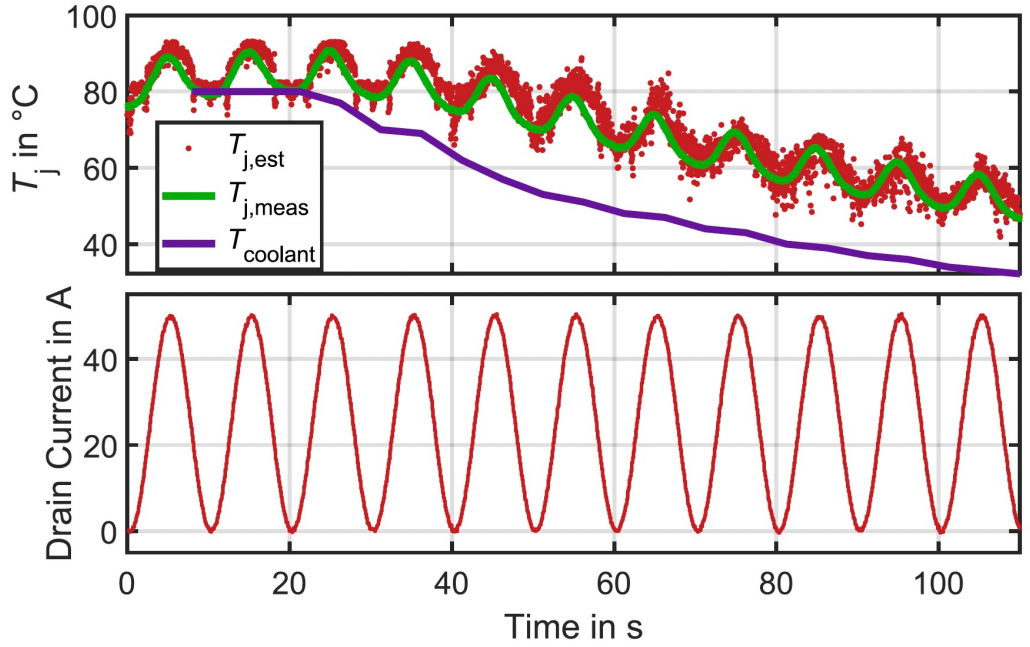
- can use raw or filtered data
- can make use of data augmentation
- can increase linearity, robustness, fidelity, ...
- can distinguish TSEP from DSEP

Machine Learning Based Sensor Fusion for Junction Temperature Estimation

- Correlation of TSEPs

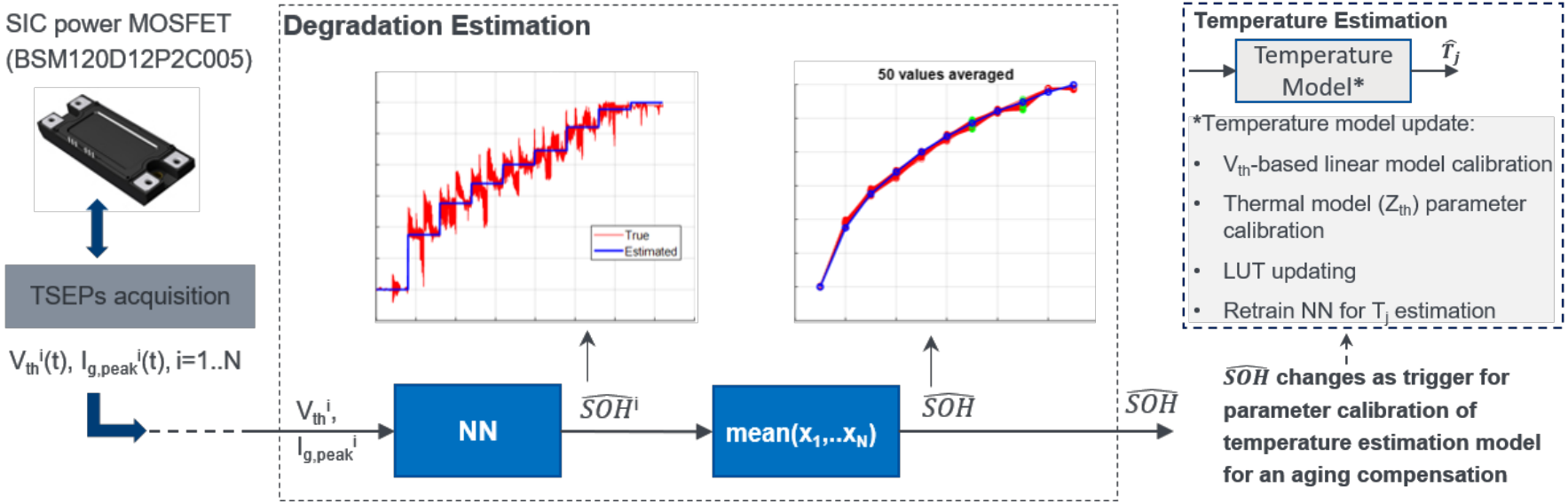


- ML-based temperature estimation



Online Degradation Detection and Estimation of SiC Power MOSFET based on TSEP

Combination of two TSEPs (V_{th}, $I_{g,peak}$) acquired under different temperature and operational conditions throughout the aging process to estimate degradation status via ANN



Outlook

Outlook / Quo vadis?

- Parallelisation of muliple dAPCs
- dAPC tests of novel SiC power MOSFETs
- Extension of dAPC to GaN power transistors
- Increased degree of automisation
- Cloud access
- Online state-of-health monitoring during real drive profiles
- Parameterised drivers
- More extensive use of ML/AI

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Thank you!

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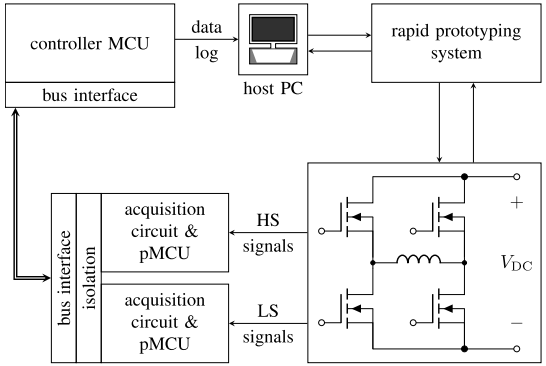
Code Overview - Device Potential

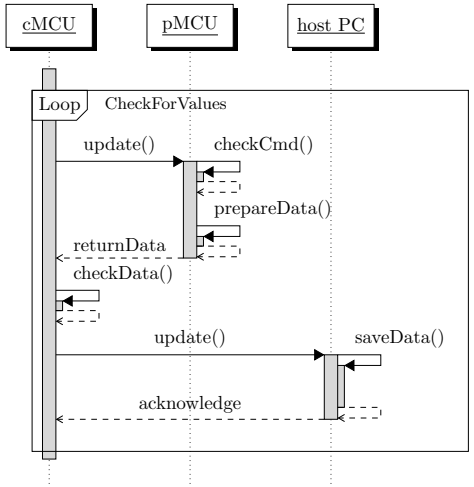
Goal

- Provide accurate data for health monitoring
- Lay the ground-work for further analysis by providing increased amount of data

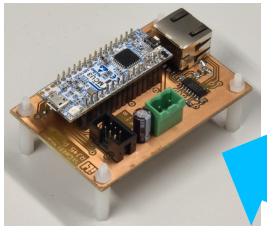
Approach

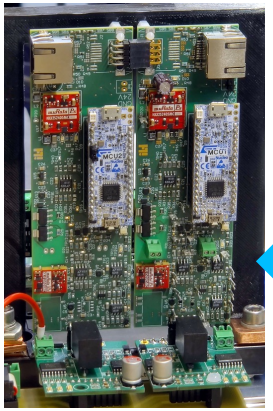
- Isolated acquisition
- Measurement in operation & in real time
- Simultaneous implementation on multiple transistors

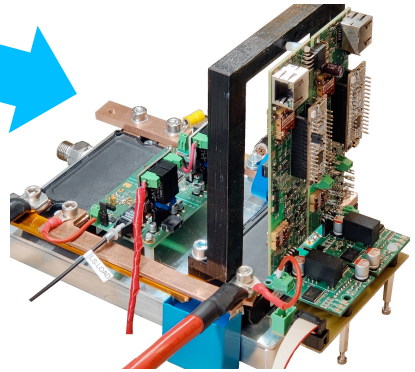


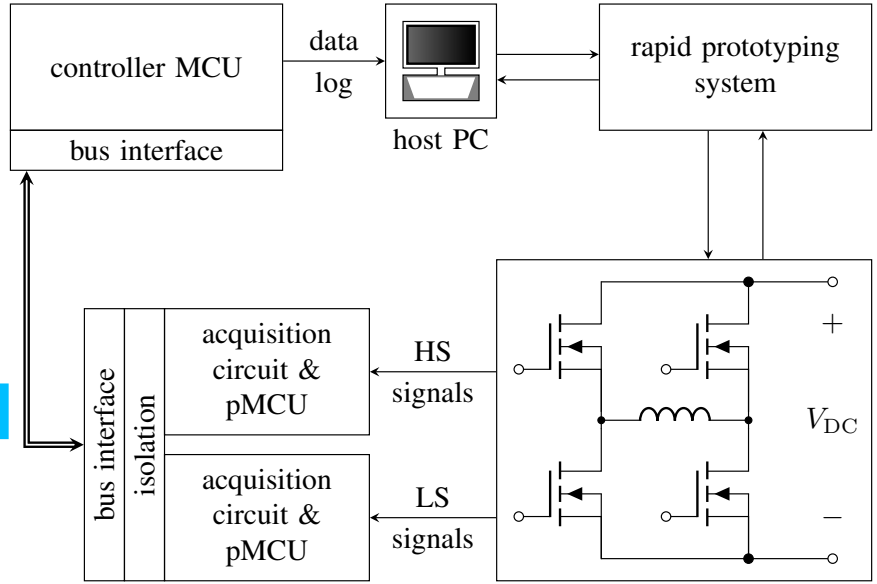


Dynamic Active Power Cycling
System Overview



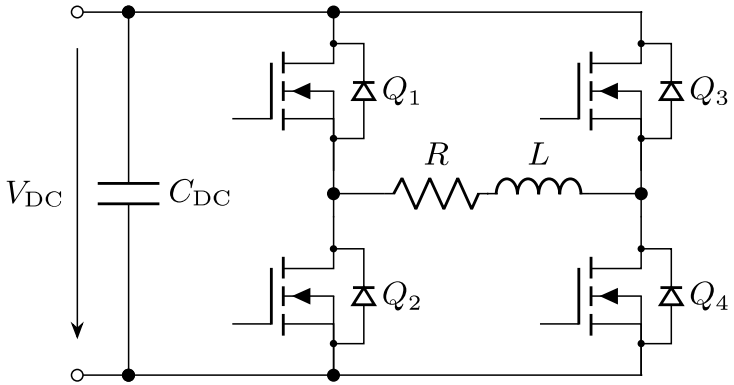


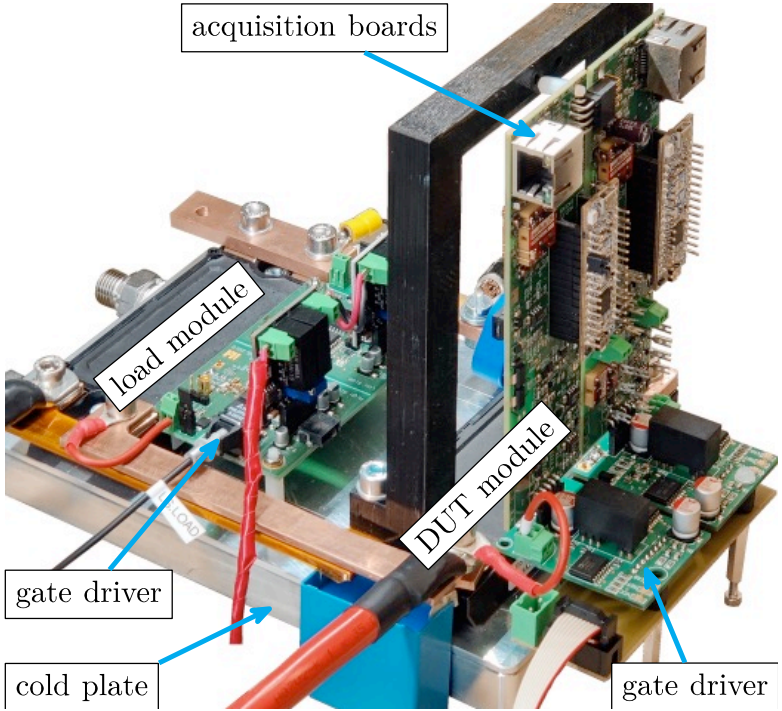




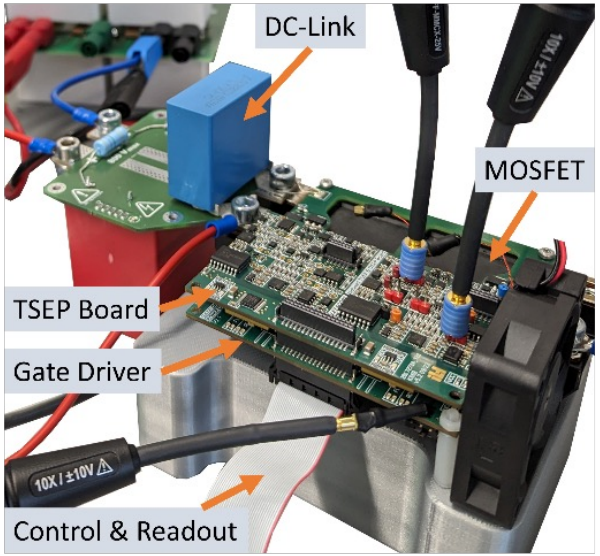
Dynamic Active Power Cycling Tests (dAPC)
Single-phase Prototype Inverter using two SiC Modules

- 1.2 kV 120 A SiC half-bridge module as DUT
- acquisition board connected directly to power module
- $V_{\mathrm{GS,on}} = 18\ \mathrm{V}$, $V_{\mathrm{GS,off}} = -3\ \mathrm{V}$, $R_{\mathrm{G,ext}} = 4.7\ \Omega$,

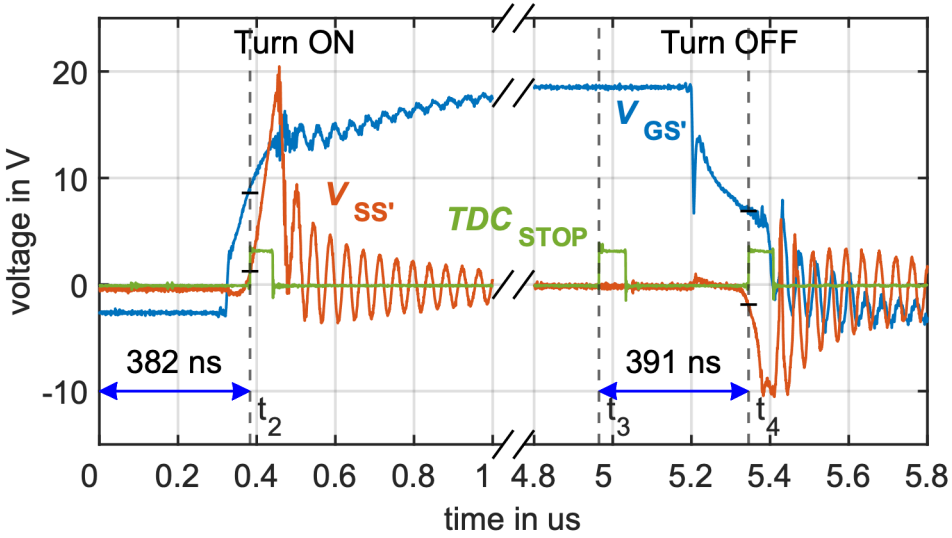




Calibration of the TSEP Sensor Board



setup of TSEP board connected directly to the gate driver of a $\mathbf{1.2\ kV}$ / $\mathbf{120\ A}$ SiC half bridge module.



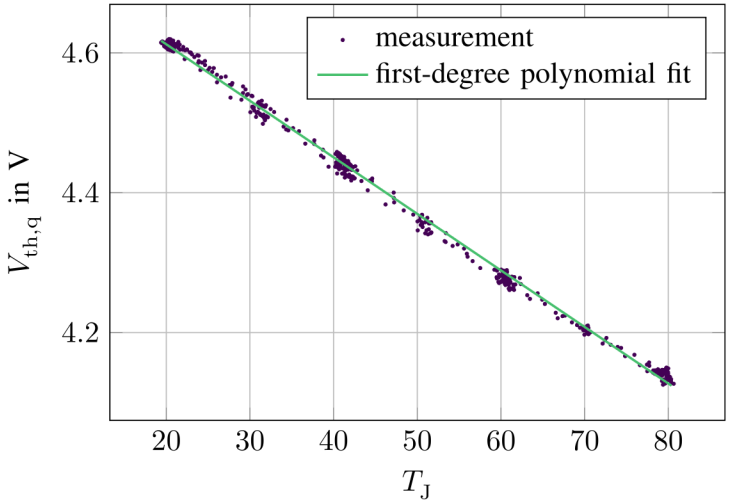
Turn ON & OFF waveform at $\mathbf{400\ V}$ / $\mathbf{100\ A}$, $\mathbf{25\ °C}$.

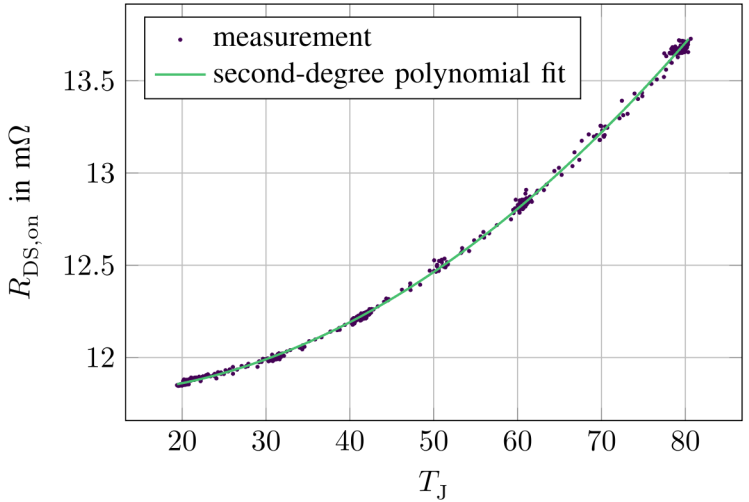
Parameter sweep (0 – 600 V & 10 – 100 A)

Calibration

Temperature Dependency $V_{\mathrm{th,q}}$ and $R_{\mathrm{DS,on}}$ in Operation

- Buck converter mode at $V_{\mathrm{ZK}} = 400\,\mathrm{V}$, $I_{\mathrm{D}} = 100\,\mathrm{A}$

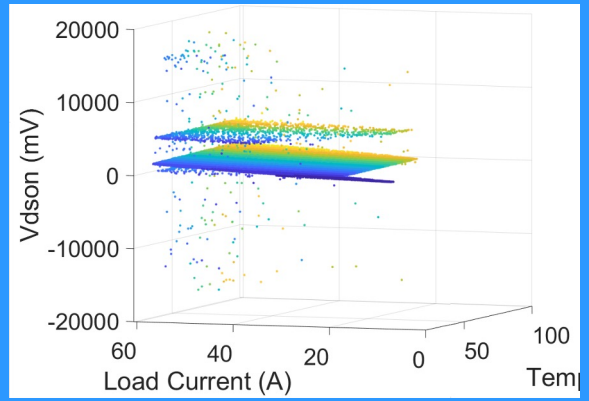




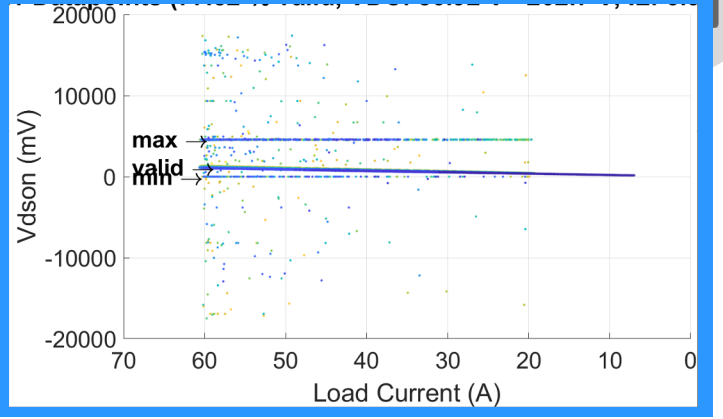
Parameter	*absolute sensitivity*	*relative sensitivity*
$V_{\mathrm{th,q}}$	$-8.1\,\mathrm{mV\,K^{-1}}$	$-1.9\,‰\,\mathrm{K^{-1}}$
$R_{\mathrm{DS,on}}$	$9.8\,\mu\Omega\,\mathrm{K^{-1}}$ to $52\,\mu\Omega\,\mathrm{K^{-1}}$	$0.77\,‰\,\mathrm{K^{-1}}$ to $4.1\,‰\,\mathrm{K^{-1}}$

TSEP Measurements – Data Filtering – Example $R_{ds,on}$

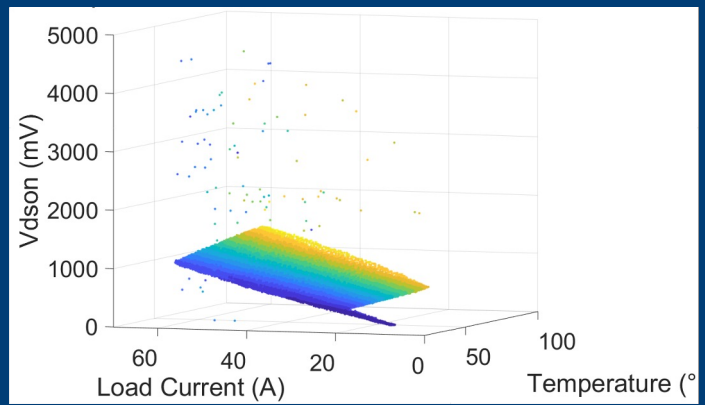
raw data



raw data



AD-conversion range



final values