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The Maximally Efficient Amplifier

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The energy efficiency of an RF front-end (RFFE) is a vital characteristic, whether a radio is battery or mains powered. For battery powered, reducing the maximum current drawn from the battery increases the time between charges. For mains powered, important properties such as size, weight and power are dictated by the RFFE efficiency. Consequently, many amplifier architectures and inventions have been developed to minimize wasted energy in the transmitter. Although improving efficiency, some of these rely on theoretically impossible modes of operation, and some fail to fully use the device's capabilities.

This article provides some analysis of and insight into amplifier efficiency. First, the tuned amplifier concept and efficiency enhancing mechanisms are explained. Then, the effects of each mechanism on amplifier efficiency are illustrated, revealing some surprises. The better known methods for improving amplifier efficiency are classified by their mechanisms—also noting the mechanisms not used—and identifying areas for improvement. Finally, the article shows that harmonic load-pull measurements on a device highlight its potential; using such measurement data with a look-up table, for example, amplifier performance in a variety of schemes can be predicted.

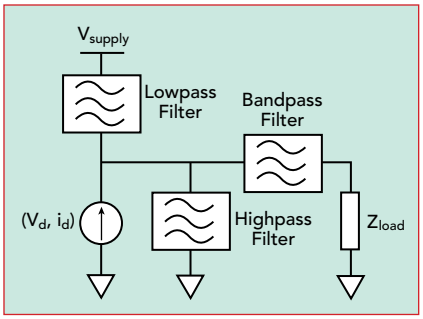


Fig. 1 **Simplified schematic of a tuned amplifier, class A to C.**

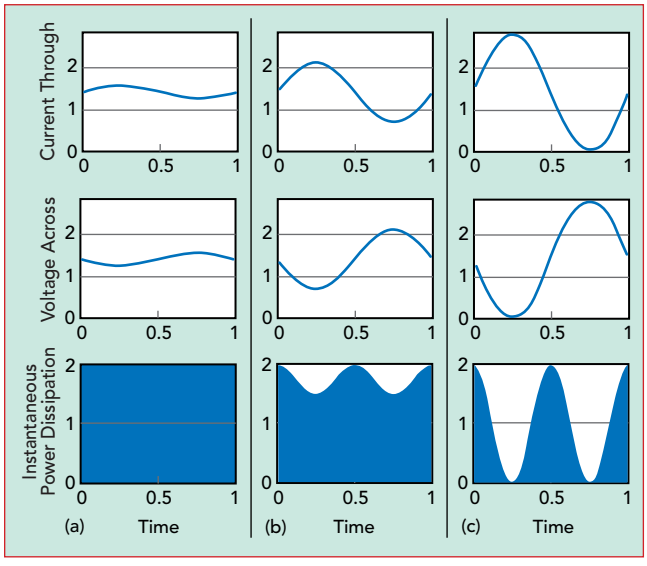
THE TUNED AMPLIFIER

A tuned amplifier circuit can be used to describe the continuum of amplifier class characteristics from A to C, via AB and B, based on sinusoidal voltage waveforms and quasi-linear operation. A more detailed explanation is provided in Chapter 3 of Cripps' book.[1] A simplified model of the power amplifier built around a controlled current source is shown in ***Figure 1***. The model can be simplified into three frequency domains:

- DC current flows through the lowpass filter and the controlled current source (i.e., the device). Its progress elsewhere in the circuit is blocked by the bandpass and highpass filters.

- At the fundamental frequency, the signal current through the device passes solely to the intended load impedance (Z_{load}), creating a voltage across the device and load.
- Harmonic currents flowing through the device are short circuited through the highpass filter, as any harmonic currents flowing in the device "see" zero impedance and do not create any voltage.

The voltage across the device comprises only DC and fundamental components and is sinusoidal. Power is dissipated by the device when a current (i_d) flows through it with a voltage (v_d) across it and where the current and voltage overlap during the waveform cycle. For a class A amplifier, the simplest case, ***Figure 2*** shows the power dissipation versus time at three power levels. As the output power reduces, the power dissipated waveform tends to a constant value. At higher output power, the dissipated power reduces. The power consumption is constant in all cases, and the power dissipated is the total area under the power dissipation curve. In the case of this class A amplifier, the amount of power dissipated (wasted) decreases as output power level increases, from (a) to (c).



▲ Fig. 2 **Class A amplifier waveforms at low (a), medium (b) and high (c) output power.**

EFFICIENCY ENHANCEMENT

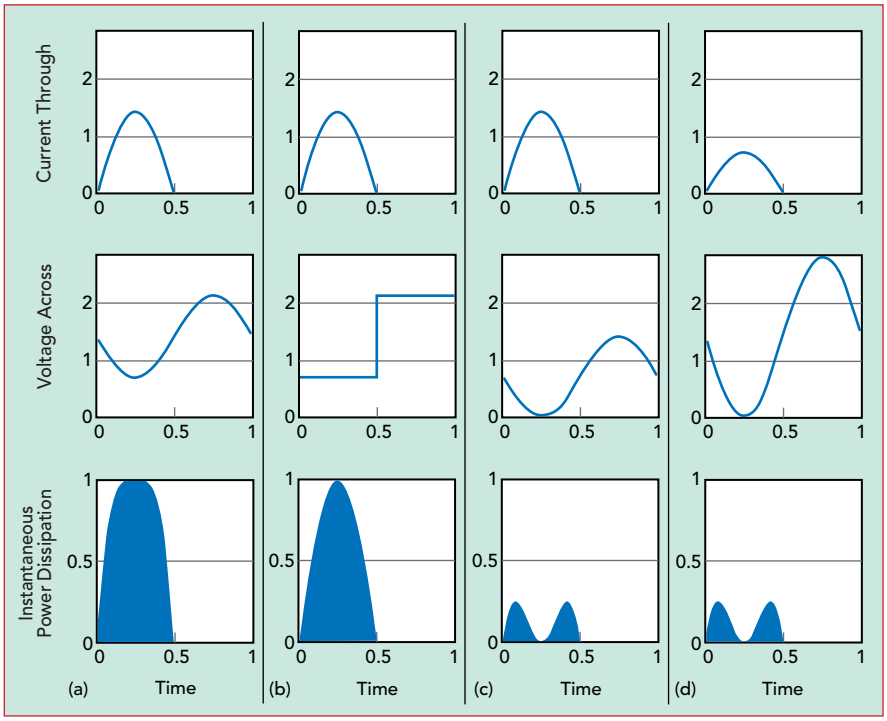
How will efficiency enhancement mechanisms improve the energy efficiency? Consider classifying the mechanisms for reducing the wasted power in a tuned amplifier. These mechanisms relate only to the device itself, not to external modulating circuitry such as harmonic terminations or modulators. Three base mechanisms can enhance the efficiency of a single-ended amplifier: waveform engineering, supply modulation and load modulation.

Waveform Engineering—The shape of the voltage and/or current waveform is modified, which is what happens when passing through the class A to C continuum. Harmonic content is introduced into the current, modifying its waveform, in a predictable but restricted way.[1] Alternatively, the ratio of the current's harmonic content may be modified by injecting harmonics from either the input side or output side. For the current's harmonic content to affect the voltage waveform, a non-zero impedance must be present at that harmonic frequency. In the limiting case, both current and voltage waveforms are square waves and antiphase. As one of them is zero at any instant in time, the power dissipation is zero. This zero dissipation applies at least to the device, but it could just be shifted elsewhere in the system.

Supply Modulation—The average or envelope supply voltage across the device, V_{supply}, is modified. With a perfect device, V_{supply} is the root-mean-square value of the voltage waveform, set so the minimum value of vd reaches zero.

Load Modulation—The Z_{load} presented to the device at the fundamental frequency is modified, ideally so the voltage (vd) swings from 0 to 2 times the supply.

Figure 3 illustrates these mechanisms using a class B waveform as the reference. The class B current waveform is half sinusoidal, compared to fully sinusoidal for class A operation. The fundamental current is equal in both classes A and B when the peak-to-peak current variation is equal. The reason for using a class B waveform as the baseline is because the efficiency can be enhanced by all three methods. Class A, on the other hand, cannot be improved with load modulation alone: class A power consumption remains constant regardless of the load impedance.



▲ Fig. 3 **Efficiency enhancement mechanisms compared to a class B waveform at 6 dB back-off (a), waveform engineering (b), supply modulation (c) and load modulation (d).**

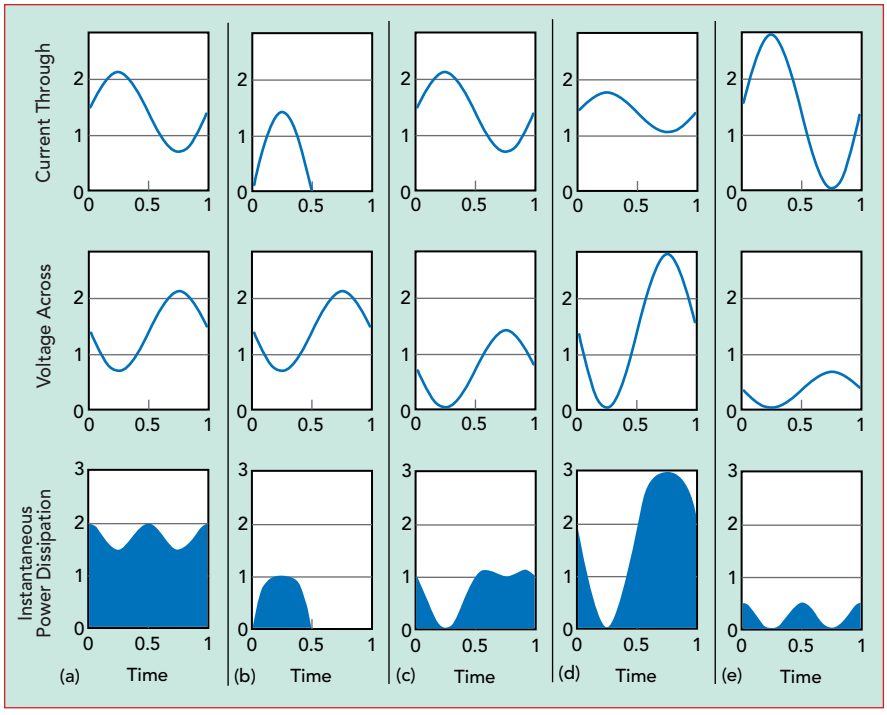


Fig. 4 **Class A amplifier efficiency at 6 dB back-off (a) enhanced by waveform engineering (b), supply modulation (c), load modulation (d) and an unexpected improvement using a counter-intuitive hybrid (e).**

TABLE 1

APPROACHES TO INCREASE CLASS A AMPLIFIER EFFICIENCY

Configuration	*% Efficiency at 6 dB Back-Off (25% of Rated Power)*
Class A Baseline	12.5
Waveform Engineered (Equivalent to Class B)	39.3
Supply Modulation	25.0
Load Modulation	12.5
Anti-Load & Supply Modulation	50.0

Class A Case Study

One of the goals of this article is to illustrate efficiency enhancement mechanisms so they can be used optimally. The class A case is not a lost cause. ***Figure 4*** shows the voltage, current and dissipation for a class A amplifier, illustrating that waveform engineering and supply modulation enhance efficiency, but load modulation does not. Waveform engineering can convert the class A sinusoidal current into the class B case of the half sinusoid in Fig. 4(b). Referring to Figure 3, class B efficiency could now be enhanced with load modulation.

What if the device could not be waveform engineered to add the required harmonics? For example, it might be operating close to its upper frequency limit and cannot support the harmonic currents. Supply modulation in Fig. 4(c) could be used, although combining it with load modulation would be counterproductive. Load modulation increases the peak-to-peak voltage, decreasing the range where supply modulation could be deployed. Turning the problem around, if load modulation degrades the effectiveness of supply modulation, what if "unload" modulation were applied? Instead of maximizing the load impedance to maximize peak-to-peak voltage, minimize the load impedance to minimize the peak-to-peak voltage and then use supply modulation. This is the case shown in Figure 4(e), the "anti-load modulation + supply modulation" case. The peak-to-peak values of current and voltage have been completely reversed from the load modulation case, and supply modulation has been applied—achieving a quite unexpected result: the efficiency at the output power back-off of the class A amplifier has been maintained at the theoretical maximum of 50 percent.

The respective efficiencies of the five scenarios of Figure 4 are summarized in ***Table 1***. Note that the waveforms all have the same output power.

POPULAR APPROACHES

Having classified various enhancement mechanisms and discussed their effects on theoretical amplifier blocks, including advantageous effects from hybrid approaches, the discussion moves from theory to practice, classifying the popular enhancement methods according to the mechanisms they use (see ***Figure 5***). Using a Venn diagram for classification helps identify where additional schemes are complementary and may further improve efficiency.

For example, the Doherty amplifier, which applies load modulation to its constituent amplifiers, can be improved by adding supply modulation, especially to the main channel, and/or waveform engineering, by modifying the design to incorporate class F^{-1} operation, for example.

Harmonic Load-Pull

A bottleneck is getting real world, practical devices to use the theoretical enhancements. For example, a typical GaN device may be sensitive to efficiency enhancement by load modulation over a 5–10:1 impedance range. However, when used as the main device in a Doherty architecture, it is typically exploited only over a 2–3:1 range. The Doherty scheme will fail to maximize the potential performance of the device.

Harmonic load-pull measurements over a range of bias conditions make it possible to establish the maximum performance envelope for the device technology. Load-pull data can be obtained using various setups, such as Maury Microwave's harmonic load-pull test bench with an R&S ZNA vector network analyzer (see ***Figure 6***). By comparing harmonic load-pull measurement data with the theoretical

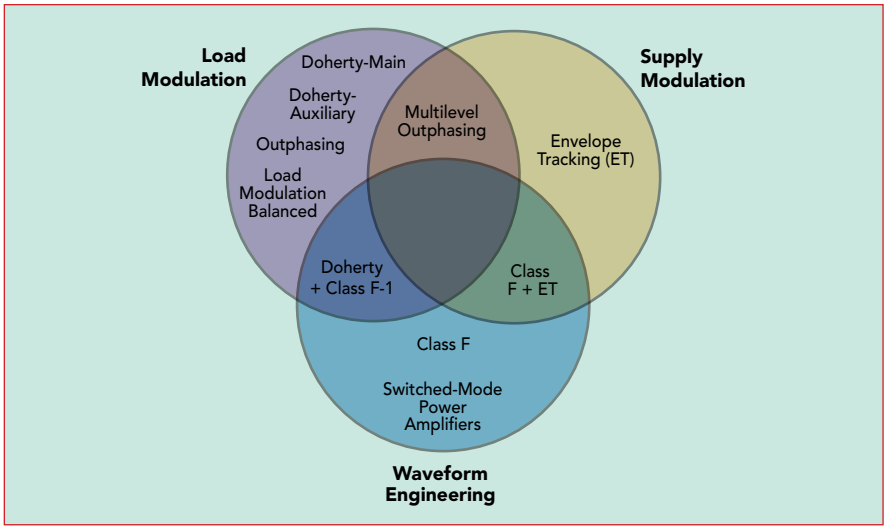


Fig. 5 **Efficiency enhancement mechanisms, their hybrids and possible areas for further improvement.**

Fig. 6 **Maury load-pull test system using the R&S®ZNA VNA.**

performance of a selected high efficiency technique, the performance gap can be quantified, answering the question of the difference between what has been built and the performance limit. Alternatively, if the device is assumed to be the bottleneck, the harmonic load-pull measurement data enables a scheme to be designed to maximize its potential, using the optimal enhancement mechanisms in the correct proportions.

Thus there are several ways to use the data from a rigorous and repeatable setup for measuring load-pull. One is to create characterization and architectural databases for cross-referencing device performance with various circuit architectures and enhancement methods: Doherty, load modulated, balanced, outphasing, etc. The design flow of ***Figure 7*** shows possible steps for setting up and using a look-up table for assessing device performance and enhancement techniques. To illustrate the concept, a commercially available Wolfspeed GaN transistor (CG2H40010) was characterized at a fundamental frequency of 2 GHz and a bias current of 100 mA using a Maury harmonic load-pull test bench. The measurement data was analyzed to understand device performance in a Doherty amplifier, then compared with the maximum performance possible from the device. ***Figure 8*** shows the output power and drain efficiency as the input power, fundamental and harmonic terminations and supply voltages were swept. This scatter plot provides the performance limit of a single-ended device; to achieve drain efficiency greater than 50 percent, the dynamic range of the output power approaches 15 dB.

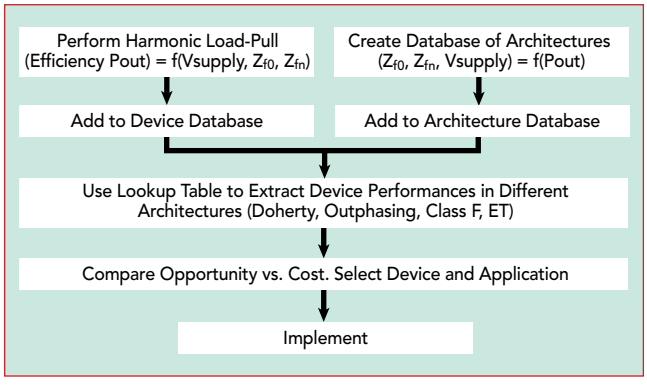


Fig. 7 **Process flow to achieve the best device-architecture pairing.**

For a Doherty amplifier, the (simplified) relationship between output power and impedance is defined by:

$i_{aux} = 2i_{main}-1$, where i_{main}, the normalized output current from the main transistor, varies from 0 to 1.

$i_{aux} = 0$ where $i_{aux} < 0$. i_{aux} is the normalized output current of the auxiliary device.

The normalized impedances presented to the main and auxiliary transistors are

$Z_{main} = 2 - i_{aux}/i_{main}$ and $Z_{aux} = 1/(i_{aux}/i_{main})$, respectively.

The output power contributions from the constituent amplifiers are given by

$P_{main} = i_{main}^2 \times Z_{main}$ and $P_{aux} = i_{aux}^2 \times Z_{aux}$

In this Doherty example, a theoretical output current relationship is used, although the equation relating i_{aux} and i_{main} can be changed, using a square law auxiliary relationship for example, where $i_{aux}=\sqrt{i_{main}}$. The impedance values Z_{main} and Z_{aux} may be scaled to any value in the dataset. In this case, 10 Ω is used as a multiplier prior to the look-up operation; fixed values for the harmonic impedances have also been chosen prior to look-up. With the definition for output power and impedance for the main and auxiliary devices, the look-up-table operation is performed on the measurement data to extract the drain efficiency, with interpolation of the measurements used to determine intermediate values.

With the output power and drain efficiency for the main and auxiliary known individually, the composite power consumption and output power can be calculated. The simulated output power and drain efficiency of the Doherty power amplifier is plotted in ***Figure 9***, using the measured data for the look-up operation. Because two devices are used in a Doherty, the output power capability is 3 dB higher, so a second scatter plot of the measured data, increased by 3 dB, is included. The second scatter plot represents the performance limit. The load modulation mechanism offered by the Doherty architecture—the limited

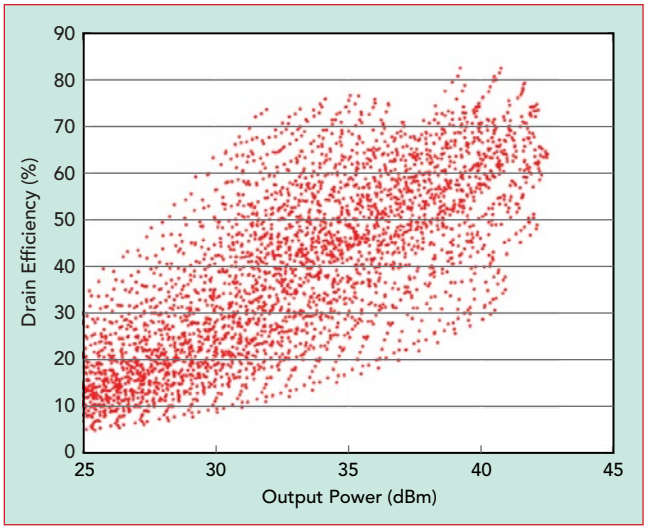


Fig. 8 **Single-ended GaN transistor drain efficiency and output power vs. swept input power, supply voltage (10, 20 and 28 V) and fundamental, second and third harmonic impedances.**

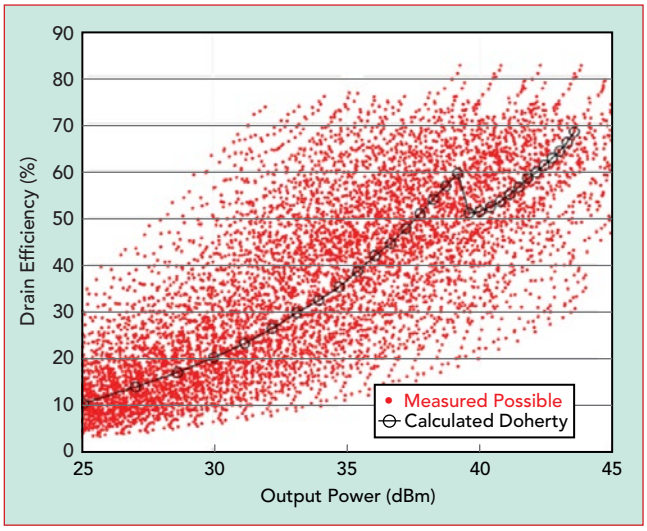


Fig. 10 **Calculated drain efficiency and output power vs. measured drain efficiency and output power showing full supply voltage and harmonic impedance variations.**

2:1 modulation range presented to the dominant main device, combined with the arbitrary impedance trajectory selected for this illustration—does not fully exploit the device's capability for load modulation. The device is, in effect, being driven in first gear. While the measurement space indicates a capability of 8 dB dynamic range achieving at least 50 percent drain efficiency, the Doherty only manages to exploit about 5 dB of that range, also missing a couple of dB of saturated output power. The same extracted Doherty performance plotted on the entire measurement space, including the full harmonic and supply variations, is shown in ***Figure 10***. For efficiency of 50 percent or greater, the output power dynamic range is now nearly 18 dB with the addition of the auxiliary transistor's 3 dB contribution. Clearly the performance of the Doherty in this example would benefit from the addition of supply modulation and/or waveform engineering.

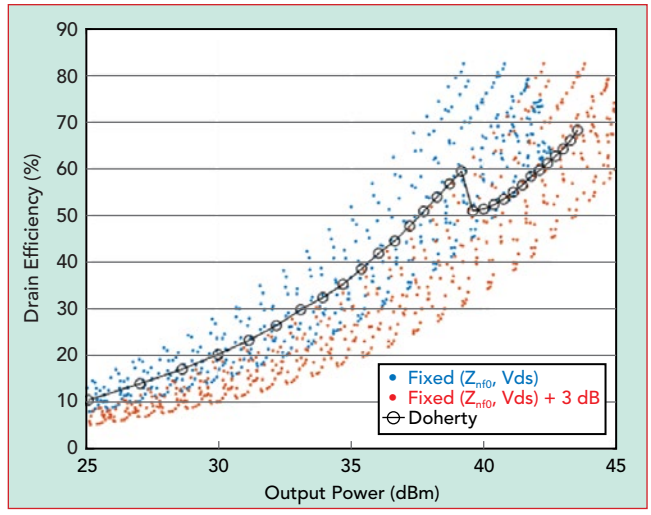


Fig. 9 **Calculated drain efficiency and output power vs. measured drain efficiency and output power with fixed supply voltage and harmonic impedances.**

This model for the Doherty could be more sophisticated, including other effects without detracting from the basic flow. Alternatively, it could be that a different enhancement scheme offers a greater benefit for the device, whether tailored from the ground up or off-the-shelf. Other concepts can be analyzed using different equations and look-up parameters. For example, using the outphasing architecture, the impedances presented to the voltage source devices are derived from the cotangent of the inverse sine of the output amplitude.[1]

CONCLUSION

A classification of efficiency enhancement mechanisms has been proposed, and their effects on class A and class B amplifiers described, allowing for complementary mechanisms to be identified.

It is suggested that harmonic load-pull measurements, over a range of supply voltages, which are analogous to the mechanisms, can fully extract the performance potential of the device.

From those measurements, performance of the device in a range of architectures (e.g. Doherty) can be predicted.

State-of-the-art devices, such as the Wolfspeed device illustrated in this article, are capable of much better performance than state-of-the-art architectures.

Therefore, that designing a "good enough" supply-modulated harmonic load-pull, appropriate for the application at hand, should be a goal for those responsible for developing power efficient RFFEs.■

ACKNOWLEDGMENT

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Reference

1. Cripps, S. C., "RF Power Amplifiers for Wireless Communications," 2006, *Artech House*, Norwood, Mass., Chapter 3.