CONFORMANCE TEST FAILED. WHAT NOW?

Root cause analysis of signal integrity problems on high speed digital buses

Reprint NEWS 225 | Guido Schulze

CONFORMANCE TEST FAILED. WHAT NOW?

Conformance tests are performed on serial data interfaces such as USB, HDMI and PCI Express to ensure interoperability between electronic devices and accessories. In cases where signal integrity problems are encountered, the R&S®RTP oscilloscope supports root cause analysis by providing powerful tools such as eye diagrams, jitter and noise separation as well as time domain reflectometry.

Automatic conformance tests for high speed data interfaces

Conformance tests represent an important milestone during product development. The relevant standardization committees have published detailed test specifications for many interfaces such as USB and Ethernet. Specialized test labs offer complete testing services for such interfaces, including documentation and certification. For users who need to perform these tests on their own, the R&S®RTP provides automated test solutions for all common interface standards. These solutions are equipped with graphical measurement configuration tools and off-shelf test sequences. No matter how the testing is performed: If results do not comply with the standard, time-consuming debugging is required.

Fig. 1: Conformance test for USB 3.2 Gen 1 with the R&S®RTP164 oscilloscope (16 GHz).

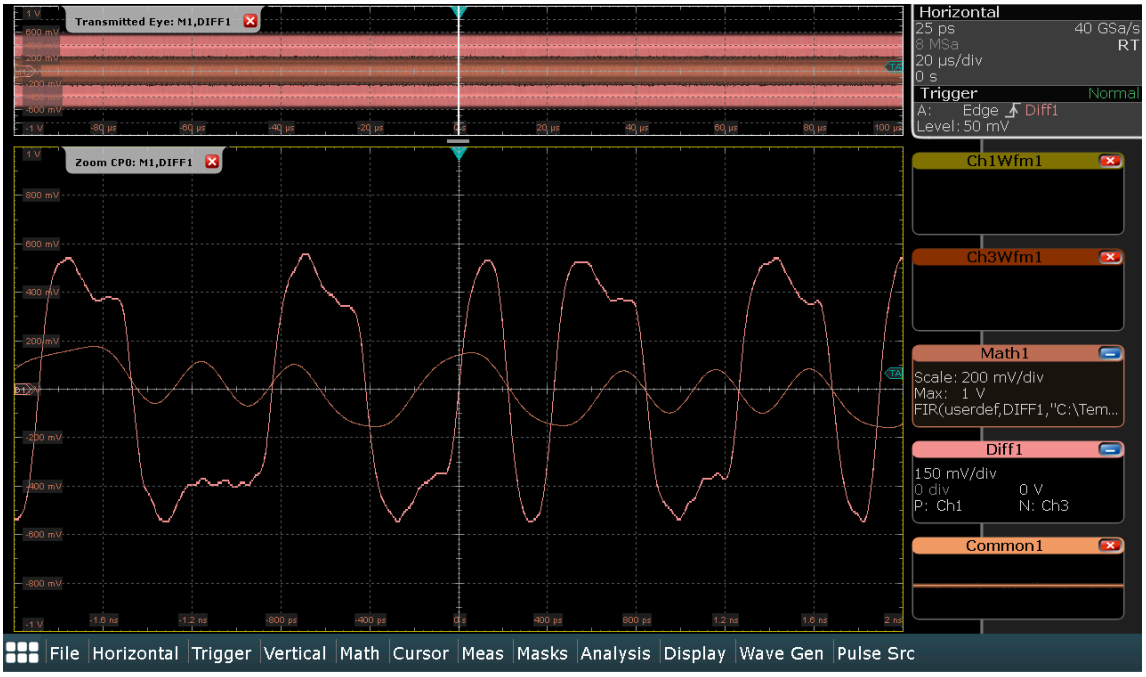


Fig. 2: Acquisition of the "short channel" trace for a USB 3.2 Gen 1 device on channels 1 and 3 with real-time calculation as a differential signal (Diff 1). Calculation of the "long channel" signal through embedding of the S-parameters from the USB-IF (Math 1).

During root cause analysis, the R&S®RTP oscilloscope provides support with analysis tools such as eye diagrams with mask tests or separation of jitter and noise components. Time domain reflectometry is also available for verifying the transmission characteristics of passive signal path components such as connectors, cables and signal lines on the printed board.

Conformance testing for USB 3.2 transmitters

USB 3.2 transmitter conformance testing focuses on the eye diagram (transmitted eye) for verifying the eye opening, signal levels and jitter components. This test is performed directly on the device output (short channel) as well as with a simulated signal path (long channel). For long channel tests, the USB Implementers Forum (USB-IF) has published files with S-parameters for various cable and signal trace lengths. During the tests, the oscilloscope acquires clock and data signal sequences with a length of 200 µs. These sequences are then checked for compliance with the standard using the SigTest USB-IF analysis software. Depending on the test mode, each USB device must generate the compliance patterns on its own: For USB 3.2 Gen 1, this means patterns CP0 (data) and CP1 (clock) and for USB 3.2 Gen 2, patterns CP9 (data) and CP10 (clock). Switching to the next CP pattern involves sending short LFPS sequences to the receiver in the USB device.

The R&S®RTP supports conformance testing for USB 3.2 Gen 1 (13 GHz model required) and for Gen 2 (16 GHz model) (Fig. 1). The SigTest analysis software is integrated into the R&S®RTP-K101 USB 3.2 conformance testing option, and the corresponding test sequence is automated. The option provides convenient graphical support to guide the user through the measurement. With the integrated two-channel 100 MHz generator option, switching between the individual test patterns takes place automatically. Simultaneous testing of the short and long channels is another simplification. The trace from the short channel setup is processed using embedding filters generated on the basis of USB-IF S-parameter files to produce a long channel trace (Fig. 2). Complete test results are compiled in a detailed report.

USB 3.2 device error example

Fig. 3 shows an example of errors that occurred during the transmitted eye test for a USB 3.2 Gen 1 device. The random jitter (RJ) determined with the clock pattern (CP1) is especially noticeable. The corresponding eye diagram for the data pattern (CP0) also exhibits high jitter and noise. The analysis tools provided with the R&S®RTP make it possible to investigate the root causes of these problems.

Fast overview with the eye pattern

Eye pattern analysis is one of the best-known techniques for performing fast signal integrity tests. It involves superimposing the individual data bits of a signal sequence (Fig. 4).

Selection of the appropriate timebase for bit analysis is critical here. For all USB standard generations, 2nd order clock data recovery (CDR) is defined with different transfer functions.

The eye masks specified in the USB standard have a hexagonal shape (Fig. 5). The minimum height of the eye opening is specified with a value of 100 mV for Gen 1 and 70 mV for Gen 2. The minimum eye width is equal to the bit length (unit interval, UI) minus the maximum total jitter (TJ) that is defined for a bit error rate of 10^{-12}. For USB 3.2 Gen 1, this value is 68 ps and for Gen 2, it is 28.6 ps.

The R&S®RTP is equipped to generate eye diagrams with a configurable CDR that is implemented in the hardware and can be used as a trigger. A continuously running CDR enables a large observation interval for the signal stream that allows detection of sporadic errors. The mask can be configured in the eye center so that acquisition is stopped when a mask violation occurs.

Fig. 6 shows the eye test for the faulty USB 3.2 Gen 1 device that was mentioned above. As was already detected during the conformance test, the eye diagram exhibits a high jitter and noise component. The additional histogram on the right side of the eye clarifies the timing distribution of the bit edges and thus the jitter. The bimodal histogram format reveals some additional information: High deterministic jitter is also contained in the signal.

Resolving error sources due to jitter and noise components

A histogram in the eye diagram can provide initial insights into the jitter and noise contained in the test signal. However, in order to gain more detailed information about the interference sources, it is very helpful to break down the total jitter and total noise into the individual components (Fig. 7).

For example, high random jitter (RJ) or high random noise (RN) can be a sign of problems in the semiconductor itself (thermal noise, shot noise) or an unstable clock oscillator. Deterministic periodic jitter (PJ) components can arise, for example, due to an unstable PLL or interference from switching power supplies. Data dependent jitter (DDJ) components are divided into duty cycle distortion (DCD), e.g. due to asymmetrical signal edges and intersymbol interference (ISI). The latter can be caused, for example, by transmission losses due to low bandwidth of signal traces or by reflections on vias or connectors.

Once the jitter separation is completed, detailed results are available (Fig. 8). The results table (top right)

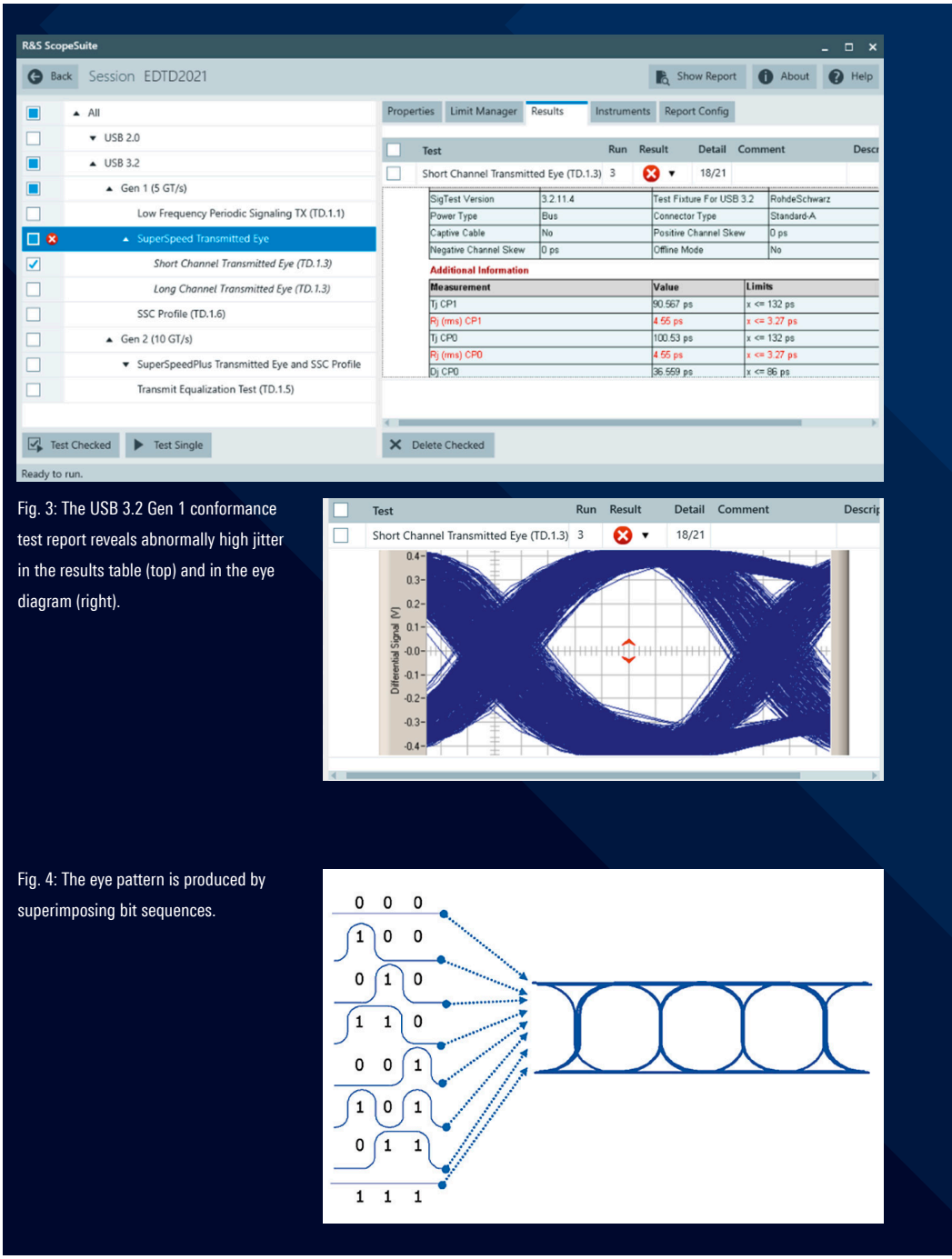
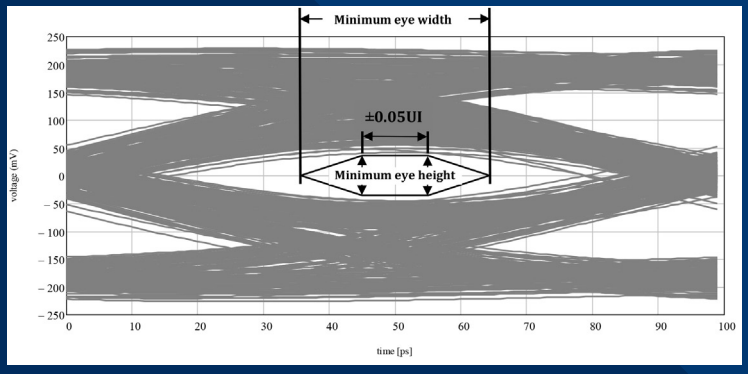


Fig. 3: The USB 3.2 Gen 1 conformance test report reveals abnormally high jitter in the results table (top) and in the eye diagram (right).

Fig. 4: The eye pattern is produced by superimposing bit sequences.

shows that the periodic jitter (PJ) dominates the deterministic jitter. The random jitter (RJ + (O)BUJ) is also noticeably high. The PJ histogram has a distribution that suggests sinusoidal interference. The second table (bottom right) lists the estimated periodic jitter components. Here, high jitter values are noticeable at 100 MHz. This is generally valuable information since the interference frequencies can be tracked back to the corresponding function blocks. Appropriate measures can then be taken to reduce the interference coupling. The power supply is a typical weak point. Interfering signals are easily injected via the supply lines and ground planes. In this example, the R&S®RTP generator option was connected to the 5 V supply voltage of the USB device under test. The injected generator signal caused the periodic interference at 100 MHz, while the additional noise resulted in strong random jitter (Fig. 9). Comparison with the situation after switching off the interference source makes this clear (Fig. 10). Once the interfering signal is eliminated, the jitter measurement included in the conformance test passes with no problems.



Signal Characteristic	5GT/s		10GT/s		Units	Note
	Minimum	Maximum	Minimum	Maximum		
Eye Height	100	1200	70	1200	mV	2, 3, 4
Dj		0.43		0.530	UI	1, 2, 3
Rj		0.23		0.141	UI	1, 5, 6
Tj		0.66		0.671	UI	1, 2, 3

Fig. 5: Mask definition from the Universal Serial Bus 3.2 Specification, Revision 1.0.

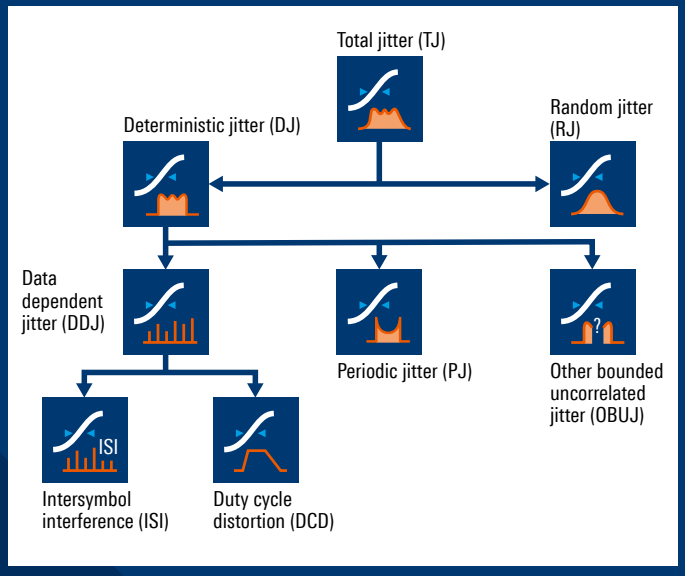


Fig. 7: The total jitter can be divided into random and deterministic components.

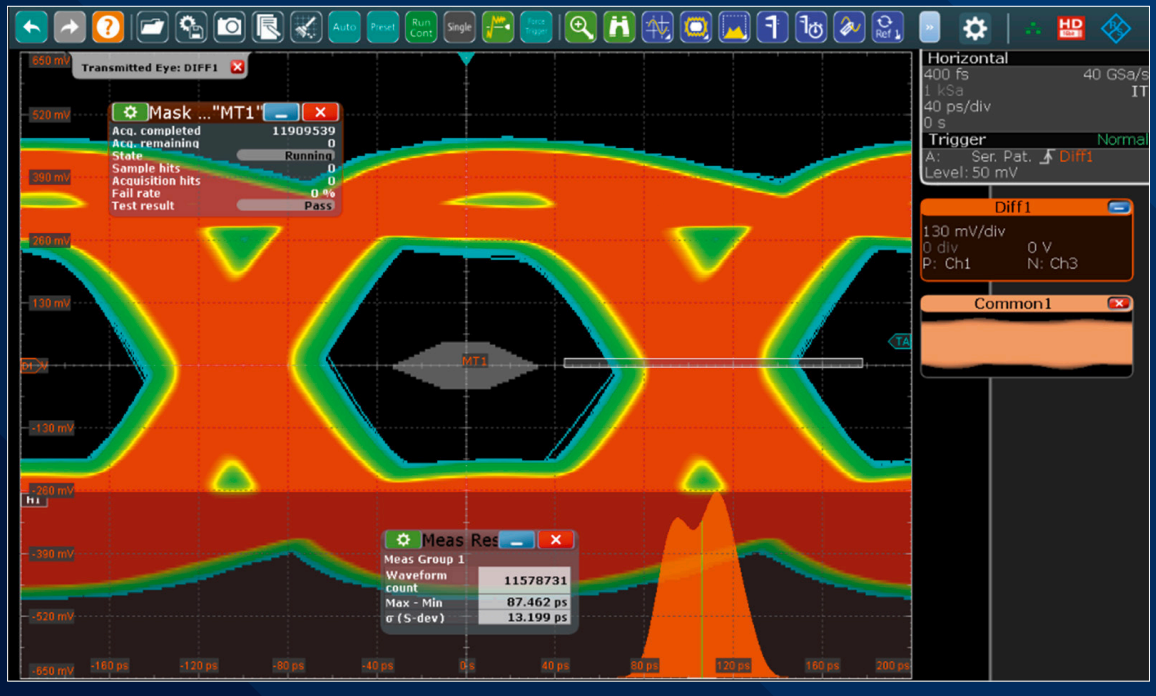


Fig. 6: Real-time eye pattern for the faulty USB device using hardware based CDR, mask testing and histogram with the R&S®RTP164 oscilloscope.

Testing the signal path with TDR

In addition to analyzing the active signals, it is also important to check the signal paths in case of signal integrity problems. Here, the focus is on the transmission losses as well as the impedance response and stability along the signal path. Depending on the signal, the bandwidth of the signal paths on the printed board, the connectors, the cables, etc. requires appropriate design and selection. Impedance steps should also be avoided due to the reflections they can cause.

The relevant measurements are usually performed using network analyzers. The R&S®RTP with integrated time domain reflectometry (TDR) provides a useful alternative. The differential 16 GHz pulse source is used as a stimulus; its reference outputs allow measurement of the reflected signals with the oscilloscope channels.

The application software provides support during setup calibration as well as during the measurement. TDR can be used to measure the impedance and reflection coefficient along the signal path.

Fig. 11 shows measurement of a USB test fixture. The differential pulse source was connected to the SMA connectors. The USB type A connector was left open so the supplied signal pulse would be fully reflected. The impedance and the reflection coefficient can be displayed vs. time as well as vs. distance, allowing easy correlation to local sections of the device under test. We can clearly see the impedance step at the transition from the SMA connectors to the printed board, the constant impedance along the signal trace, and the reflection at the USB connector.

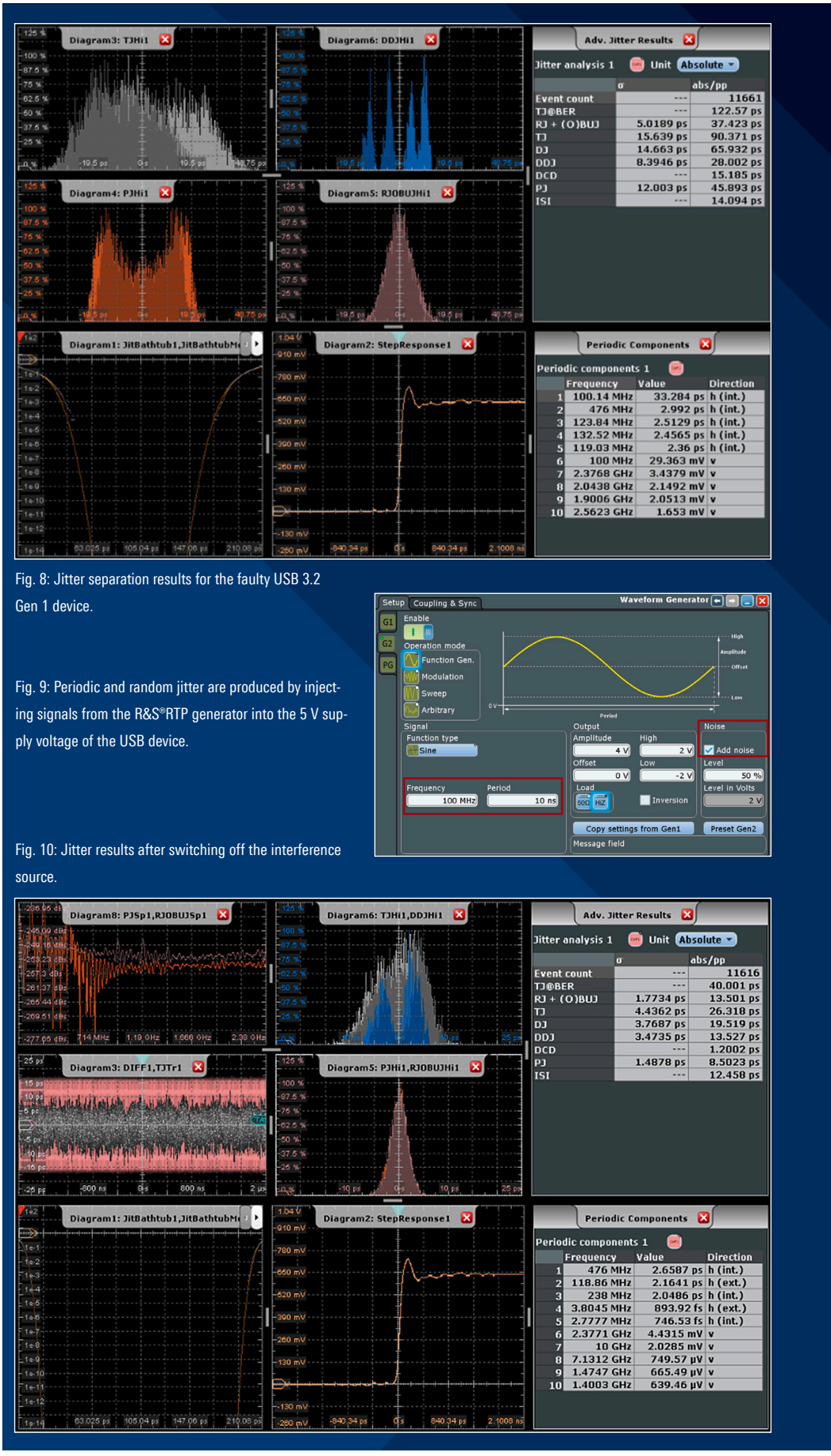


Fig. 8: Jitter separation results for the faulty USB 3.2 Gen 1 device.

Fig. 9: Periodic and random jitter are produced by injecting signals from the R&S®RTP generator into the 5 V supply voltage of the USB device.

Fig. 10: Jitter results after switching off the interference source.

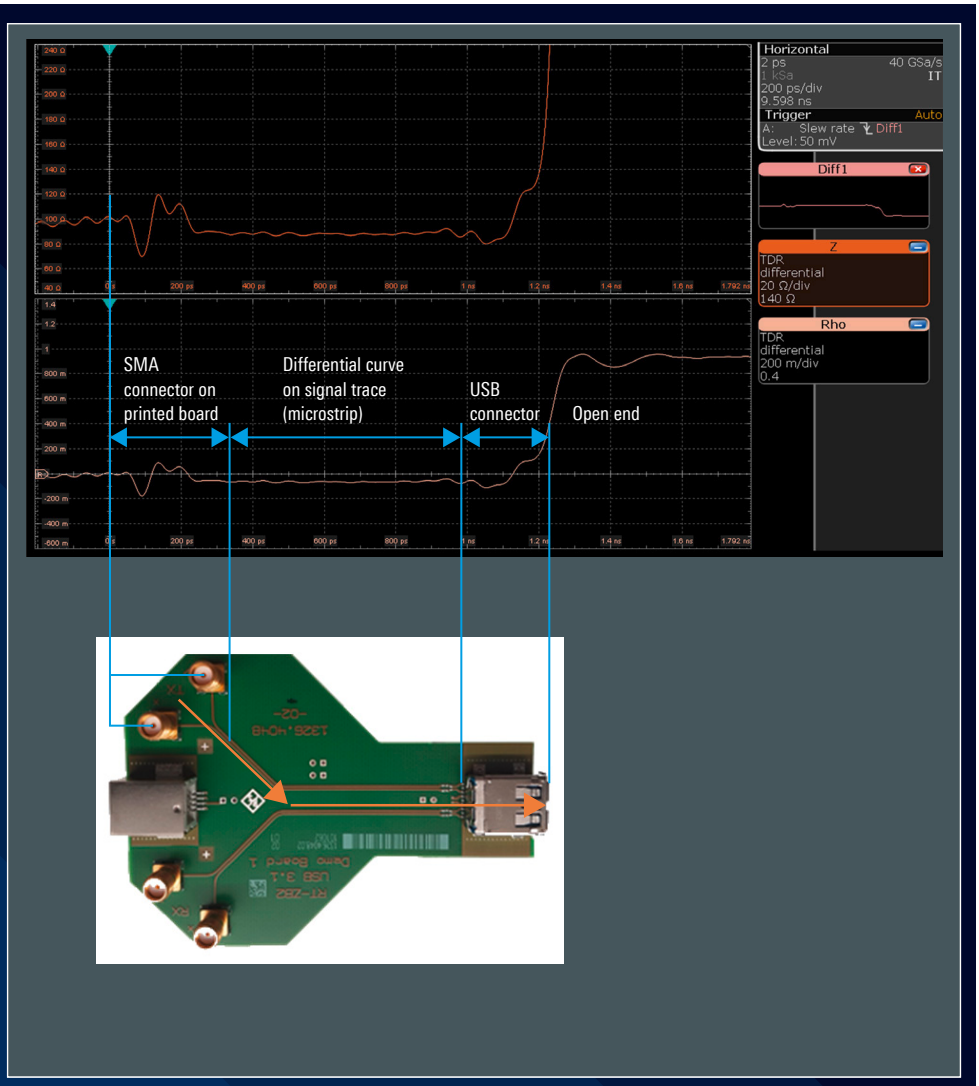


Fig. 11: TDR measurement on the USB test fixture: impedance (top), reflection coefficient (bottom).

Fig. 12: TDT measurement on the USB test fixture: The pulse rise time at the output is 108 ps.

Time domain transmissometry (TDT) is another useful measurement capability. Here, a fast pulse is also fed into the signal path. The output is connected to the oscilloscope channel to allow determination of the transmission losses. The TDT result shows the pulse shape that arises due to transmission losses. The rise time measured in the example in Fig. 12 suggests a bandwidth of about 3.2 GHz (BW = $0.35/t_{rise}$).

Summary

Conformance tests on serial bus interfaces include important measurements when it comes to ensuring interoperability between electronic devices and their accessories. When errors are encountered, appropriate T&M equipment is the key to rapidly determining the root causes. Along with software options for performing automated conformance tests, the R&S®RTP oscilloscope provides a number of very useful tools for debugging signal integrity problems.

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