TEST CHALLENGES IN MODERN POWER ELECTRONICS

Dr. Gabriel Rojas
Application Engineer Power Electronics

ROHDE&SCHWARZ
Make ideas real

AGENDA

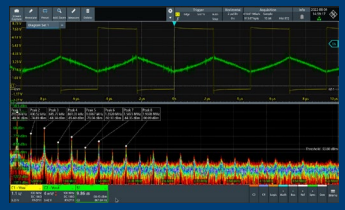
- Design steps in power electronics
- Switching stage challenges
- Probing
- Parasitic components
- Conducted and radiated emissions
- Stability of SMPS
- Power integrity
- Start-up sequence behavior

DESIGN STEPS

1. Define the architecture
2. Select the integrated circuits
3. Circuit design
4. Simulation
5. Testing

Testing the design

- Verify sub-circuits and switching times of the transistors
- Switching losses
- Characterization of passive components
- Stability
- Efficiency
- Transient response, start-up, shut down
- Voltage ripple
- Electromagnetic compatibility

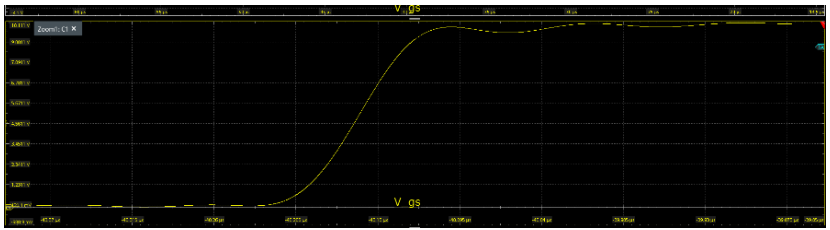


SWITCHING STAGE
BANDWIDTH

- Among the greatest challenges in modern power electronics is testing systems with wide bandgap materials like SiC and GaN. Their faster switching times condition the bandwidth.
- Oscilloscope and probes must be chosen accordingly.

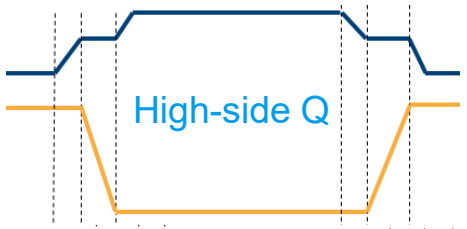
$$Bandwidth \sim \frac{0.35}{t_{sw,rise}}$$

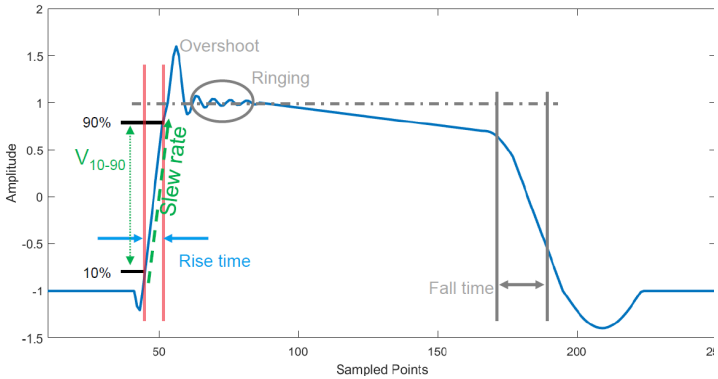
- Example: If a semiconductor has a rise time of 4 ns, a minimum bandwidth of 87.5 MHz is required.



SWITCHING STAGE
BEST PRACTICE MEASUREMENTS

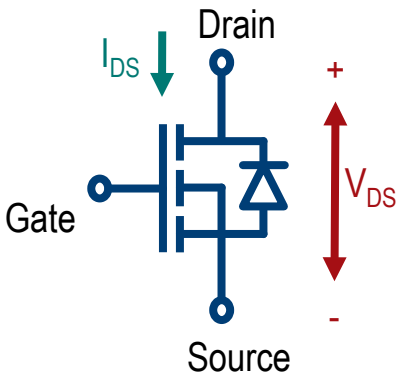
- As a rule of thumb, it should be checked:
  - ✓ V_{GS} and V_{DS}
  - ✓ Rise times and fall times (10/90 or 20/80)
  - ✓ Overshoot, ringing
  - ✓ General timing of high- and low-side switch (syncronous converter)
  - ✓ Robustness test



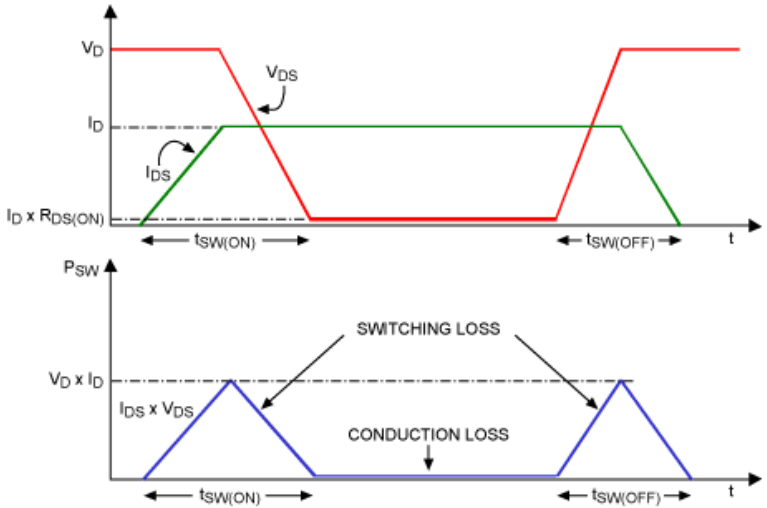


SWITCHING STAGE
QUANTIFY LOSSES

- **Semiconductors operation generate losses**
  - Conduction losses
  - Switching losses
- **Losses are important for cooling system**

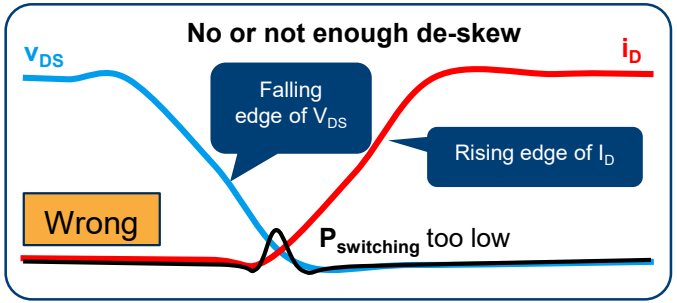


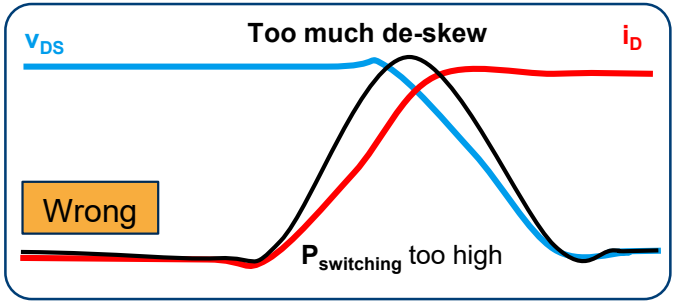
- **Switching losses to be evaluated**
  - Turn on losses
  - Turn off losses
  - Reverse recovery losses

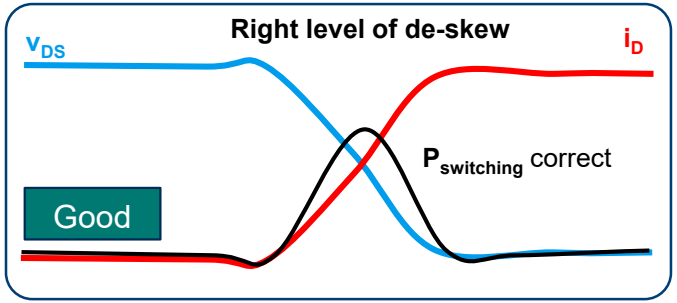


SWITCHING STAGE
DE-SKEW

- **Voltage and current probes have different rise times and propagation delays**
- **Examples**
  - High voltage differential probe: ~8 ns group delay
  - Clamp-on current probe: ~15 ns
  - Small loop Rogowski probes: ~12 – 20 ns
- **For accurate switching loss measurements the delay has to be compensated for (de-skew)**
  - The point of alignment depends on the application
  - This process is uncertain and requires repetitions

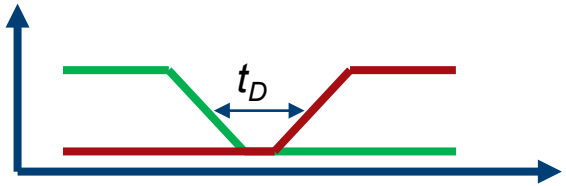


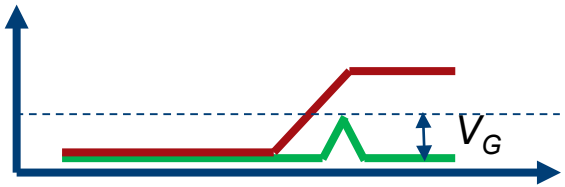




SWITCHING STAGE
ROBUSTNESS TESTING

- Robust test ensures that the design criteria are fulfilled and allows the identification of critical conditions.
  - Load variations.
  - Input voltage variation
  - Mode transition: CCM to DCM.
- These situations are hard to capture using an oscilloscope, however, with a digital trigger it is possible to:
  - Trigger on dead time violation between HS and LS switching. Source of EMI problems.
  - Find glitches in HS transistors, which can be induced by the turn-on of the LS switch.

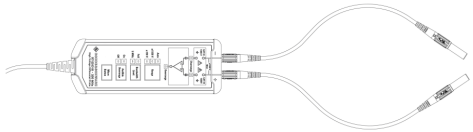




SWITCHING STAGE
PROBES

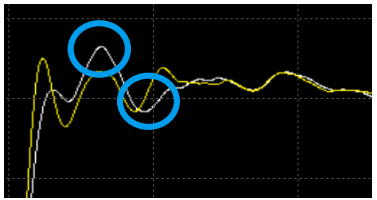
► Leads and clips also have an influence in the measurement.

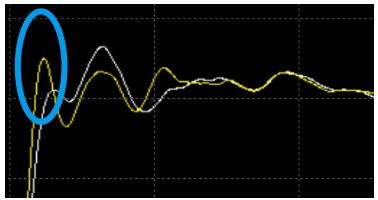
Untwisted or twisted?:



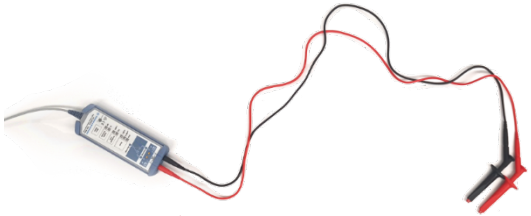
pro	minimizes the capacitive load on the measuring point
con	interferers are looped in

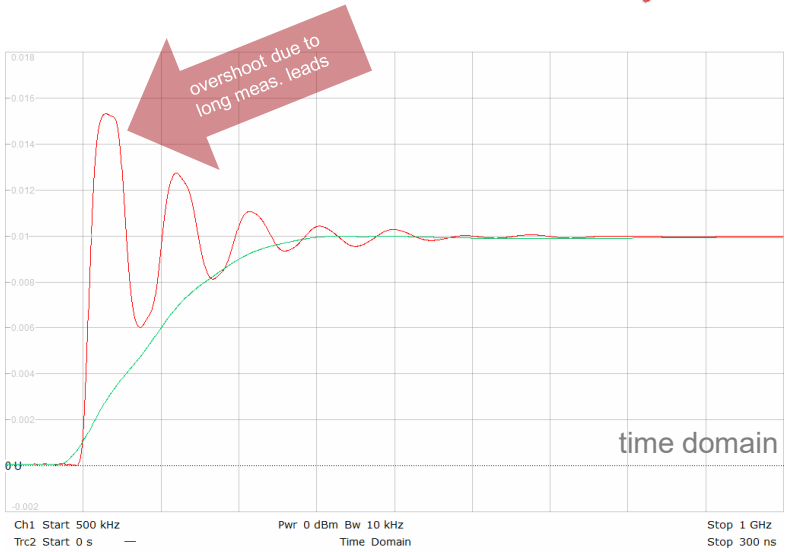
pro	interferers are minimized
con	greater load on the measuring point





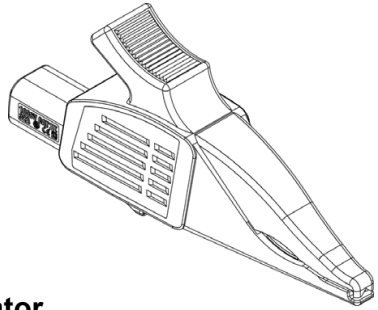
Length:



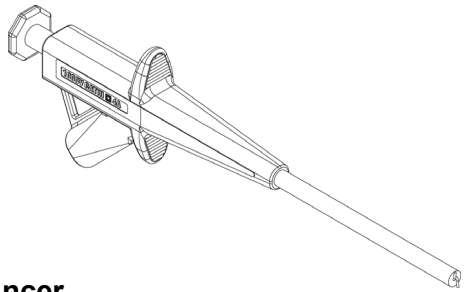


SWITCHING STAGE
PROBES

- Clips.

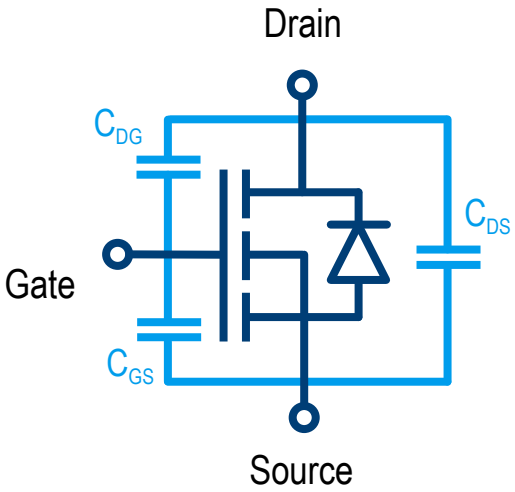


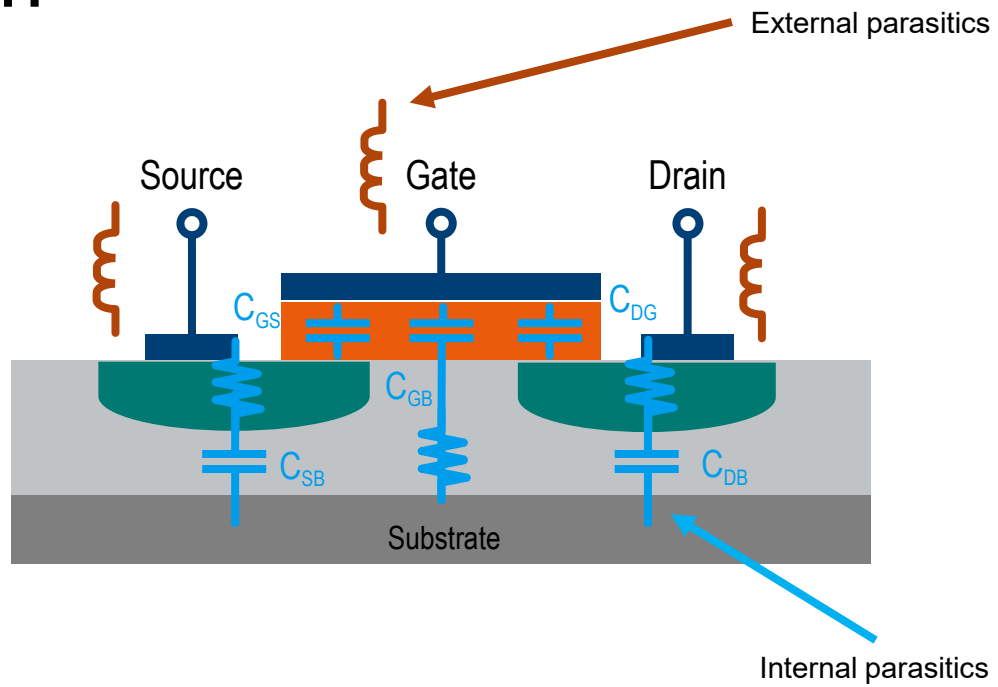
Alligator



Pincer

PARASITICS
SHOULD I CONSIDER THEM?



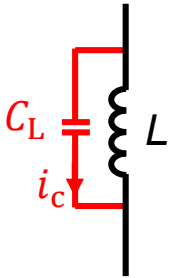


… parasitics in transistors will affect its behavior in fast switching

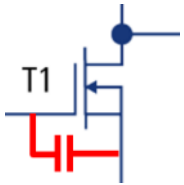
… and might affect its efficiency in power consumption

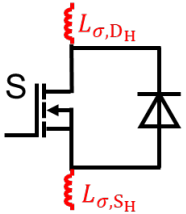
PARASITICS
MAIN CHALLENGES

- Effects:
  - Voltage spikes
  - Ringing
  - EMI problems
  - Reliability problems



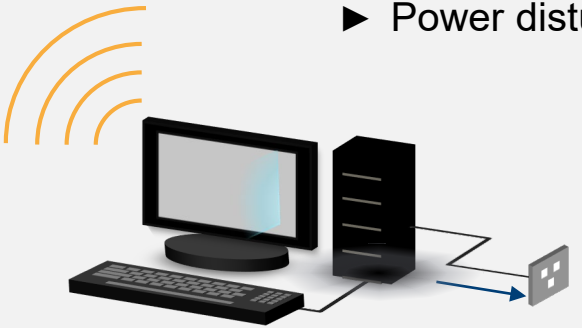
- Main sources of problems:
  - Stray capacitance in inductors: Change in the rise/fall times
  - Stray inductances: Change in the rise/fall times
  - Parasitic capacitance in transistors: Hard switching





EMI

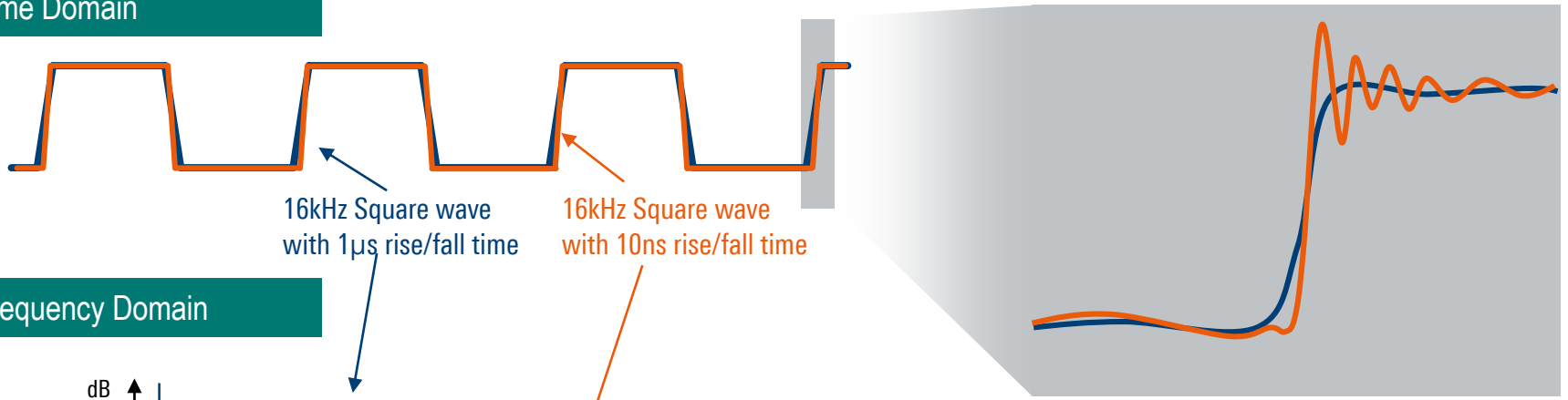
Radiated EMI	Conducted EMI
► Magnetic radiation	► Voltage disturbance
► Electric radiation	► Power disturbance



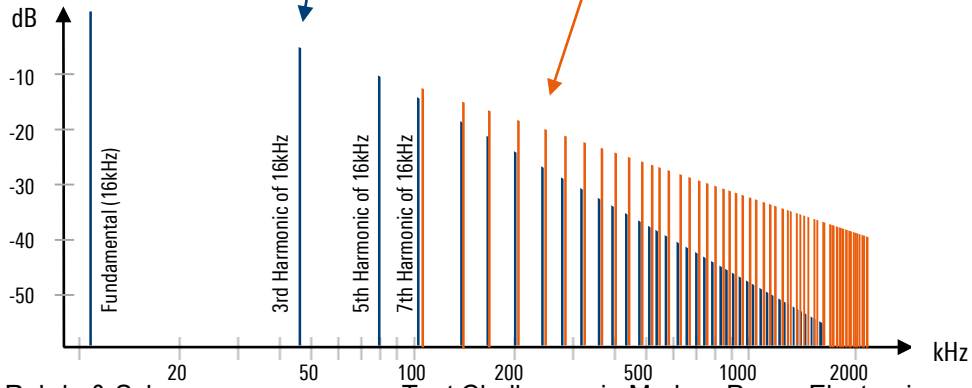
Main problems:
- ► Voltage overshoot
- ► Switching oscillations
- ► Displacement currents

IMPACT OF FASTER SWITCHING AND STEEP EDGES ON EMI

Time Domain



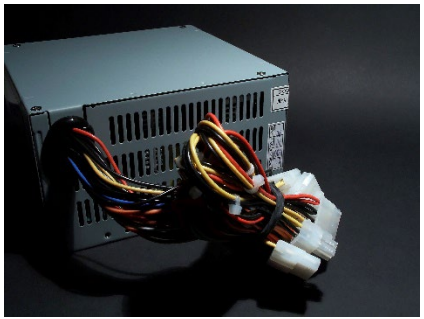
Frequency Domain

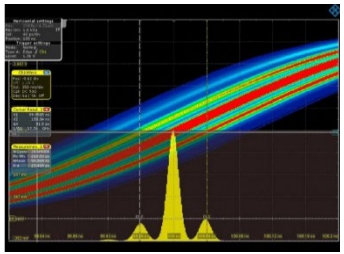


High frequency Harmonics come with higher levels

STABILITY IN SWITCHED-MODE POWER SUPPLIES

- SMPS are equipped in electronic circuits, computers and telecommunication systems, uninterruptible power supply systems and many more.
- An stable SMPS is characterized by:
  - Fast transient response (High bandwidth)
  - High phase margin
- An unstable SMPS may lead to:
  - High output voltage oscillations after a load transient
  - Jitter
  - Noise from passive components
  - Failures in the transistors



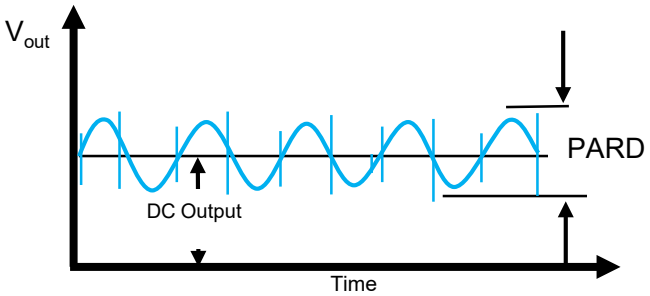


STABILITY
CHALLENGES

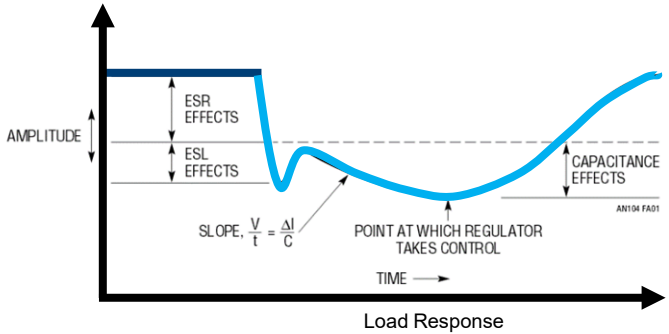
- Closed loop response measurement:
  - Large decoupling capacitance may affect the response
  - Selection of the amplitude profile
  - Probe attenuation and leads.
  - Low noise floor
  - Injection point

POWER INTEGRITY
CHALLENGES ON DC POWER LINES

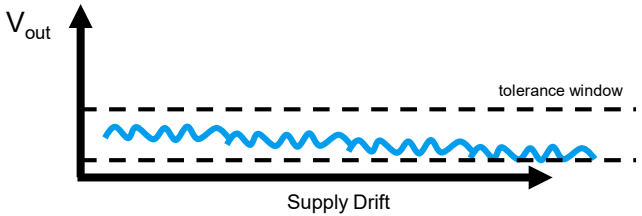
- PARD (Periodic and Random Disturbances):
  - Switching noise
  - Ripple
  - Transients
  - Random noise



- Load step response



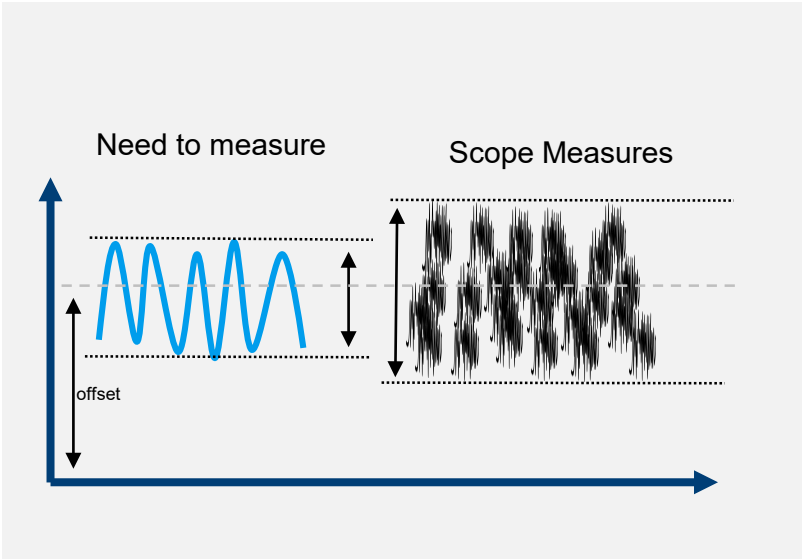
- Supply drift



POWER INTEGRITY
CHALLENGES ON DC POWER LINES

- Attenuation ratio increases displayed noise floor of the instrument.
- Offset of the oscilloscope
- Vertical resolution of the oscilloscope
- Decreasing voltage and tolerance levels:

Rail Value	Tolerance	Need to measure
3.3 V	1%	33 mV$_{pp}$
1.8 V	2 %	36 mV$_{pp}$
1.2 V	2 %	24 mV$_{pp}$
1 V	1 %	10 mV$_{pp}$



START-UP SEQUENCE

- Most converters have a Soft-Start function meant to start-up in a smooth way and avoid large inrush currents or overshoots.
- The main challenge is to acquire at the same time:
  - Input and output voltages
  - Switching characteristics
- This requires significant memory depth.

Find out more

www.rohde-schwarz.com/oscilloscopes

For further questions please contact
Gabriel.rojas@rohde-schwarz.com
with subject “Oscilloscope days 2022”

ROHDE&SCHWARZ

Make ideas real