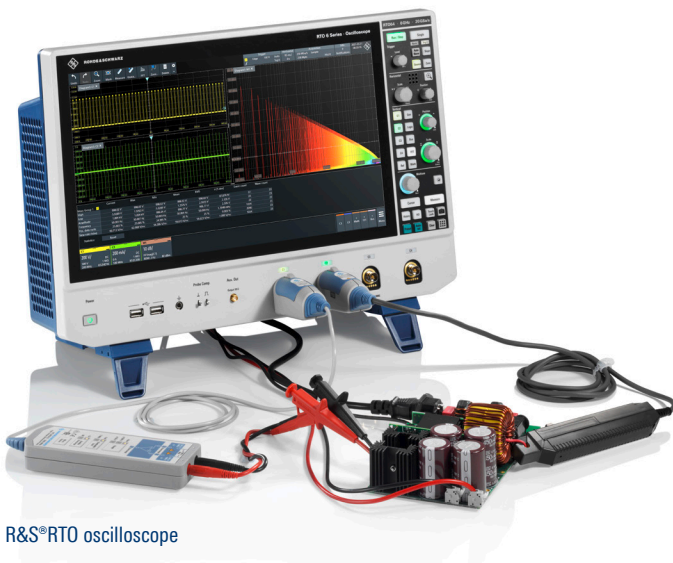


# INCREASING TEST COVERAGE IN HARD SWITCHING HALF BRIDGE CONFIGURATIONS

Power converter and inverter designs for higher power levels are usually based on hard switching half bridge configurations. In such setups, users must pay particular attention to proper switching operations to prevent shoot-through events. Setting up complex real-time trigger conditions using the R&S®RTE and R&S®RTO oscilloscopes increases the test coverage and robustness of converter and inverter systems.



R&S®RTO oscilloscope

## Your task

Hard switching in half bridge configurations is a commonplace technique for efficient power conversion, in particular at higher power levels. With increasing switching speeds as in SiC designs, parasitic coupling from the switch node to the gate is becoming more and more critical. This can lead to unwanted high side gate glitches and turn-on conditions with both transistors of the half bridge conducting at the same time. Such a shoot-through condition can destroy the transistors. Increasing the robustness of high-power designs is an important safety concern. It is important to make sure there are no critical glitches on the high side gate of the half bridge.

## Rohde & Schwarz solution

The R&S®RTO and R&S®RTE oscilloscopes offer an advanced, easy-to-use digital trigger unit. In contrast to analog trigger units, the digital trigger unit uses the sampling values of the acquisition paths to decide on trigger events in the digital domain. Users do not have the disadvantages of a separate analog trigger path as used in conventional oscilloscopes.

## The advantages of digital triggers for identifying critical operation points

The benefits of the Rohde & Schwarz solution are:

- ▶ High flexibility in setting up complete real-time A/B/R trigger conditions
- ▶ Individual setting of the trigger hysteresis to optimize the trigger sensitivity for the respective signal
- ▶ High trigger sensitivity at full bandwidth to capture small, unwanted glitches
- ▶ Very low jitter values for stable triggering

When adjusting the trigger value for the high side gate signal to the largest acceptable value, users can easily identify any switching event that violates this condition, i.e. bears the risk of a shoot through. Thanks to real-time operation, no critical event is missed. Operating the DUT at different load and environmental conditions during verification tests makes it possible to identify critical conditions and eliminate the risk of a shoot through.

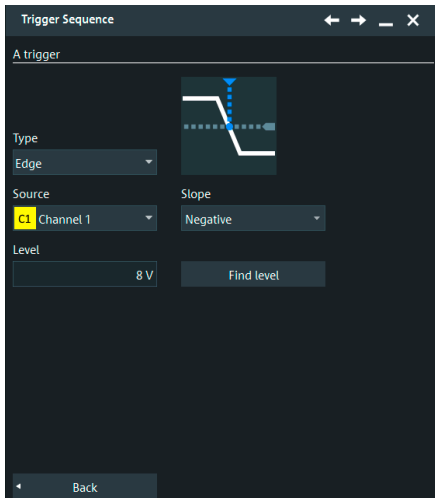
## Measurement setup

To verify the risk of shoot-through events, the gate to source voltage on the high side and low side switch has to be simultaneously measured. Users have to make sure there are no glitches on the high side gate signals exceeding a predefined voltage level in order to prevent the corresponding transistor from accidentally being turned on. This task requires a complex trigger setup and very high trigger accuracy, and the trigger threshold must be precisely defined.

## Trigger setup

After connecting the oscilloscope to the DUT, the oscilloscope application dialog helps the user configure all relevant trigger options.

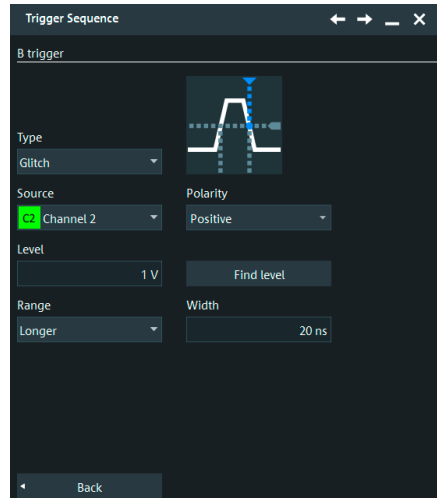
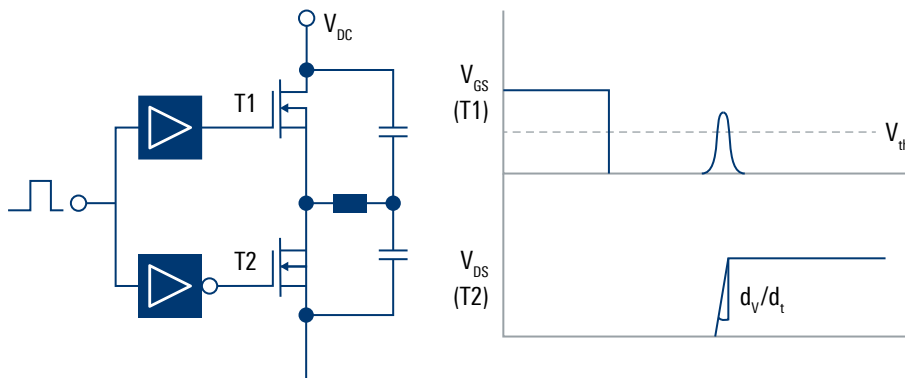
- ▶ Select the trigger sequence where you are able to define two events in a sequence



Trigger setup: edge event on negative slope for trigger A

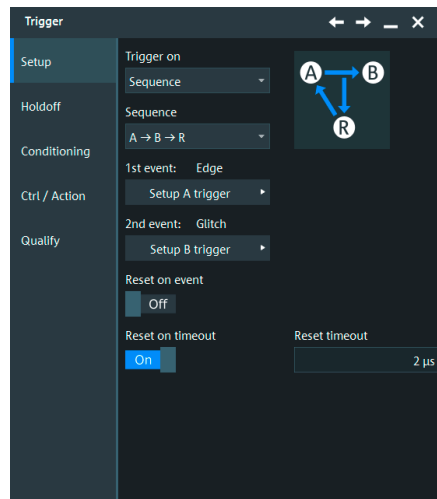
- ▶ Define the first trigger event (A) as a negative edge trigger to catch the falling edge of the gate to source voltage at switch T2. Define a suitable trigger level for this condition. This trigger event will catch every switch-off event of the low side switching device during continuous operation of the half bridge

## Measurement setup



Trigger setup: glitch event for trigger B

- ▶ Define the next trigger event (B) of the sequence to detect a glitch on the gate to source terminal on switch T1. This trigger is only active after the first trigger event (A) has occurred. Define the glitch level, polarity and width values according to the worst case condition of the application
- ▶ Define a reset condition to reset the first pre-trigger event after a specific timeout in case no glitch event has occurred. The maximum on-time of the low side switch defines the timeout value in the trigger setting



Trigger setup: timeout condition for trigger reset

## Application measurement results

A 500 W DC/DC converter based on a symmetrical half bridge topology is used to demonstrate how to automatically identify critical gate timing events that can lead to a shoot through. The converter under test with an input voltage between 36 V and 72 V generates an output voltage of 3.3 V. The switching frequency is 400 kHz. According to the data sheet, the lowest possible threshold voltage of the MOSFET gate is 2 V.



Measurement result of a half bridge configuration

To identify the safety margin, reduce the trigger level for the high side gate glitch trigger starting at 2 V until a trigger event happens. At 1.88 V (green box) trigger events are generated as shown in the measurement result. This means a safety margin of 120 mV, depending on the actual application. It has to be decided whether this is sufficient for the robustness of the converter or inverter system.

In addition to the trigger capability, the user gains even more insight into the circuit, such as the resonance frequency (blue box) between leakage inductance of the transformer and output capacitance of the switch.

## Summary

The digital trigger system of the R&S®RTO and R&S®RTE oscilloscopes features real-time trigger capability. The digital trigger yields high precision, very low trigger jitter and enables high trigger sensitivity at full bandwidth. These advantages combined with other features such as a high dynamic range and intuitive user interface turn the instruments into powerful tools for debugging and analyzing converter designs with bridge configurations.

## See also

[www.rohde-schwarz.com/oscilloscopes](http://www.rohde-schwarz.com/oscilloscopes)

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