Application Note

METHOD OF IMPLEMENTATION (MOI) FOR IEEE UP TO 100 GBPS INTERFACE CHANNEL TEST

Products:

- R&S®ZNA
- R&S®ZNB
- R&S®ZNBT

Curtis Donahue, UNH-IOL | GFM356 | Version 0e | 03.2021

http://www.rohde-schwarz.com/appnote/GFM356

Contents

Many thanks to Mr. Curtis Donahue, Senior Manager, Ethernet Technologies (UNH-InterOperability Lab, https://www.iol.unh.edu) for his significant contribution to this application note. By combining his expertise as a neutral party within industry and standards bodies knowledge, we have achieved synergies that will benefit both design and test engineers.

1 Introduction

This application note created by the Test and measurement specialist Rohde & Schwarz and the University of New Hampshire Interoperability Laboratory (UNH-IOL) describes methods of implementation (MOI) for precise, fast and error-free compliance testing of high-speed cables and backplanes according to IEEE 802.3 standards (up to 802.3ck), using vector network analyzers test equipment from Rohde & Schwarz.

The purpose of this document is to provide a step by step guideline on how to perform compliance testing for cable assembly and channel characteristics as defined in the following IEEE 802.3 serial interface specifications:

Specification		PHY Type	Typical Connector Type
IEEE P802.3ck D2.0 (Mar. 2021 draft)	Clause 162	100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4	SFP112, QSFP112, QSFP-DD112, OSFP112
	Clause 163	100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4	2.4mm, 1.85mm connector
IEEE 802.3cd-2018	Clause 136	50GBASE-CR1, 100GBASE-CR2, 200GBASE-CR4	SFP28, SFP56, QSFP28, QSFP56
	Clause 137	50GBASE-KR1, 100GBASE-KR2, 200GBASE-KR4	2.92mm, 2.4mm connector
IEEE 802.3by-2016	Clause 110	25GBASE-CR	SFP28, SFP56
	Clause 111	25GBASE-KR	2.92mm, 2.4mm connector
IEEE 802.3bj-2014	Clause 92	100GBASE-CR4	QSFP28
	Clause 93	100GBASE-KR4	2.92mm, 2.4mm connector

Several industry-recognized mechanical interfaces can be used in the implementation of the above listed serial specifications. This document assumes the channel/cable assembly under test utilizes one for the following mechanical definitions as the available Test Point (TP):

- 2.92mm, 2.4mm, 1.85mm connector (or equivalent coaxial connector)
- SFP28
- SFP56
- SFP-DD
- QSFP28
- QSFP56
- QSFP-DD

1.1 Glossary

COM ……Channel Operating Margin

ERL……Effective Return Loss

fb…… Nominal Signaling Rate Value

FEXT……Far-End Crosstalk

ICN …… Integrated Crosstalk Noise

ICMCN …… Integrated Common Mode Conversion Noise

IFBW…….. Intermediate Frequency Bandwidth

ILD ……... Insertion Loss Deviation

NEXT…….. Near-End Crosstalk

VNA…… Vector Network Analyzer

1.1.1 Definition of MOI terminology

1.1.1.1 ERL – Effective Return Loss

ERL is a Figure of Merit which incorporates an aggregate of mismatches within the channel.

Unlike standard Return Loss, which is only a function of Impedance Mismatches within the channel, ERL incorporates return loss with the effects of equalization, as well as transmitter noise and receiver frequency response into a signal-to-noise-like figure of merit.

It is not a parameter that can be individually tuned for or otherwise optimized.

The only way to optimize or improve the “result” is to improve or otherwise enhance the individual mismatches within the channel.

1.1.1.2 COM – Channel Operating Margin

COM is also a Figure of Merit, basically it is the delta (magnitude) between Insertion Loss and Isolation, which can be loosely described as a Signal to Noise Ratio or SNR

The referenced “Isolation” is comparable to crosstalk, in the sense that inter-channel or intra-channel leakage is recorded.

This leakage has traditionally been described as FEXT (far end crosstalk), NEXT (Near end crosstalk).

By means of a formulaic interpretation:

$$COM = 20 \log \frac{A_{signal}}{A_{noise}}$$

1.1.1.3 ILD – Insertion Loss Deviation

Insertion loss is attenuation versus frequency. For passive circuits or structures, Insertion Loss will increase versus frequency. Ideally, insertion loss will increase monotonically with a straight-line transfer function. In practice insertion loss will have ripple or other flatness deviations.

ILD is a polynomial fit of the measured data, which bounds the non-monotonic deviations.

2 Required equipment

2.1 For IEEE P802.3ck D2.0 (Mar. 2021 draft)

Description	Equipment	Quantity
Network Analyzer	R&S® ZNA50 Vector Network Analyzer, material number 1332.4500.54, 4 ports, 10MHz - 50GHz, 2.4mm(m) test ports	1
RF Cable	R&S® ZV-Z197, 50 Ohm, DC to 50GHz, 2.4mm(f)-2.4mm(m), flexible, phase stable	per port of VNA
Calibration Unit/Kit	R&S® ZN-Z55 Calibration Unit, 9kHz to 50GHz, 2 ports, 2.4mm(f) or R&S® ZN-Z224 Calibration Kit, 50 Ohm, DC to 50GHz, 2.4mm, male/female	1
Test Fixture and adapter	Wilder Technologies – www.wilder-tech.com 100GBASE-CR1: SFP112– with 2.4mm or 1.85mm, Coming soon 200GBASE-CR2: QSFP112 - with 2.4mm or 1.85mm, Coming soon 400GBASE-CR4: QSFP-DD112 or OSFP112 - with 2.4mm or 1.85mm or PHY-SI - www.phy-si.com 400GBASE-CR4: QSFP-DD-800G & OSFP-800G - 2.92mm or 2.4mm 802.3ck Draft 2.0 specs fixtures out to 50GHz	2
50 Ohm Terminator	Midwest Microwave CGT-1500-M0-24M-02 or API-Weinschel M1460	per open fixture port
Software Environment	Matlab/Matlab Runtime	

2.2 For IEEE 802.3cd-2018

Description	Equipment	Quantity
Network Analyzer	R&S® ZNB40 Vector Network Analyzer, material number 1311.6010.84, 4 ports, 100kHz - 40GHz, 2.92mm connectors or R&S® ZNA43 Vector Network Analyzer, material number 1332.4500.44, 4 ports, 10MHz - 43.5GHz, 2.92mm connectors	1
RF Cable	R&S® ZV-Z195, 50 Ohm, DC to 40GHz, 2.92mm(f)-2.92mm(m), flexible, phase stable	per port of VNA
Calibration Unit/Kit	R&S® ZN-Z54 Calibration Unit, 9kHz to 40GHz, 2 ports, 2.92mm(f) or R&S® ZN-Z129 Calibration Kit, 50 Ohm, 0Hz to 40GHz, 2.92mm(f)	1
Test Fixture and adapter	Wilder Technologies – www.wilder-tech.com 50GBASE-CR1: SFP28/56 – with 2.92mm 100GBASE-CR2: QSFP28 – with 2.92mm 200GBASE-CR4: QSFP56– with 2.92mm or PHY-SI - www.phy-si.com 50GBASE-CR1: SFP28/56 - 2.92mm or 2.4mm 100GBASE-CR2: QSFP28/56 - 2.92mm 200GBASE-CR4: QSFP28/56 - 2.92mm 802.3cd-2018 specs fixtures out to 25GHz	2
50 Ohm Terminator	Amphenol SF8015-6002 or API Technologies TS400M or Midwest Microwave CGT-1400-M0-29M-02	per open fixture port
Software Environment	Matlab/Matlab Runtime	

2.3 For IEEE 802.3by-2016

Description	Equipment	Quantity
Network Analyzer	R&S® ZNB40 Vector Network Analyzer, material number 1311.6010.84, 4 ports, 100kHz - 40GHz, 2.92mm connectors or R&S® ZNA26 Vector Network Analyzer, material number 1332.4500.24, 4 ports, 10MHz -26.5GHz, 3.5mm connectors	1
RF Cable	R&S® ZV-Z193, 50 Ohm, DC to 26.5GHz, 3.5mm(f)-3.5mm(m), flexible, phase stable	per port of VNA
Calibration Unit/Kit	R&S® ZN-Z53 Calibration Unit, 100kHz to 26.5GHz, 2 ports, 3.5mm(f) or R&S® ZN-Z52 Calibration Unit, 100kHz to 26.5GHz, 4 ports, 3.5mm(f) or R&S® ZN-Z135 Calibration Kit, 50 Ohm, 0Hz to 26.5GHz, 3.5mm(f)	1
Test Fixture and adapter	Wilder Technologies – www.wilder-tech.com 25GBASE-CR: SFP28 – with SMA or PHY-SI - www.phy-si.com 25GBASE-CR: SFP28/56 - 2.92mm or 2.4mm 802.3by-2016 specs fixtures out to 25GHz	2
50 Ohm Terminator	Hirose HRM-601A(52) or XMA 2003-6110-00 or P1dB P1TR-SAM-26G2W	per open fixture port
Software Environment	Matlab/Matlab Runtime	

2.4 For IEEE 802.3bj-2014

Description	Equipment	Quantity
Network Analyzer	R&S® ZNB40 Vector Network Analyzer, material number 1311.6010.84, 4 ports, 100kHz - 40GHz, 2.92mm connectors or R&S® ZNA26 Vector Network Analyzer, material number 1332.4500.24, 4 ports, 10MHz - 26.5GHz, 3.5mm connectors	1
RF Cable	R&S® ZV-Z193, 50 Ohm, DC to 26.5GHz, 3.5mm(f)-3.5mm(m), flexible, phase stable	per port of VNA
Calibration Unit/Kit	R&S® ZN-Z53 Calibration Unit, 100kHz to 26.5GHz, 2 ports, 3.5mm(f) or R&S® ZN-Z52 Calibration Unit, 100kHz to 26.5GHz, 4 ports, 3.5mm(f) or R&S® ZN-Z135 Calibration Kit, 50 Ohm, 0Hz to 26.5GHz, 3.5mm(f)	1
Test Fixture and adapter	Wilder Technologies - www.wilder-tech.com 100GBASE-CR4: QSFP28 – with SMA or PHY-SI - www.phy-si.com 100GBASE-CR4: QSFP28 - 2.92mm 802.3bj-2014 specs fixtures out to 25GHz	2
50 Ohm Terminator	Hirose HRM-601A (52) or XMA 2003-6110-00 or P1dB P1TR-SAM-26G2W	per open fixture port
Software Environment	Matlab/Matlab Runtime	

3 External References

Table of Applicable IEEE Conformance Requirements

IEEE 802.3		Differential insertion loss	Differential insertion loss @ Nyquist	Differential return loss	Differential return loss @ Nyquist	Differential to common-mode return loss	Differential to common-mode conversion loss	Common-mode to common-mode return loss	COM	ERL	IEEE Reference
802.3bj-2014	Clause 92 100GBASE-CR4	x	x	x		x	x	x	x		See 92.10
	Clause 93 100GBASE-KR4	Informative		Informative					x		See 93.9
802.3by-2016	Clause 110 25GBASE-CR	x	x	x		x	x	x	x		See 110.9
	Clause 111 25GBASE-KR	Informative		Informative					x		See 111.9
802.3cd-2018	Clause 136 50GBASE-CR1 100GBASE-CR2 200GBASE-CR4	x	x			x	x	x	x	x	See 136.11
	Clause 137 50GBASE-KR1 100GBASE-KR2 200GBASE-KR4	Informative							x	x	See 137.10
P802.3ck Draft 2.0	Clause 162 100GBASE-CR1 200GBASE-CR2 400GBASE-CR4	x	x			x	x	x	x	x	See 162.11
	Clause 163 100GBASE-KR1 200GBASE-KR2 400GBASE-KR4	Informative							x	x	See 163.10

4 IEEE Defined Test Points

The following sections, and included diagrams, demonstrate the Test Point (TP) definitions that are found in the respective IEEE Clauses covered by this MOI. There can be several test points defined depending on the IEEE Clause being tested, but not all are applicable to cable assemblies or backplane channels.

4.1 BASE-CR Test Points

Figure 1 shows an entire 100GBASE-CR4 link from PHY to PHY, and the location of all five test points defined in Clause 92. This same diagram is applicable to other CR clauses (Clause 110 25GBASE-CR, Clause 136 50GBASE-CR1, etc.) by scaling the number of transmit and receive signals accordingly. TP0 and TP5 are specified at the chip interface; TP1 and TP4 are specified at the host side of the MDI interconnect; TP2 and TP3 are used when characterizing a mated set of Module Compliance Board (MCB) and Host Compliance Board (HCB) test fixtures.

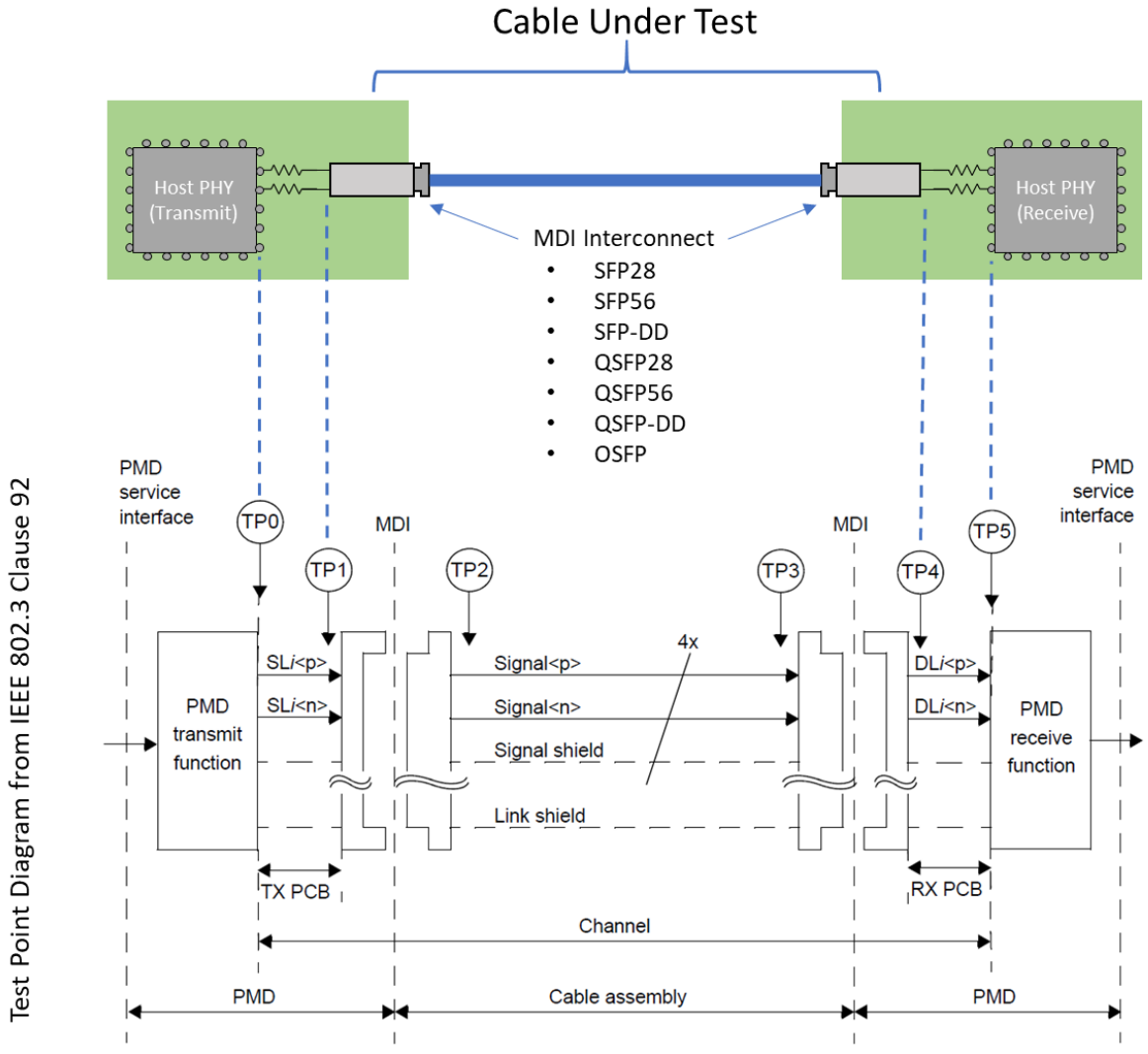


Figure 1:Example of IEEE Cable Assembly and respective Test Points [1]

The test points that are of most interest for the purposes of this MOI are TP1 and TP4. TP1 and TP4 are where the IEEE channel parameters (differential insertion loss, differential return loss, COM, ERL, etc.) are characterized. Figure 2 demonstrates the relationship between TP1 and TP4 to the cable assembly under test and the test fixtures used to characterize the channel.

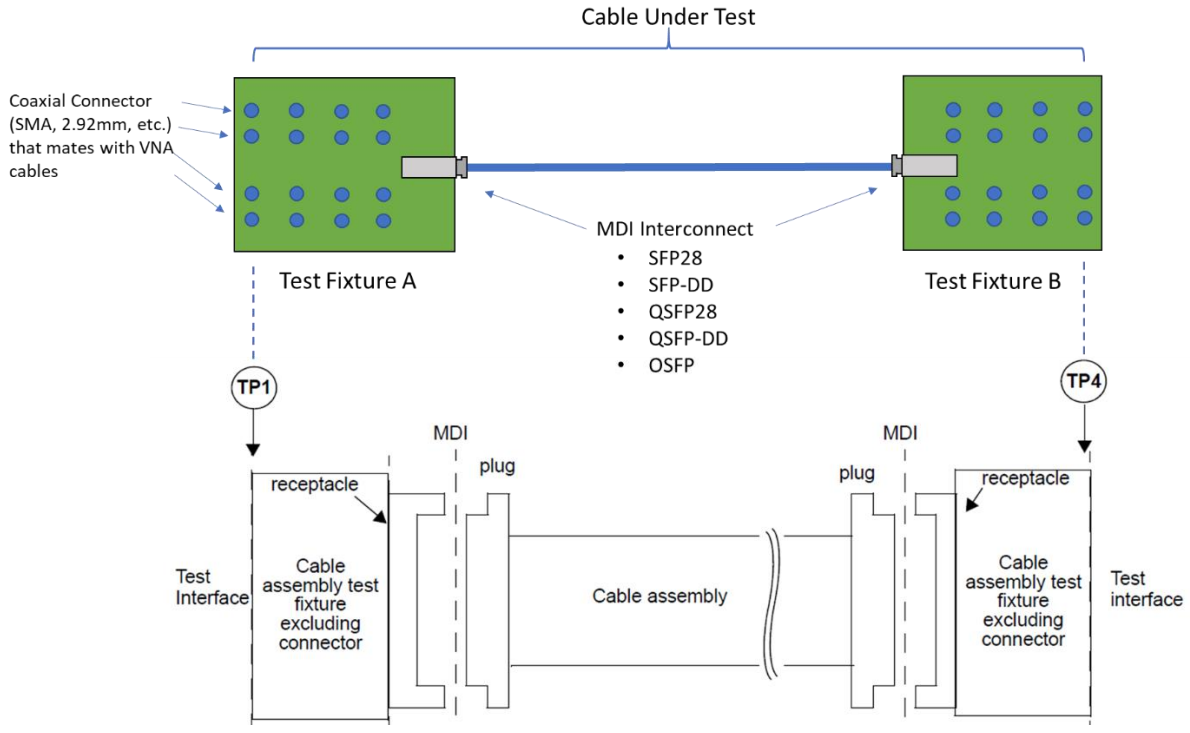


Figure 2: Example of IEEE Test Fixtures with Cable Assembly Under Test [2]

It is worth clarifying that the impairments associated with the MCB test fixture are included in the channel measurements. They are not removed by de-embedding or time gating or any other post-processing calibration method. Instead the IEEE defines additional requirements that determine if a test fixture is sufficient to be used for such applications. Since it is very difficult to accurately isolate the impairments and effects of each side of the MDI interconnect, the IEEE decided to create a "Mated Test Fixture" definition that is measure from TP1 to TP2 across mated HCB and MCB test fixtures. This is shown in Figure 3.

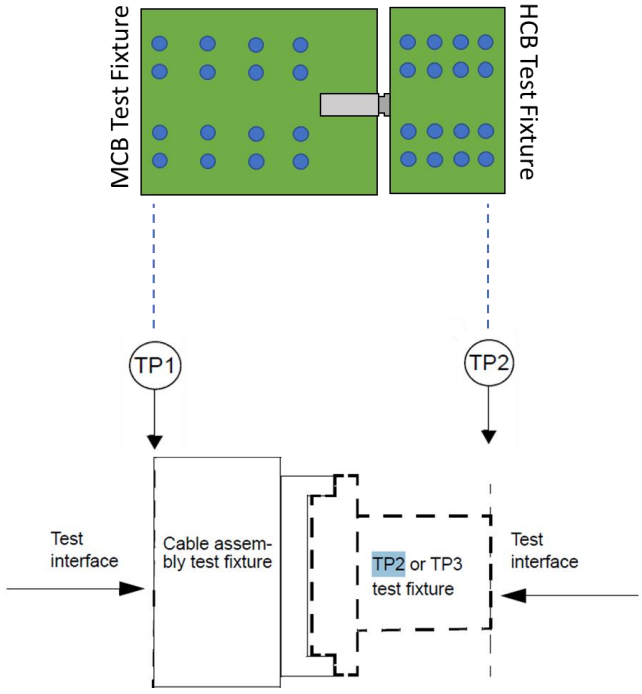


Figure 3: Example of IEEE Mated Text Fixture Set [3]

The mated HCB & MCB parameters, and validation of the conformance of the mated test fixtures, is considered to be outside the scope of this MOI and up to the tester to validate; however, the table below lists the IEEE 802.3 subclauses that include the mated test fixture references.

Specification		Cable Definition			IEEE Mated Test Fixture Definition
IEEE 802.3	802.3bj-2014	Clause 92	100GBASE-CR4		92.11.3
	802.3by-2016	Clause 110	25GBASE-CR	CA-25G-L CA-25G-S CA-25G-N	92.11.3
	802.3cd-2018	Clause 136	50GBASE-CR1 100GBASE-CR2 200GBASE-CR4		Annex 136B.1.1
	P802.3ck Draft 2.0	Clause 162	100GBASE-CR1 200GBASE-CR2 400GBASE-CR4		Annex 162B.1.3

As stated previously, impairments associated with the MCB test fixture are included in the channel measurements. They are not removed by de-embedding or time gating or any other post-processing calibration method. However, this can be done for design development purposes using a Rohde & Schwarz

ZNA, ZNB, or ZNBT network analyzer. The test fixture used will e.g. need to include a '2x Thru' standard to accurately isolate the characteristics of the cable assembly.

4.2 BASE-KR Test Points

Figure 4 shows an entire 100GBASE-KR4 link from PHY to PHY, and the location of all test points defined in Clause 93. This same diagram is applicable to other KR clauses (Clause 111 25GBASE-KR, Clause 137 50GBASE-KR1, etc.) by scaling the number of transmit and receive signals accordingly. Although only two test points are defined, similar naming convention to the BASE-CR PHY test points was adopted to avoid discrepancies and confusion. TP0 and TP5 are specified at the chip interface.

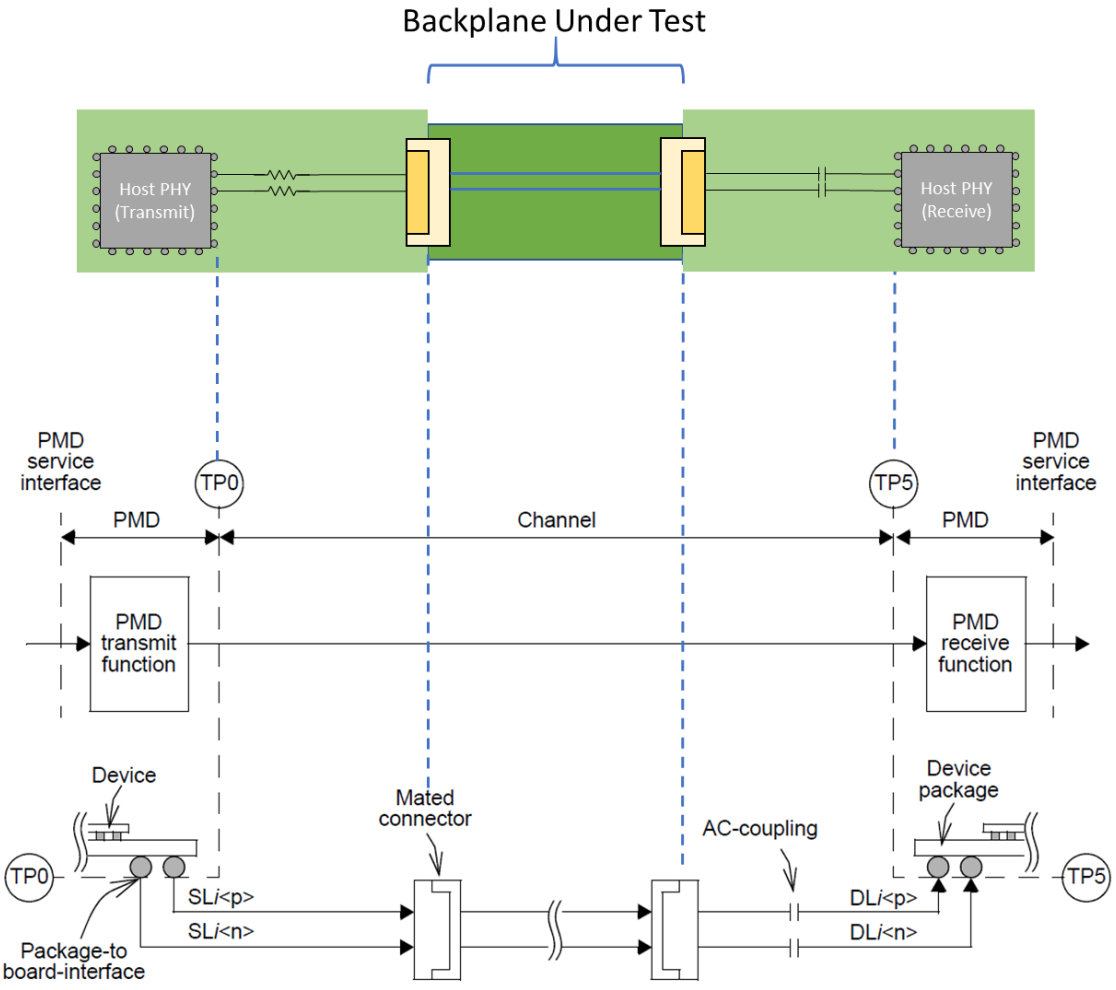


Figure 4: Example of IEEE Backplane Channel and respective Test Points [4]

Backplane channel test points are not as strictly defined as the cable assembly counterpart in BASE-CR clauses. The backplane channel is expected to be measured at the mated connectors, as shown in Figure 4. There are not any additional test fixtures defined for BASE-KR PHYs. Typically, a coaxial connector (such as SMA, 2.92mm, etc.) is exposed to characterize backplane channels. See Figure 5 for an example. It is not defined by the IEEE that such test fixtures are to be de-embedded from the measurement; such a procedure is considered outside the scope of this MOI ; however, this can be done for design development purposes

using a Rohde & Schwarz ZNA, ZNB, or ZNBT network analyzer. The test fixture used will need to include e.g. a '2x Thru' standard to accurately isolate the characteristics of the backplane channel.

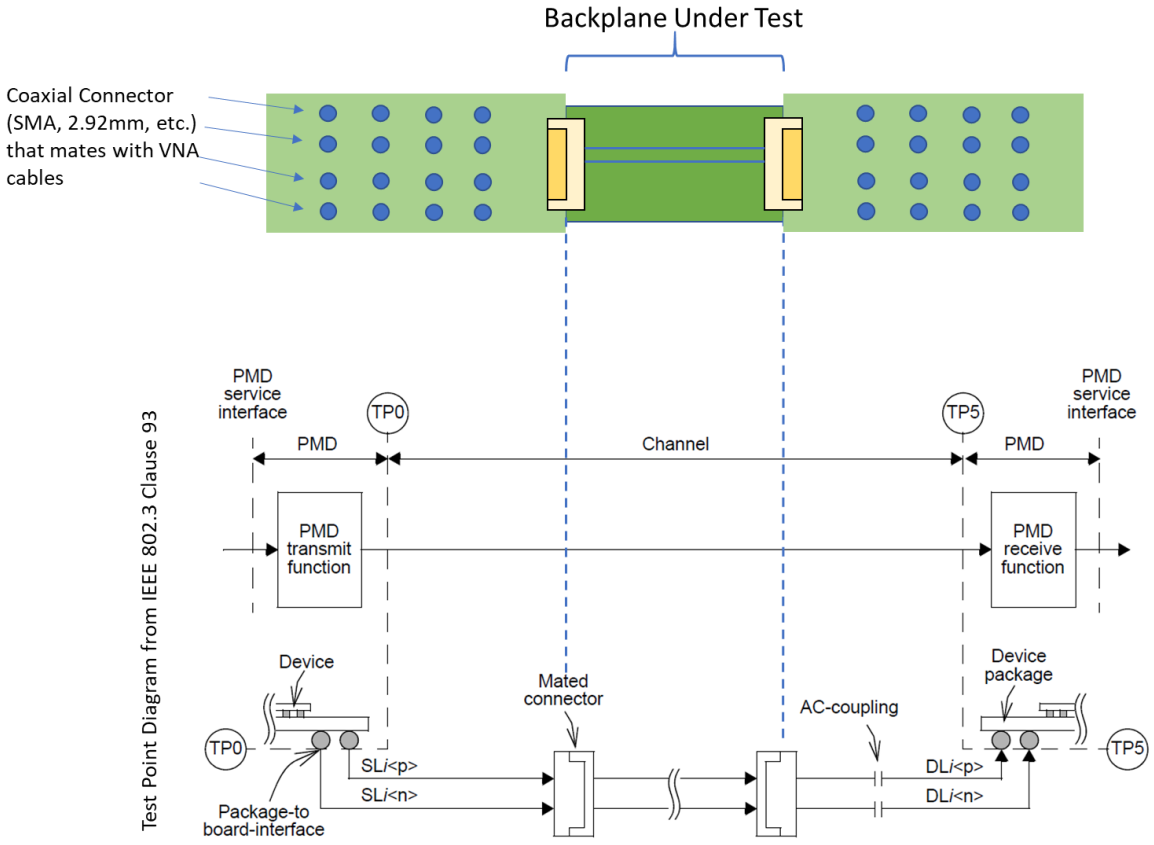


Figure 5: Example of Backplane Test Fixtures with a Backplane Channel Under Test [4]

5 Manual Operation

This section of the document focuses on how to collect data to perform conformance validation for IEEE 802.3 channel specifications. A procedure is provided for collecting all necessary S-parameter files, which are used to verify traditional channel metrics such as differential insertion loss and differential return loss, as well calculating the COM and ERL figures of merit. The following sections explain how this conformance analysis is performed without any assisting automation. Only the IEEE 802.3 provided Matlab scripts are considered for validation.

5.1 Test Preparation

See the Vector Network Analyzer Settings in the Considerations section of Appendix: IEEE Channel Operating Margin (COM) and Effective Return Loss (ERL) Matlab Scripts at the end of this document.

Take care to use the recommended parameters specific to the Ethernet PHY type being tested.

5.2 Recall Setup Files

There are recall files delivered together with this document which makes it more convenient to perform the required measurements. There is one recall file for each IEEE 802.3 specification covered by this MOI.

Recalling the setup files

1. First press the green **PRESET** button on the front panel of the instruments
2. After that press **FILE** button on the front panel
3. Select **Open Recall...** in 'File' menu
4. Open the recall files (*.znx) for the desired tests. In total there are 19 recall files for the different tests associated with each channel type:

1. IEEE_100GBASE-CR4.znx 2. IEEE_25GBASE-CR_CA-25G-L.znx 3. IEEE_25GBASE-CR_CA-25G-S.znx 4. IEEE_25GBASE-CR_CA-25G-N.znx 5. IEEE_50GBASE-CR1.znx 6. IEEE_100GBASE-CR2.znx 7. IEEE_200GBASE-CR4.znx 8. IEEE_100GBASE-KR4.znx 9. IEEE_100GBASE-CR1.znx 10. IEEE_200GBASE-CR2.znx 11. IEEE_400GBASE-CR4.znx	12. IEEE_25GBASE-KR.znx 13. IEEE_25GBASE-KR-S.znx 14. IEEE_50GBASE-KR1.znx 15. IEEE_100GBASE-KR2.znx 16. IEEE_200GBASE-KR4.znx 17. IEEE_100GBASE-KR1.znx 18. IEEE_200GBASE-KR2.znx 19. IEEE_400GBASE-KR4.znx

5. Overview about the setting in the different recall files:

Recall File	Applicable Specification	Start	Stop	Step size	IFBW	Power
ZNA_IEEE_100GBASE-CR4.znx ZNB_IEEE_100GBASE-CR4.znx	IEEE 802.3 Clause 92: 100GBASE-CR4	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_25GBASE-CR_CA-25G-L.znx ZNB_IEEE_25GBASE-CR_CA-25G-L.znx	IEEE 802.3 Clause 110: 25GBASE-CR: CA-25G-L	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_25GBASE-CR_CA-25G-S.znx ZNB_IEEE_25GBASE-CR_CA-25G-S.znx	IEEE 802.3 Clause 110: 25GBASE-CR: CA-25G-S	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_25GBASE-CR_CA-25G-N.znx ZNB_IEEE_25GBASE-CR_CA-25G-N.znx	IEEE 802.3 Clause 110: 25GBASE-CR: CA-25G-N	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_50GBASE-CR1.znx ZNB_IEEE_50GBASE-CR1.znx	IEEE 802.3 Clause 136: 50GBASE-CR1	10 MHz	26.565 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_100GBASE-CR2.znx ZNB_IEEE_100GBASE-CR2.znx	IEEE 802.3 Clause 136: 100GBASE-CR2	10 MHz	26.565 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_200GBASE-CR4.znx ZNB_IEEE_200GBASE-CR4.znx	IEEE 802.3 Clause 136: 200GBASE-CR4	10 MHz	26.565 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_100GBASE-KR4.znx ZNB_IEEE_100GBASE-KR4.znx	IEEE 802.3 Clause 93: 100GBASE-KR4	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_25GBASE-KR.znx ZNB_IEEE_25GBASE-KR.znx	IEEE 802.3 Clause 111: 25GBASE-KR	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_25GBASE-KR-S.znx ZNB_IEEE_25GBASE-KR-S.znx	IEEE 802.3 Clause 111: 25GBASE-KR-S	10 MHz	25.785 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_50GBASE-KR1.znx ZNB_IEEE_50GBASE-KR1.znx	IEEE 802.3 Clause 137: 50GBASE-KR1	10 MHz	26.565 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_100GBASE-KR2.znx ZNB_IEEE_100GBASE-KR2.znx	IEEE 802.3 Clause 137: 100GBASE-KR2	10 MHz	26.565 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_200GBASE-KR4.znx ZNB_IEEE_200GBASE-KR4.znx	IEEE 802.3 Clause 137: 200GBASE-KR4	10 MHz	26.565 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_100GBASE-CR1.znx	* IEEE 802.3 Clause 162: 100GBASE-CR1	10 MHz	50 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_200GBASE-CR2.znx	* IEEE 802.3 Clause 162: 200GBASE-CR2	10 MHz	50 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_400GBASE-CR4.znx	* IEEE 802.3 Clause 162: 400GBASE-CR4	10 MHz	50 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_100GBASE-KR1.znx	* IEEE 802.3 Clause 163: 100GBASE-KR1	10 MHz	50 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_200GBASE-KR2.znx	* IEEE 802.3 Clause 163: 200GBASE-KR2	10 MHz	50 GHz	5 MHz	10 kHz	0 dBm
ZNA_IEEE_400GBASE-KR4.znx	* IEEE 802.3 Clause 163: 400GBASE-KR4	10 MHz	50 GHz	5 MHz	10 kHz	0 dBm

*: At the time of this MOIs creation the IEEE 802.3ck Specification was still being edited. Recall files for Clause 162 and Clause 163 are based on Draft v2.0 (released in March 2021). Due to the increased bandwidth needed for 802.3ck designed channels, only the ZNA product line is listed as appropriate for this testing.

Note that instrument state files between the ZNA and ZNB vector network analysis are not interchangeable. When selecting the file appropriate for the PHY type under test, also take care to select to the instrument state file specific to the VNA model being used.

5.3 Calibration Recommendations

This section described the recommended procedure to calibrating the VNA before collecting the touchstone files needed for processing COM and ERL of a Channel Under Test. The following images are derived from the graphical interface included on a ZNB40 instrument.

1. While the VNA is powered off, connect all necessary accessories including the ZN-Z54 (or applicable) calibration unit.

2. Power on and let the VNA idle for at least 45 minutes. Measurements are very sensitive to changes in temperature, so it is very important that the instrument be running for some time before data is collected, allowing it to acclimate to its internal operating temperature.

3. Launch the VNA software interface if it did not open automatically.

4. Navigate the graphical interface and press the "Preset" button.

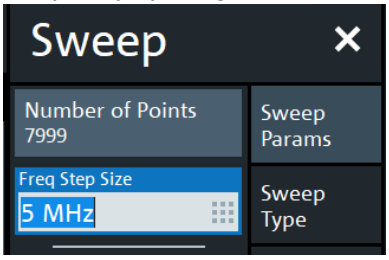
5. Load the appropriate Instrument Configuration file as provided by Rohde & Schwarz for the PHY type to be tested. This is described above in Recall Setup Files

Verify that the following VNA parameters were loaded correctly for the respective PHY under test:

- Balanced Ports: 1-3, 2-4
- Start Frequency: 10 MHz

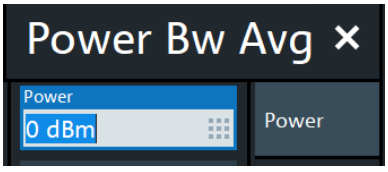
- Stop Frequency: The Stop Frequency is specific to the PHY type under test. The values are as follows:

- 25.7850 GHz for IEEE 802.3bj-2014 & 802.3by-2016 PHY types
- 26.5650 GHz for IEEE 802.3cd-2018 PHY types
- 50 GHz for IEEE P802.3ck Task Force PHY types
- Frequency spacing: 5 MHz



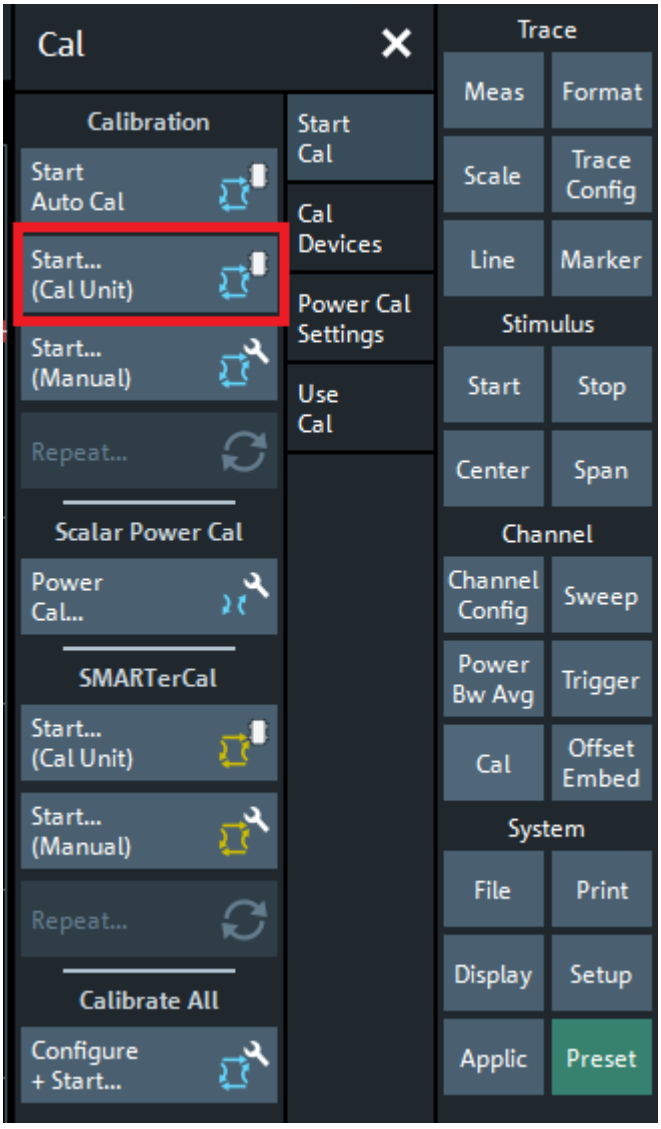
- Intermediate Frequency Bandwidth (IFBW) = 10 KHz

- Power: 0 dBm

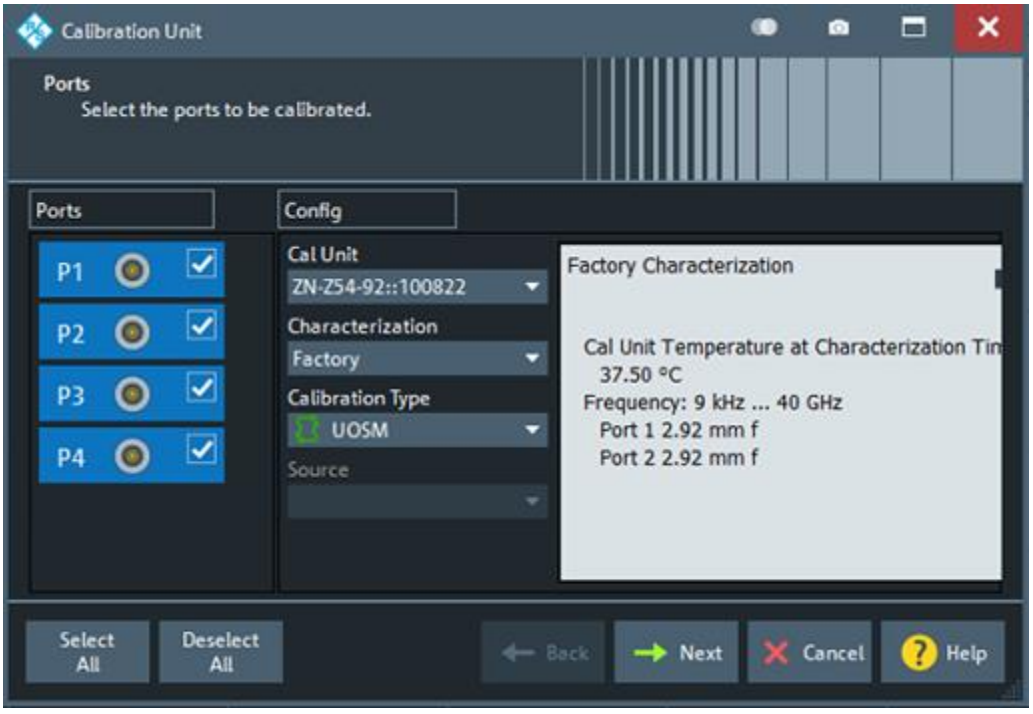


6. Once sufficient time has lapsed to acclimate the internal temperature of the instrument (see step 2), click the "Cal" button in the software menu.

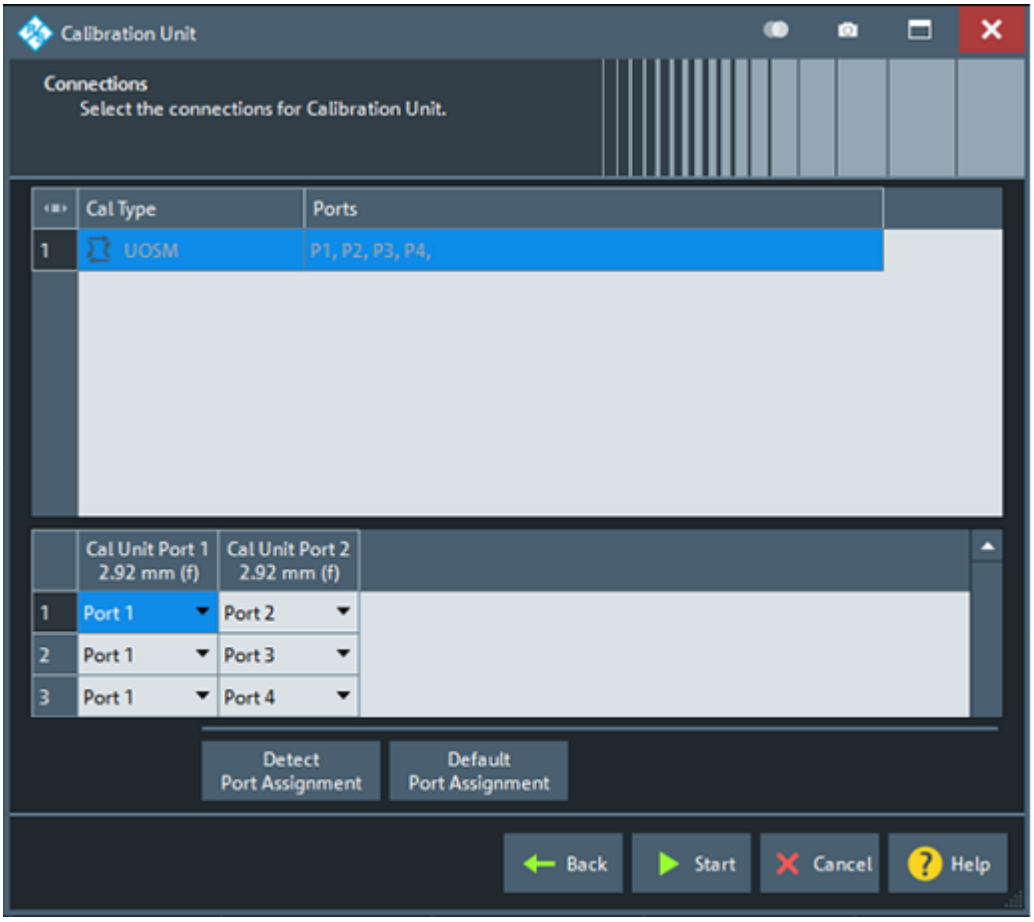
7. Then click "Start … (Cal Unit)", from the submenu that appears.


Cal
Calibration
Start Auto Cal
Start... (Cal Unit)
Start... (Manual)
Repeat...
Scalar Power Cal
Power Cal...
SMARTerCal
Start... (Cal Unit)
Start... (Manual)
Repeat...
Calibrate All
Configure + Start...
Start Cal
Cal Devices
Power Cal Settings
Use Cal
Trace
Meas
Format
Scale
Trace Config
Line
Marker
Stimulus
Start
Stop
Center
Span
Channel
Channel Config
Sweep
Power Bw Avg
Trigger
Cal
Offset Embed
System
File
Print
Display
Setup
Applic
Preset

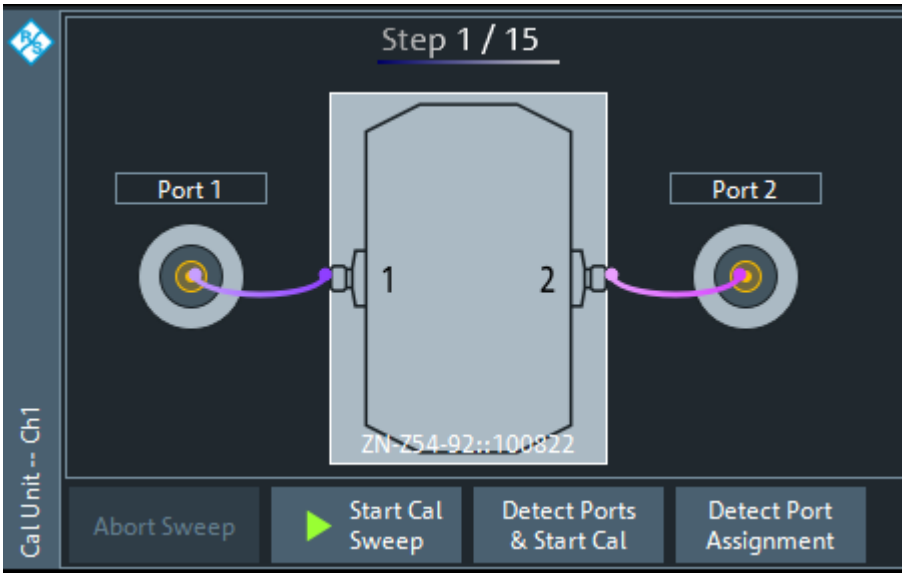
8. A new window will appear in the middle of the screen with information specific to the calibration unit being used. Choose the ports you would like to calibrate (typically this is all 4 ports). Make sure the check box next to each applicable port is selected. Additionally, the user may choose the Calibration Type in this window. If using an automated calibration unit, UOSM is the recommended type. Once all settings are confirmed, press "Next".



9. The next window describes the port combinations to be connected to the calibration unit. The default connects Port 1 to all other ports. Press "Start".



10. Now the graphical interface shows the first port combination to be calibrated. In the bottom left corner of the screen is a diagram of the showing that Port 1 should connect to the left side of the calibration unit, and Port 2 on the right. Once the cables are connected appropriately and sufficiently torqued, click the "Start Cal Sweep" button.



11. Once the sweep for the Port 1 & Port 2 combination is complete, click "Next" in the bottom right corner of the screen.

12. Repeat steps 10 & 11 for the respective port combination specified by the software.

13. Once all port combinations have been calibrated, press the "Save" button in the bottom right corner of the screen.

14. Calibration is complete, and ready to proceed to collecting the necessary touchstone files.

NOTE: Additional calibration, de-embedding, or port extension procedures are not required by the standards covered in this MOI. Instead, the channel conformance parameters specified by IEEE 802.3 are designed assuming a test fixture of a specific loss budget is used during testing. The standards bodies go to great lengths to specify requirements regarding the test fixture characterization, and it is the responsibility of the tester to verify that the set of test fixture module compliance boards (MCB) being used during testing meet these requirements. The test fixture requirements can be found in the respective Clause or section of the standard that defines the PHY type under test. Verification of the MCB test fixtures, or additional de-embedding of the fixtures, is considered outside the scope of this MOI.

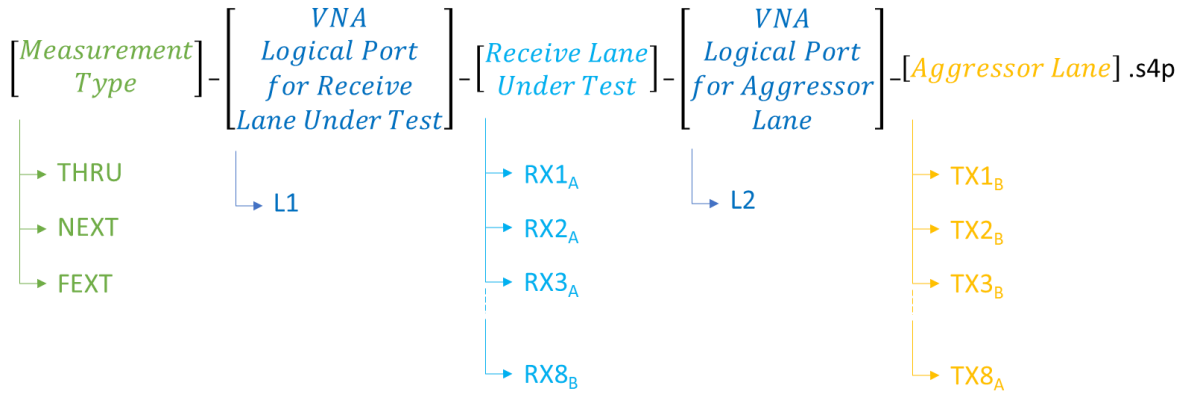
5.4 Compliance Measurements

5.4.1 Introductions

This section defines the test procedures to collect all data necessary to fully characterize a given channel, and validate it to the requirements defined in the respective standards identified in this MOI. This section is divided into two subsections; 5.4.2 describes the channel parameters that can be verified on the VNA (such as differential insertion loss), and 5.4.3 describes the process to collect the s4p files necessary to calculate a channels COM and ERL (which requires additional software processing on a PC).

5.4.1.1 Assumed Pin Assignment

Since several of the PHY types considered in this MOI have multiple transmit lanes, a consistent pin mapping and naming convention is needed to easily describe the test setup and which S-parameter measurements apply to which pins. The following naming convention is recommended,



Below are diagrams for each PHY type (1x, 2x, 4x, or 8x transmit lanes) with touchstone file names using the above formula:

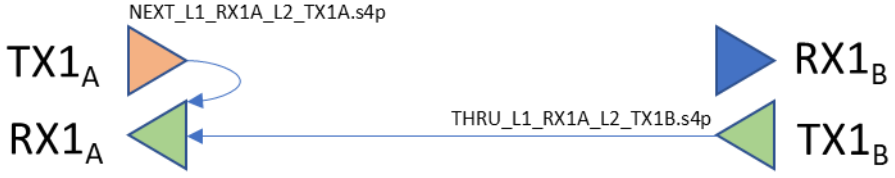


Figure 6: PHY with 1x transmit lanes (CR1/KR1 or equivalent) connections for RX1A Victim

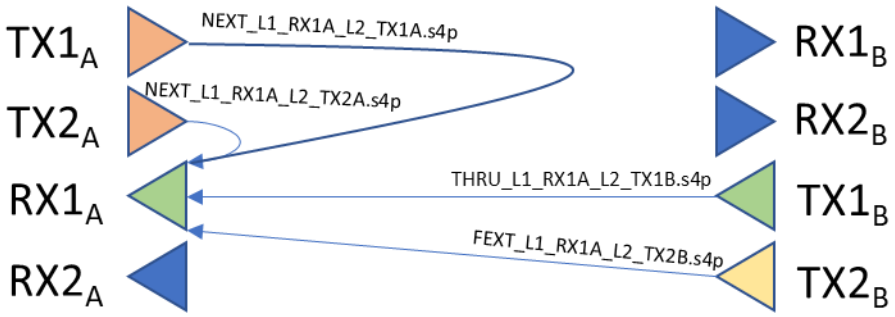


Figure 7: PHY with 2x transmit lanes (CR2/KR2 or equivalent) connections for RX1A Victim

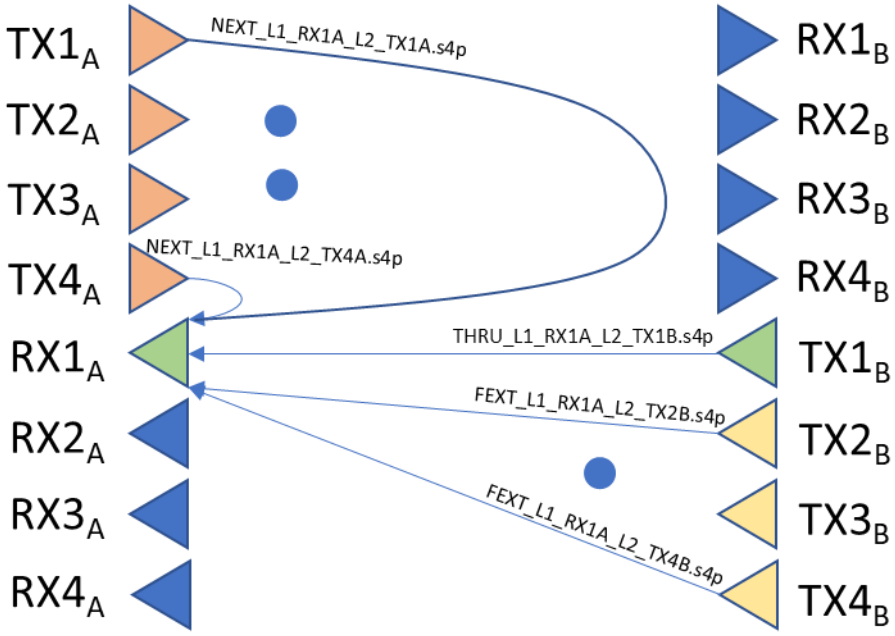


Figure 8: PHY with 4x transmit lanes (CR4/KR4 or equivalent) connections for RX1A Victim

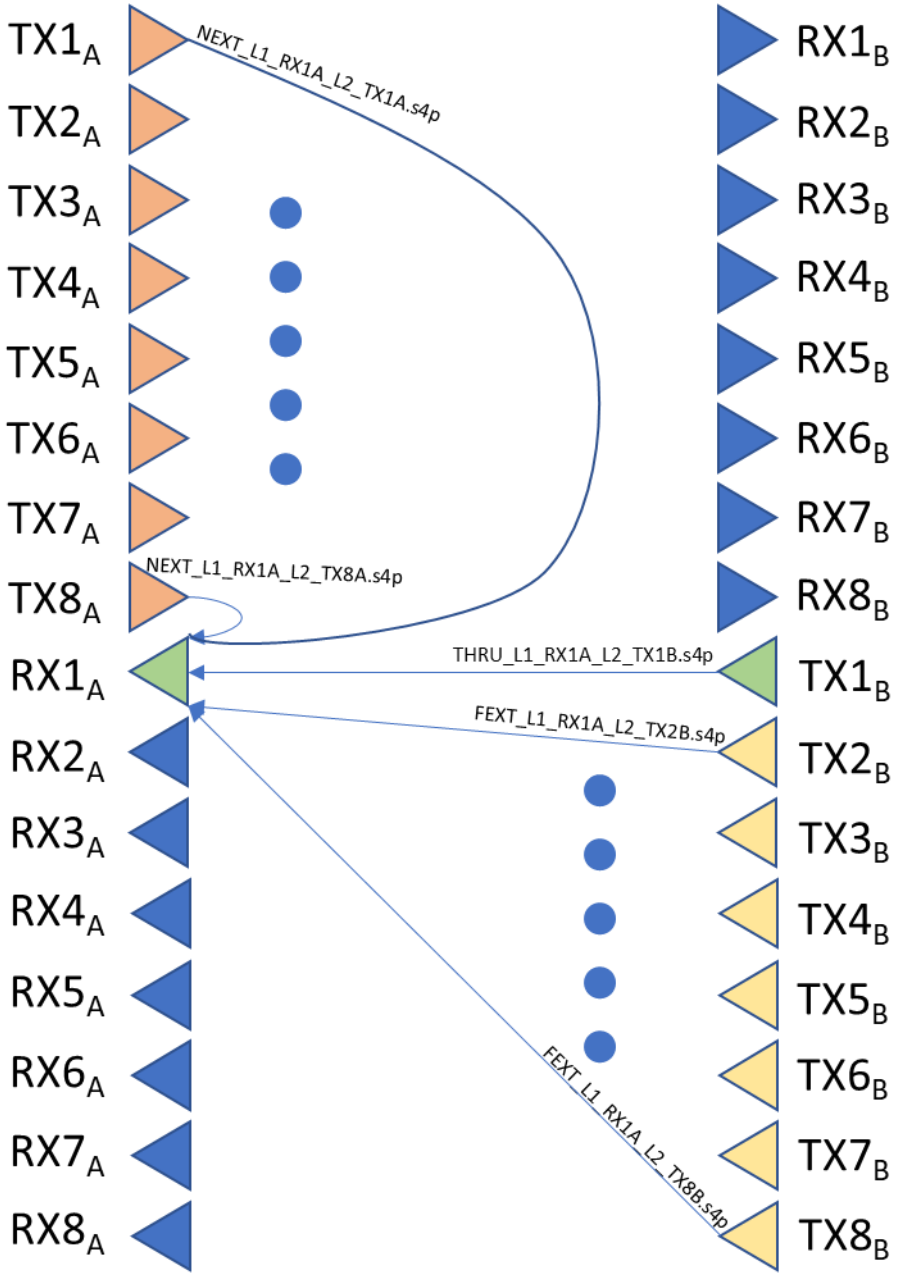


Figure 9: PHY with 8x transmit lanes (CR8/KR8 or equivalent) connections for RX1A Victim

5.4.2 VNA S-Parameter Validation

This section defines the procedure to validate the conformance requirements that do not need additional software to process. The exact S-Parameters with corresponding conformance masks and limits are unique to each PHY type under test. The following is a list of parameters covered:

- ► Differential Insertion Loss - SDD21
- ► Differential Return Loss - SDD11, SDD22
- ► Differential to Common-Mode Return Loss - SCD11, SCD22
- ► Differential to Common-Mode Conversion Loss - SCD21
- ► Common-Mode to Common-Mode Return Loss - SCC11, SCC22

1. Make sure that the VNA is calibrated as specified above, in Calibration Recommendations.

2. Connect the VNA ports to the test fixture interface as follows:

VNA Port 1 to RX1A (+)

VNA Port 3 to RX1A (-)

VNA Port 2 to TX1B (+)

VNA Port 4 to TX1B (-)

For best results, all coaxial connectors for TX and RX lanes that are not connected to the VNA test instrument should be terminated with 50 Ohm loads.

The following procedures assume a 4-lane interface (such as QSFP28) is being tested. This is merely a convenience to the reader, the following instructions apply to all of the interfaces described in Overview.

3. Perform an acquisition of the VNA, collecting the "Thru" measurements of the RX1A lane.

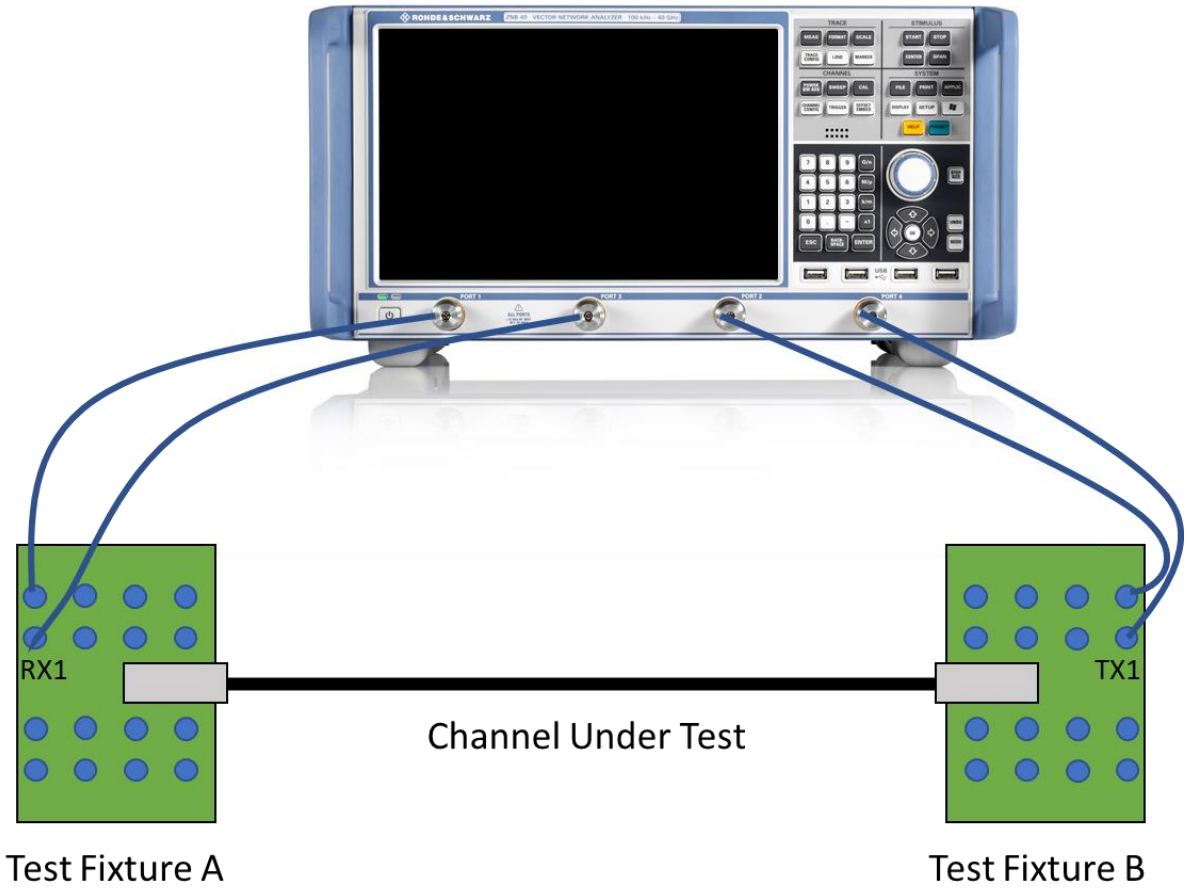


Figure 10: Example QSFP28 setup for RX1A "Thru" measurement

4. Review the individual S-Parameters with associated limit lines in the VNA software interface.

Figure 11: Example of pass and fail indication

5. Repeat Step 3-4 for each additional receive lane on Side A of the channel.
6. Repeat Step 3-5 for Side B (RX1B, etc.) of the channel.
7. Done.

5.4.3 COM & ERL Validation

This section defines the test procedure to collect all data to characterize the COM and ERL.

1. Make sure that the VNA is calibrated as specified above, in Calibration Recommendations.

2. Connect the VNA ports to the test fixture interface as follows:

VNA Port 1 to RX1A (+)

VNA Port 3 to RX1A (-)

VNA Port 2 to TX1B (+)

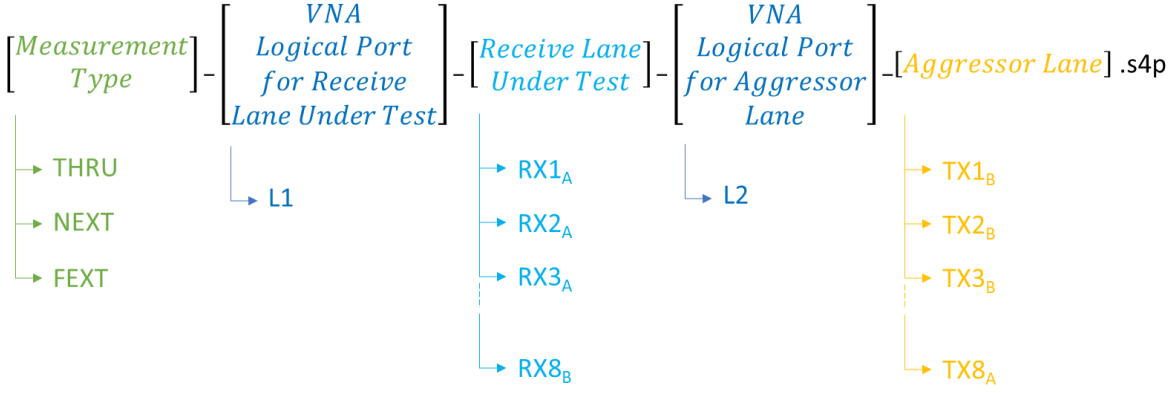
VNA Port 4 to TX1B (-)

For best results, all coaxial connectors for TX and RX lanes that are not connected to the VNA test instrument should be terminated with 50 Ohm loads.

The following procedures assume a 4-lane interface (such as QSFP28) is being tested. This is merely a convenience to the reader, the following instructions apply to all of the interfaces described in Overview.

NOTE: The COM/ERL Matlab scripts assume the touchstone files to be processed are measured in a 4-port setup, so the remainder of the procedures in this section will assume that a 4-port setup is being used. If a VNA configuration of >4 ports is used for collecting all necessary data, it is necessary to derive an .S4P equivalent of the touchstone files saved before being able to proceed to Step 6. See Appendix: Recommended VNA Port Mapping for suggested port configuration for ZNB40 and ZNA43.

3. Save all necessary touchstone files for receiver lane RX1A. The following naming convention is recommended:

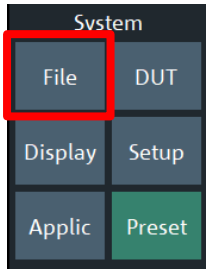


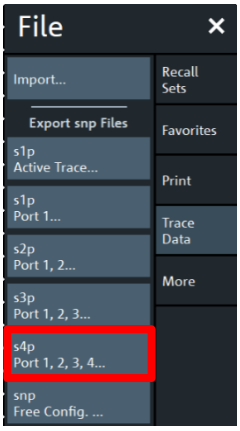
For example, when collecting the touchstone file which includes the differential insertion loss and differential return loss of receiver RX1A, or the RX1A "Thru" file, the file name would be:

THRU_L1_ RX1A_L2_TX1B.s4p

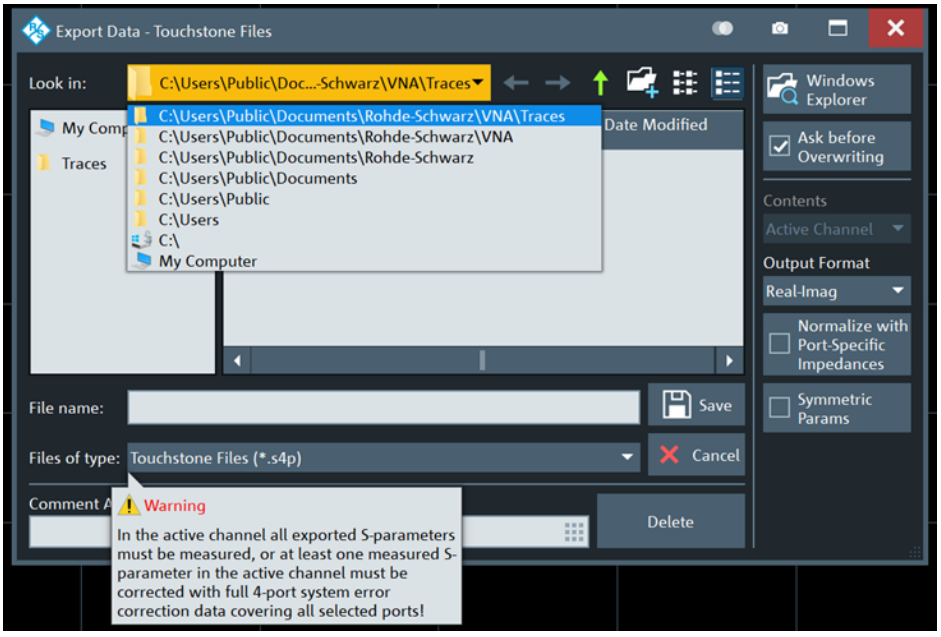
A full list of all s4p touchstone file names, following the above convention, is provided in Appendix: Recommended VNA Port Mapping.

The s4p file can be saved by selecting File > Trace Data > s4p Port 1,2,3,4…





Lastly, manually enter the name as described above.



a. Collect the “Thru” touchstone. Save as 'THRU_L1_ RX1A_L2_TX1B.s4p'.

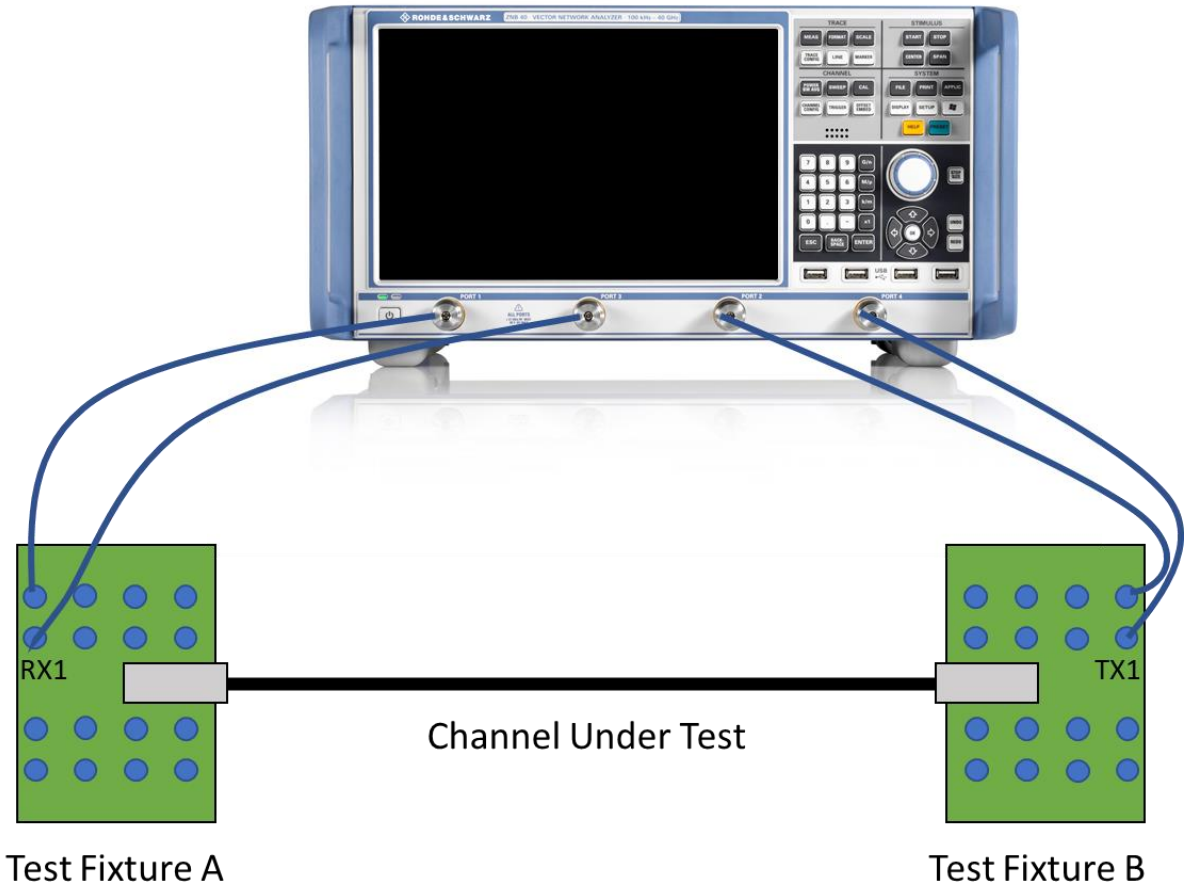


Figure 12: Example QSFP28 setup for RX1A "Thru" measurement

b. Collect the “NEXT” touchstone file(s). Save as 'NEXT_L1_ RX1A_L2_TX1A.s4p', 'NEXT_L1_ RX1A_L2_TX2A.s4p', 'NEXT_L1_ RX1A_L2_TX3A.s4p', and 'NEXT_L1_ RX1A_L2_TX4A.s4p', respectively.

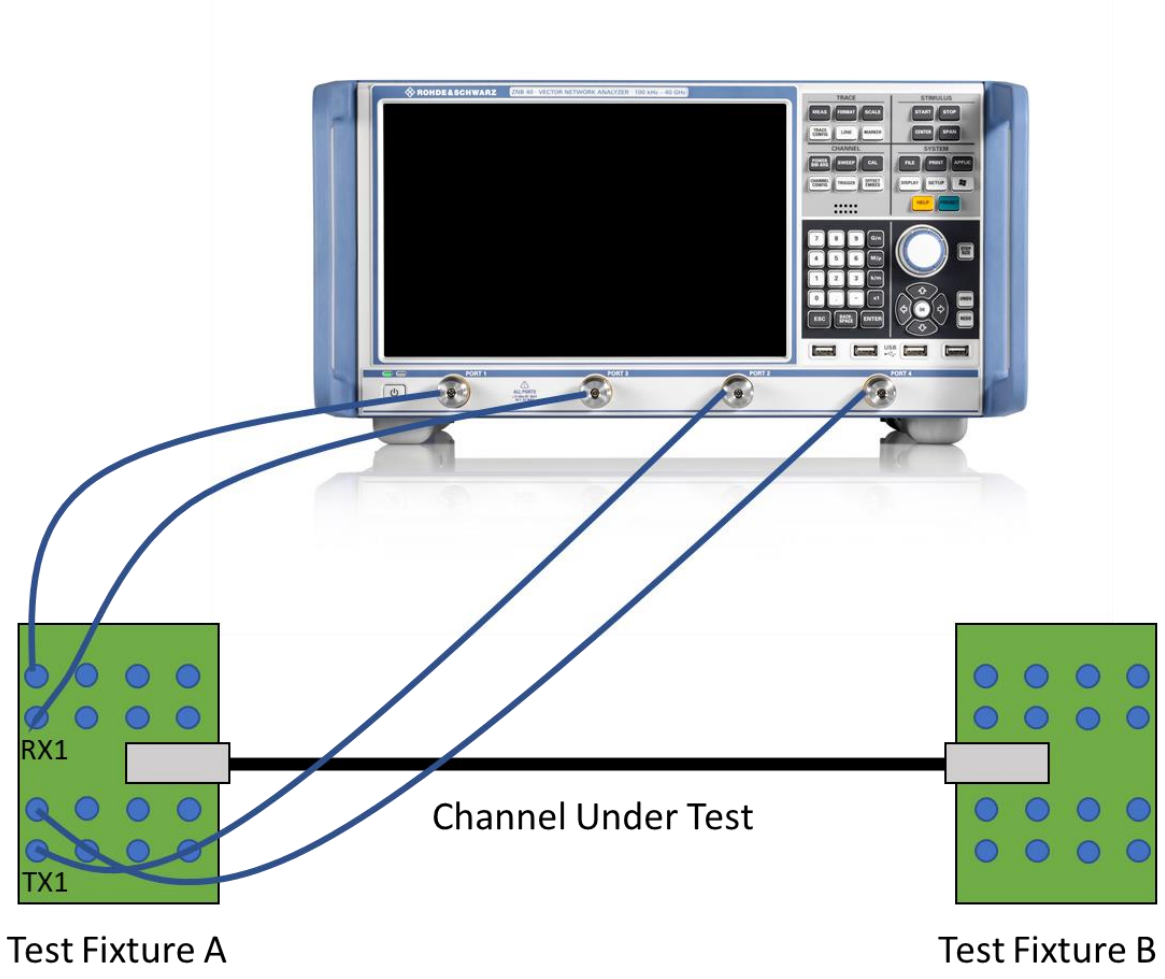


Figure 13: Example QSFP28 setup for RX1A "NEXT" measurement from TX1A

c. Collect the “FEXT” touchstone file(s). Save as ' FEXT_L1_ RX1A_L2_TX2B.s4p', 'FEXT_L1_ RX1A_L2_TX3B.s4p', and 'FEXT_L1_ RX1A_L2_TX4B.s4p', respectively.

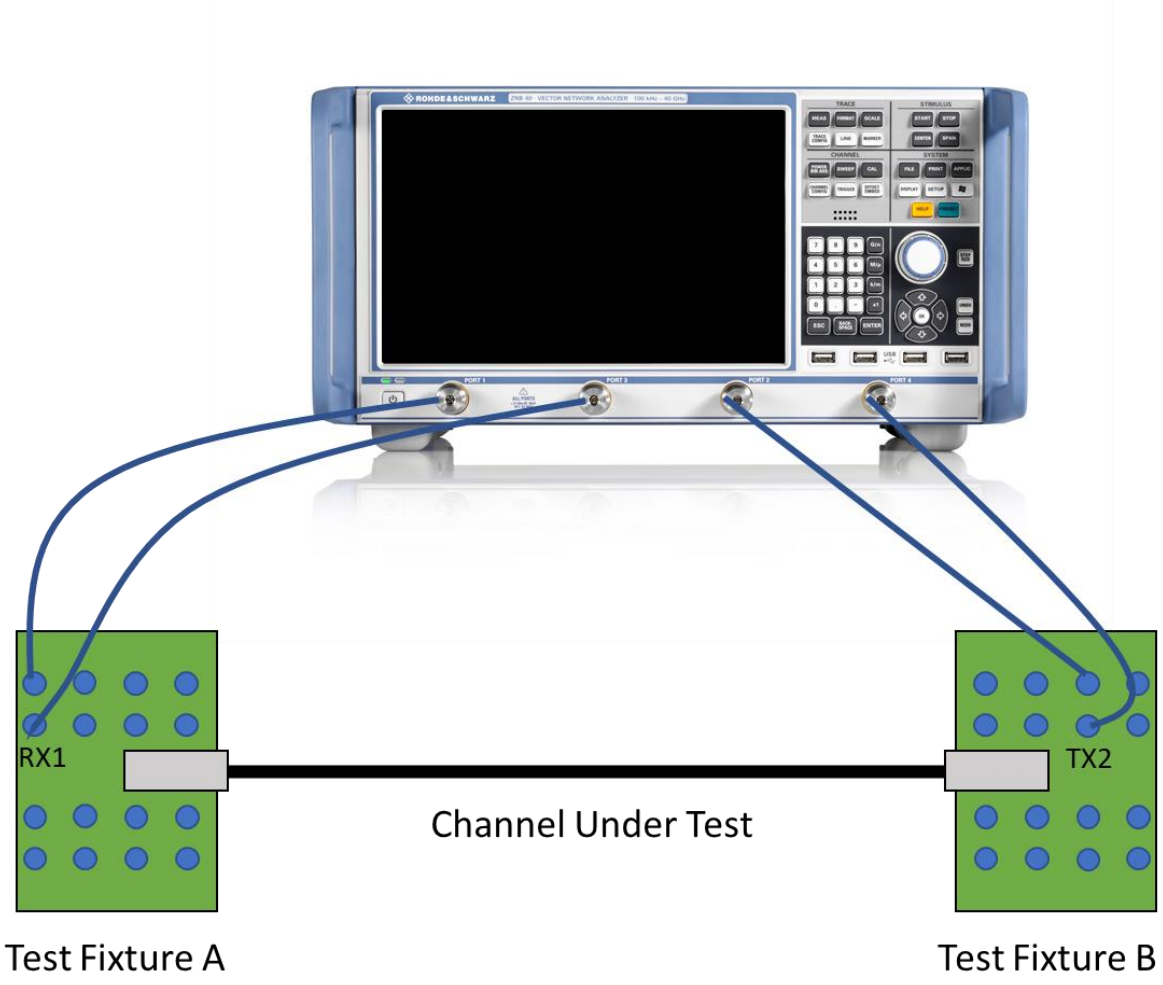


Figure 14: Example QSFP28 setup for RX1A "FEXT" measurement from TX2B

4. Repeat Step 3 for each additional receive lane on Side A of the channel.
5. Repeat Step 3-4 for Side B (RX1B, etc.) of the channel.
6. Execute the COM/ERL scripts as described in Appendix: IEEE Channel Operating Margin (COM) and Effective Return Loss (ERL) Matlab Scripts with the data collected in Step 3.
7. Repeat Step 6 for each receive lane on Side A, as collected in Step 4.
8. Repeat Step 6 for each receive lane on Side B, as collected in Step 5.
9. Done.

6 Channel Operating Margin (COM) and Effective Return Loss (ERL) Matlab Scripts

6.1 Introduction

The IEEE 802.3 Working Group adopted COM and ERL as channel metrics for several 25+ Gbps serial interfaces. The underlying post-processing functions of COM and ERL are too extensive and complicated to include within the IEEE 802.3 Standard text, instead the IEEE 802.3 Working Group published Matlab scripts necessary to calculate the COM and ERL conformance values. The scripts were created in Matlab by IEEE 802.3 Working Group participants. Each specification has a unique Matlab script and Excel XLS configuration file that is publicly available for review and use, the Matlab scripts for the IEEE definitions can be found at the respective links below:

- IEEE 802.3bj-2014
- IEEE 802.3by-2016
- IEEE 802.3cd-2018
- IEEE P802.3ck Task Force (currently in-development)

6.2 Assumptions

This document assumes that the reader has successfully downloaded the appropriate COM/ERL scripts for their respective product and has the necessary licenses to run a Matlab environment to process channel measurements. Given that the Matlab environment is setup correctly, the COM/ERL scripts will run without error. Any errors witnessed when running the Matlab scripts are up to the user to resolve and outside the scope of this MOI.

This document also assumes that the user can collect the necessary touchstone files to accurately characterize the COM and ERL of the device under test. The exact procedure for collecting touchstone files on vector network analyzers not explicitly listed in this document is outside the scope of this MOI. Additionally, it is assumed that the test fixtures used for collecting the channel characteristics meets the test fixture requirements of the respective PHY interface being tested. This is up to the tester to verify.

6.3 Considerations

To properly run the COM/ERL Matlab scripts for conformance validation, the following needs to be considered:

- All lanes in a channel/cable assembly are required to be validated
  The COM/ERL Matlab scripts are run for each lane in a cable assembly individually. Performing COM analysis on a single lane is not sufficient to validate the conformance of a channel.

- COM Configuration XLS File
  COM/ERL are figures of merit that are meant to indicate signal quality at the receiver of a Host PHY. To accurately determine the signal quality at the end of a channel, characteristics of the input signal to the channel under test from the transmitter of the link partner PHY need to be known. Complimenting each Matlab script is an xls file that includes default transmitter parameters used for conformance validation. These values can be adjusted for internal development, but the original values (as provided by IEEE 802.3) are required to be used when validating conformance.
- COM/ERL is defined in reference to the receiver of a Host device
  COM/ERL are figures of merit that are meant to indicate signal quality at the receiver of a Host PHY. As such, all touchstone files need to be measured in reference to a receive lane (ie RX1A, RX2A, etc.). This means that all touchstone files associated with a crosstalk aggressor are to be stimulated at the respective TX aggressor input and observed at the RX victim output under test.
- Number of Touchstone files
  For full conformance validation, the user is required to measure all S-parameters of the victim lane. This results in multiple touchstone files per lane under test. For each lane in a channel/cable assembly, the following is required:
  - "Thru" measurement: Touchstone file which includes the differential insertion loss and differential return loss of the lane under test. There is always one "Thru" for each victim lane.
  - "NEXT" measurement(s): Touchstone file which includes the S-parameter data associated with near-end crosstalk aggressors in the assembly. The number of NEXT aggressors is dependent on the specific mechanical interface being tested. The number of "NEXT" measurements for each interface is as follows:
    - SFP28: One NEXT measurement
    - SFP-DD: Two NEXT measurement
    - QSFP28: Four NEXT measurement
    - QSFP-DD: Eight NEXT measurement
  - "FEXT" measurement(s): Touchstone file which includes the S-parameter data associated with Far-end crosstalk aggressors in the assembly. The number of FEXT aggressors is dependent on the specific mechanical interface being tested. The number of "FEXT" measurements for each interface is as follows:
    - SFP28: Zero FEXT measurement
    - SFP-DD: One FEXT measurement
    - QSFP28: Three FEXT measurement
    - QSFP-DD: Seven FEXT measurement
- Vector Network Analyzer Settings
  To accurately validate the COM and ERL of a channel, the following minimum VNA settings need to be applied:
  - Start Frequency: 10 MHz or less
  - Stop Frequency: typically use fb
    - IEEE 802.3bj-2014 & 802.3by-2016 PHY types: fb = 25.78500 GHz
    - IEEE 802.3cd-2018 PHY types: fb = 26.5650 GHz
    - IEEE P802.3ck Task Force PHY types: fb = 53.12500 GHz, use 50GHz (test fixture max. freq.)
  - Frequency spacing: 5 MHz or less

– Intermediate Frequency Bandwidth (IFBW) = 10 kHz or lower

– VNA settings for collected touchstone files need to be applied uniformly to all files per victim lane

6.4 Running Matlab Script

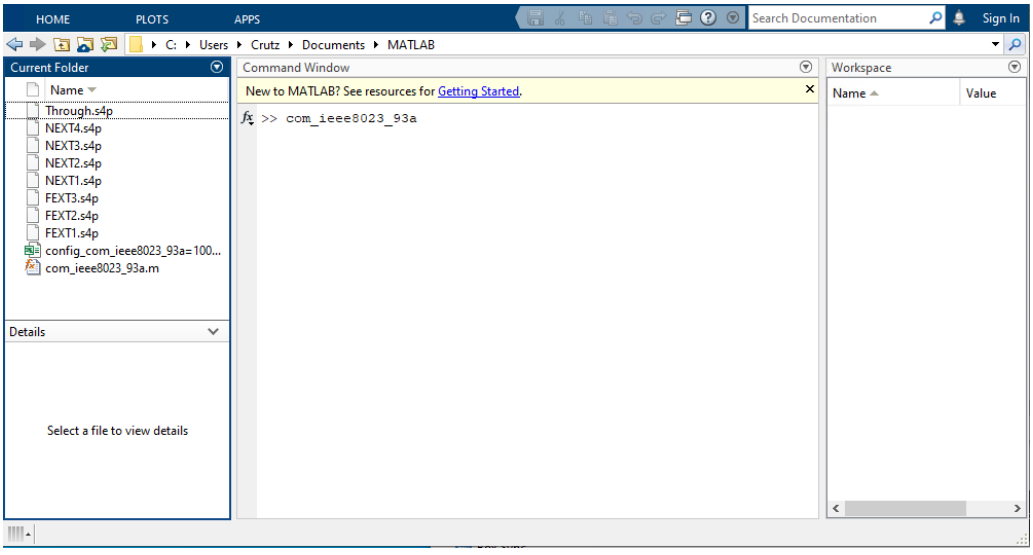
When all necessary touchstone files have been collected, the Matlab script is ready to be run. Each COM/ERL script has four input variables:

com_ieee8023_93a(config_file, num_fext, num_next, [<s4p files>])

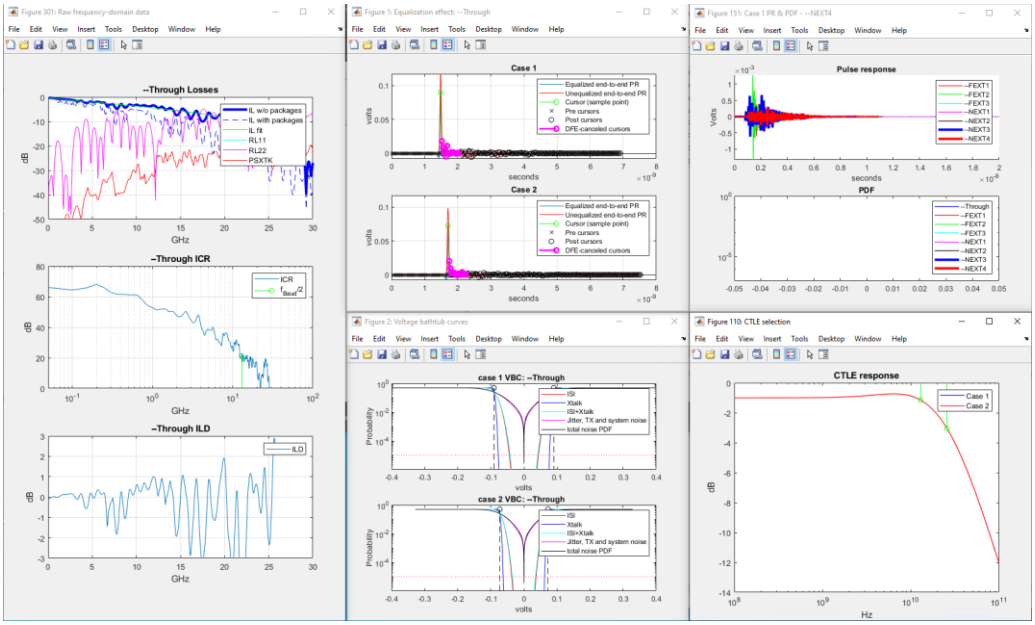
- config_file: This parameter value is a string with the full file path of the xls configuration file.
- num_fext: This parameter is an integer, specific to the number of far-end crosstalk aggressors associated with the interface being tested.
- num_next: This parameter is an integer, specific to the number of near-end crosstalk aggressors associated with the interface being tested.
- <s4p_files>: This parameter is a Matlab structure of touchstone filenames.

If the variables are not supplied by the user, the program will ask for each of them interactively.

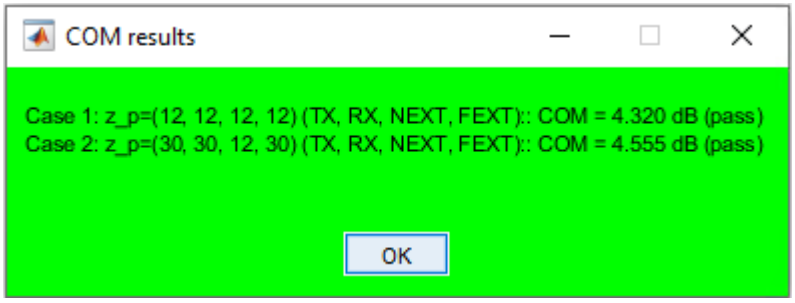
When the above input variables are accurately submitted, the Matlab functions will begin processing the touchstone files collected.

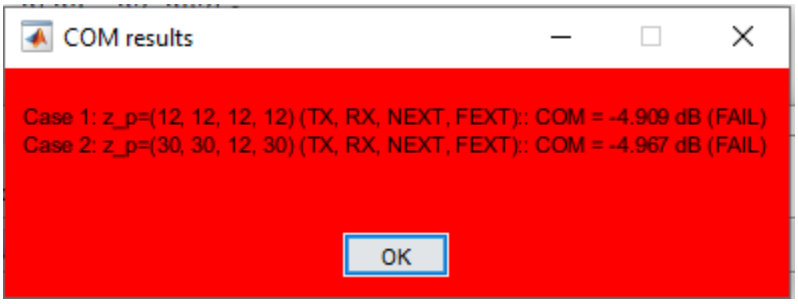


Many informative plots and diagrams are generated.



The conformance COM and ERL values are presented in a text box, as shown below. Values ≥3.0 dB are passing (presented with a green text box), and values <3.0 are failing (presented with a red text box).





The two 'cases' listed in the COM result box are indicative of an assumed frontend package length in the Host transmit and receive paths. At the time of creating this MOI all of the PHY types that include COM as a conformance metric used the same package length values, "Case 1" refers to a Host TX trace length of 12 mm, RX trace length of 12 mm, NEXT trace length of 12 mm, and FEXT trace length of 12 mm. "Case 2" refers to a Host TX trace length of 30 mm, RX trace length of 30 mm, NEXT trace length of 12 mm, and FEXT trace length of 30 mm.

7 Recommended VNA Port Mapping

7.1 Introduction

PHY with 1x Transmit lane (CR/KR & CR1/KR1 or equivalent) s4p file names

	Measurement	Receiver Under Test	VNA Logical Port		Aggressor	VNA Logical Port		Export Name
1	THRU	RX1A	L1	1, 3	TX1B	L2	2, 4	THRU_L1_RX1A_L2_TX1B.s4p
2	NEXT	RX1A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX1A_L2_TX1A.s4p
3	THRU	RX1B	L1	1, 3	TX1A	L2	2, 4	THRU_L1_RX1B_L2_TX1A.s4p
4	NEXT	RX1B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX1B_L2_TX1B.s4p

PHY with 2x Transmit Lanes (CR2/KR2 or equivalent) s4p file names

	Measurement	Receiver Under Test	VNA Logical Port		Aggressor	VNA Logical Port		Export Name
1	THRU	RX1A	L1	1, 3	TX1B	L2	2, 4	THRU_L1_RX1A_L2_TX1B.s4p
2	NEXT	RX1A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX1A_L2_TX1A.s4p
3	NEXT	RX1A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX1A_L2_TX2A.s4p
4	FEXT	RX1A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX1A_L2_TX2B.s4p
5	THRU	RX2A	L1	1, 3	TX2B	L2	2, 4	THRU_L1_RX2A_L2_TX2B.s4p
6	NEXT	RX2A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX2A_L2_TX1A.s4p
7	NEXT	RX2A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX2A_L2_TX2A.s4p
8	FEXT	RX2A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX2A_L2_TX1B.s4p
9	THRU	RX1B	L1	1, 3	TX1A	L2	2, 4	THRU_L1_RX1B_L2_TX1A.s4p
10	NEXT	RX1B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX1B_L2_TX1B.s4p
11	NEXT	RX1B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX1B_L2_TX2B.s4p
12	FEXT	RX1B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX1B_L2_TX2A.s4p
13	THRU	RX2B	L1	1, 3	TX2A	L2	2, 4	THRU_L1_RX2B_L2_TX2A.s4p
14	NEXT	RX2B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX2B_L2_TX1B.s4p
15	NEXT	RX2B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX2B_L2_TX2B.s4p

16	FEXT	RX2B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX2B_L2_TX1A.s4p

PHY with 4x Transmit Lanes (CR4/KR4 or equivalent) s4p file names

	Measurement	Receiver Under Test	VNA Logical Port		Aggressor	VNA Logical Port		Export Name
1	THRU	RX1A	L1	1, 3	TX1B	L2	2, 4	THRU_L1_RX1A_L2_TX1B.s4p
2	NEXT	RX1A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX1A_L2_TX1A.s4p
3	NEXT	RX1A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX1A_L2_TX2A.s4p
4	NEXT	RX1A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX1A_L2_TX3A.s4p
5	NEXT	RX1A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX1A_L2_TX4A.s4p
6	FEXT	RX1A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX1A_L2_TX2B.s4p
7	FEXT	RX1A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX1A_L2_TX3B.s4p
8	FEXT	RX1A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX1A_L2_TX4B.s4p
9	THRU	RX2A	L1	1, 3	TX2B	L2	2, 4	THRU_L1_RX2A_L2_TX2B.s4p
10	NEXT	RX2A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX2A_L2_TX1A.s4p
11	NEXT	RX2A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX2A_L2_TX2A.s4p
12	NEXT	RX2A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX2A_L2_TX3A.s4p
13	NEXT	RX2A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX2A_L2_TX4A.s4p
14	FEXT	RX2A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX2A_L2_TX1B.s4p
15	FEXT	RX2A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX2A_L2_TX3B.s4p
16	FEXT	RX2A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX2A_L2_TX4B.s4p
17	THRU	RX3A	L1	1, 3	TX3B	L2	2, 4	THRU_L1_RX3A_L2_TX3B.s4p
18	NEXT	RX3A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX3A_L2_TX1A.s4p
19	NEXT	RX3A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX3A_L2_TX2A.s4p
20	NEXT	RX3A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX3A_L2_TX3A.s4p
21	NEXT	RX3A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX3A_L2_TX4A.s4p
22	FEXT	RX3A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX3A_L2_TX1B.s4p
23	FEXT	RX3A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX3A_L2_TX2B.s4p
24	FEXT	RX3A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX3A_L2_TX4B.s4p
25	THRU	RX4A	L1	1, 3	TX4B	L2	2, 4	THRU_L1_RX4A_L2_TX4B.s4p

26	NEXT	RX4A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX4A_L2_TX1A.s4p
27	NEXT	RX4A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX4A_L2_TX2A.s4p
28	NEXT	RX4A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX4A_L2_TX3A.s4p
29	NEXT	RX4A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX4A_L2_TX4A.s4p
30	FEXT	RX4A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX4A_L2_TX1B.s4p
31	FEXT	RX4A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX4A_L2_TX2B.s4p
32	FEXT	RX4A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX4A_L2_TX3B.s4p
33	THRU	RX1B	L1	1, 3	TX1A	L2	2, 4	THRU_L1_RX1B_L2_TX1A.s4p
34	NEXT	RX1B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX1B_L2_TX1B.s4p
35	NEXT	RX1B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX1B_L2_TX2B.s4p
36	NEXT	RX1B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX1B_L2_TX3B.s4p
37	NEXT	RX1B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX1B_L2_TX4B.s4p
38	FEXT	RX1B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX1B_L2_TX2A.s4p
39	FEXT	RX1B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX1B_L2_TX3A.s4p
40	FEXT	RX1B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX1B_L2_TX4A.s4p
41	THRU	RX2B	L1	1, 3	TX2A	L2	2, 4	THRU_L1_RX2B_L2_TX2A.s4p
42	NEXT	RX2B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX2B_L2_TX1B.s4p
43	NEXT	RX2B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX2B_L2_TX2B.s4p
44	NEXT	RX2B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX2B_L2_TX3B.s4p
45	NEXT	RX2B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX2B_L2_TX4B.s4p
46	FEXT	RX2B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX2B_L2_TX1A.s4p
47	FEXT	RX2B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX2B_L2_TX3A.s4p
48	FEXT	RX2B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX2B_L2_TX4A.s4p
49	THRU	RX3B	L1	1, 3	TX3A	L2	2, 4	THRU_L1_RX3B_L2_TX3A.s4p
50	NEXT	RX3B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX3B_L2_TX1B.s4p
51	NEXT	RX3B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX3B_L2_TX2B.s4p
52	NEXT	RX3B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX3B_L2_TX3B.s4p
53	NEXT	RX3B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX3B_L2_TX4B.s4p
54	FEXT	RX3B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX3B_L2_TX1A.s4p
55	FEXT	RX3B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX3B_L2_TX2A.s4p

56	FEXT	RX3B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX3B_L2_TX4A.s4p
57	THRU	RX4B	L1	1, 3	TX4A	L2	2, 4	THRU_L1_RX4B_L2_TX4A.s4p
58	NEXT	RX4B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX4B_L2_TX1B.s4p
59	NEXT	RX4B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX4B_L2_TX2B.s4p
60	NEXT	RX4B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX4B_L2_TX3B.s4p
61	NEXT	RX4B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX4B_L2_TX4B.s4p
62	FEXT	RX4B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX4B_L2_TX1A.s4p
63	FEXT	RX4B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX4B_L2_TX2A.s4p
64	FEXT	RX4B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX4B_L2_TX3A.s4p

PHY with 8x Transmit Lanes (CR8/KR8 or equivalent) s4p file names

	Measurement	Receiver Under Test	VNA Logical Port		Aggressor	VNA Logical Port		Export Name
1	THRU	RX1A	L1	1, 3	TX1B	L2	2, 4	THRU_L1_RX1A_L2_TX1B.s4p
2	NEXT	RX1A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX1A_L2_TX1A.s4p
3	NEXT	RX1A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX1A_L2_TX2A.s4p
4	NEXT	RX1A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX1A_L2_TX3A.s4p
5	NEXT	RX1A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX1A_L2_TX4A.s4p
6	NEXT	RX1A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX1A_L2_TX5A.s4p
7	NEXT	RX1A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX1A_L2_TX6A.s4p
8	NEXT	RX1A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX1A_L2_TX7A.s4p
9	NEXT	RX1A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX1A_L2_TX8A.s4p
10	FEXT	RX1A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX1A_L2_TX2B.s4p
11	FEXT	RX1A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX1A_L2_TX3B.s4p
12	FEXT	RX1A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX1A_L2_TX4B.s4p
13	FEXT	RX1A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX1A_L2_TX5B.s4p
14	FEXT	RX1A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX1A_L2_TX6B.s4p
15	FEXT	RX1A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX1A_L2_TX7B.s4p
16	FEXT	RX1A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX1A_L2_TX8B.s4p
17	THRU	RX2A	L1	1, 3	TX2B	L2	2, 4	THRU_L1_RX2A_L2_TX2B.s4p

18	NEXT	RX2A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX2A_L2_TX1A.s4p
19	NEXT	RX2A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX2A_L2_TX2A.s4p
20	NEXT	RX2A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX2A_L2_TX3A.s4p
21	NEXT	RX2A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX2A_L2_TX4A.s4p
22	NEXT	RX2A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX2A_L2_TX5A.s4p
23	NEXT	RX2A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX2A_L2_TX6A.s4p
24	NEXT	RX2A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX2A_L2_TX7A.s4p
25	NEXT	RX2A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX2A_L2_TX8A.s4p
26	FEXT	RX2A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX2A_L2_TX1B.s4p
27	FEXT	RX2A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX2A_L2_TX3B.s4p
28	FEXT	RX2A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX2A_L2_TX4B.s4p
29	FEXT	RX2A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX2A_L2_TX5B.s4p
30	FEXT	RX2A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX2A_L2_TX6B.s4p
31	FEXT	RX2A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX2A_L2_TX7B.s4p
32	FEXT	RX2A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX2A_L2_TX8B.s4p
33	THRU	RX3A	L1	1, 3	TX3B	L2	2, 4	THRU_L1_RX3A_L2_TX3B.s4p
34	NEXT	RX3A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX3A_L2_TX1A.s4p
35	NEXT	RX3A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX3A_L2_TX2A.s4p
36	NEXT	RX3A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX3A_L2_TX3A.s4p
37	NEXT	RX3A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX3A_L2_TX4A.s4p
38	NEXT	RX3A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX3A_L2_TX5A.s4p
39	NEXT	RX3A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX3A_L2_TX6A.s4p
40	NEXT	RX3A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX3A_L2_TX7A.s4p
41	NEXT	RX3A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX3A_L2_TX8A.s4p
42	FEXT	RX3A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX3A_L2_TX1B.s4p
43	FEXT	RX3A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX3A_L2_TX2B.s4p
44	FEXT	RX3A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX3A_L2_TX4B.s4p
45	FEXT	RX3A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX3A_L2_TX5B.s4p
46	FEXT	RX3A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX3A_L2_TX6B.s4p
47	FEXT	RX3A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX3A_L2_TX7B.s4p

48	FEXT	RX3A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX3A_L2_TX8B.s4p
49	THRU	RX4A	L1	1, 3	TX4B	L2	2, 4	THRU_L1_RX4A_L2_TX4B.s4p
50	NEXT	RX4A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX4A_L2_TX1A.s4p
51	NEXT	RX4A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX4A_L2_TX2A.s4p
52	NEXT	RX4A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX4A_L2_TX3A.s4p
53	NEXT	RX4A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX4A_L2_TX4A.s4p
54	NEXT	RX4A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX4A_L2_TX5A.s4p
55	NEXT	RX4A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX4A_L2_TX6A.s4p
56	NEXT	RX4A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX4A_L2_TX7A.s4p
57	NEXT	RX4A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX4A_L2_TX8A.s4p
58	FEXT	RX4A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX4A_L2_TX1B.s4p
59	FEXT	RX4A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX4A_L2_TX2B.s4p
60	FEXT	RX4A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX4A_L2_TX3B.s4p
61	FEXT	RX4A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX4A_L2_TX5B.s4p
62	FEXT	RX4A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX4A_L2_TX6B.s4p
63	FEXT	RX4A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX4A_L2_TX7B.s4p
64	FEXT	RX4A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX4A_L2_TX8B.s4p
65	THRU	RX5A	L1	1, 3	TX5B	L2	2, 4	THRU_L1_RX5A_L2_TX5B.s4p
66	NEXT	RX5A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX5A_L2_TX1A.s4p
67	NEXT	RX5A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX5A_L2_TX2A.s4p
68	NEXT	RX5A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX5A_L2_TX3A.s4p
69	NEXT	RX5A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX5A_L2_TX4A.s4p
70	NEXT	RX5A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX5A_L2_TX5A.s4p
71	NEXT	RX5A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX5A_L2_TX6A.s4p
72	NEXT	RX5A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX5A_L2_TX7A.s4p
73	NEXT	RX5A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX5A_L2_TX8A.s4p
74	FEXT	RX5A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX5A_L2_TX1B.s4p
75	FEXT	RX5A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX5A_L2_TX2B.s4p
76	FEXT	RX5A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX5A_L2_TX3B.s4p
77	FEXT	RX5A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX5A_L2_TX4B.s4p

78	FEXT	RX5A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX5A_L2_TX6B.s4p
79	FEXT	RX5A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX5A_L2_TX7B.s4p
80	FEXT	RX5A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX5A_L2_TX8B.s4p
81	THRU	RX6A	L1	1, 3	TX6B	L2	2, 4	THRU_L1_RX6A_L2_TX6B.s4p
82	NEXT	RX6A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX6A_L2_TX1A.s4p
83	NEXT	RX6A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX6A_L2_TX2A.s4p
84	NEXT	RX6A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX6A_L2_TX3A.s4p
85	NEXT	RX6A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX6A_L2_TX4A.s4p
86	NEXT	RX6A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX6A_L2_TX5A.s4p
87	NEXT	RX6A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX6A_L2_TX6A.s4p
88	NEXT	RX6A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX6A_L2_TX7A.s4p
89	NEXT	RX6A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX6A_L2_TX8A.s4p
90	FEXT	RX6A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX6A_L2_TX1B.s4p
91	FEXT	RX6A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX6A_L2_TX2B.s4p
92	FEXT	RX6A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX6A_L2_TX3B.s4p
93	FEXT	RX6A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX6A_L2_TX4B.s4p
94	FEXT	RX6A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX6A_L2_TX5B.s4p
95	FEXT	RX6A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX6A_L2_TX7B.s4p
96	FEXT	RX6A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX6A_L2_TX8B.s4p
97	THRU	RX7A	L1	1, 3	TX7B	L2	2, 4	THRU_L1_RX7A_L2_TX7B.s4p
98	NEXT	RX7A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX7A_L2_TX1A.s4p
99	NEXT	RX7A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX7A_L2_TX2A.s4p
100	NEXT	RX7A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX7A_L2_TX3A.s4p
101	NEXT	RX7A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX7A_L2_TX4A.s4p
102	NEXT	RX7A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX7A_L2_TX5A.s4p
103	NEXT	RX7A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX7A_L2_TX6A.s4p
104	NEXT	RX7A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX7A_L2_TX7A.s4p
105	NEXT	RX7A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX7A_L2_TX8A.s4p
106	FEXT	RX7A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX7A_L2_TX1B.s4p
107	FEXT	RX7A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX7A_L2_TX2B.s4p

108	FEXT	RX7A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX7A_L2_TX3B.s4p
109	FEXT	RX7A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX7A_L2_TX4B.s4p
110	FEXT	RX7A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX7A_L2_TX5B.s4p
111	FEXT	RX7A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX7A_L2_TX6B.s4p
112	FEXT	RX7A	L1	1, 3	TX8B	L2	2, 4	FEXT_L1_RX7A_L2_TX8B.s4p
113	THRU	RX8A	L1	1, 3	TX8B	L2	2, 4	THRU_L1_RX8A_L2_TX8B.s4p
114	NEXT	RX8A	L1	1, 3	TX1A	L2	2, 4	NEXT_L1_RX8A_L2_TX1A.s4p
115	NEXT	RX8A	L1	1, 3	TX2A	L2	2, 4	NEXT_L1_RX8A_L2_TX2A.s4p
116	NEXT	RX8A	L1	1, 3	TX3A	L2	2, 4	NEXT_L1_RX8A_L2_TX3A.s4p
117	NEXT	RX8A	L1	1, 3	TX4A	L2	2, 4	NEXT_L1_RX8A_L2_TX4A.s4p
118	NEXT	RX8A	L1	1, 3	TX5A	L2	2, 4	NEXT_L1_RX8A_L2_TX5A.s4p
119	NEXT	RX8A	L1	1, 3	TX6A	L2	2, 4	NEXT_L1_RX8A_L2_TX6A.s4p
120	NEXT	RX8A	L1	1, 3	TX7A	L2	2, 4	NEXT_L1_RX8A_L2_TX7A.s4p
121	NEXT	RX8A	L1	1, 3	TX8A	L2	2, 4	NEXT_L1_RX8A_L2_TX8A.s4p
122	FEXT	RX8A	L1	1, 3	TX1B	L2	2, 4	FEXT_L1_RX8A_L2_TX1B.s4p
123	FEXT	RX8A	L1	1, 3	TX2B	L2	2, 4	FEXT_L1_RX8A_L2_TX2B.s4p
124	FEXT	RX8A	L1	1, 3	TX3B	L2	2, 4	FEXT_L1_RX8A_L2_TX3B.s4p
125	FEXT	RX8A	L1	1, 3	TX4B	L2	2, 4	FEXT_L1_RX8A_L2_TX4B.s4p
126	FEXT	RX8A	L1	1, 3	TX5B	L2	2, 4	FEXT_L1_RX8A_L2_TX5B.s4p
127	FEXT	RX8A	L1	1, 3	TX6B	L2	2, 4	FEXT_L1_RX8A_L2_TX6B.s4p
128	FEXT	RX8A	L1	1, 3	TX7B	L2	2, 4	FEXT_L1_RX8A_L2_TX7B.s4p
129	THRU	RX1B	L1	1, 3	TX1A	L2	2, 4	THRU_L1_RX1B_L2_TX1A.s4p
130	NEXT	RX1B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX1B_L2_TX1B.s4p
131	NEXT	RX1B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX1B_L2_TX2B.s4p
132	NEXT	RX1B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX1B_L2_TX3B.s4p
133	NEXT	RX1B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX1B_L2_TX4B.s4p
134	NEXT	RX1B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX1B_L2_TX5B.s4p
135	NEXT	RX1B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX1B_L2_TX6B.s4p
136	NEXT	RX1B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX1B_L2_TX7B.s4p
137	NEXT	RX1B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX1B_L2_TX8B.s4p

138	FEXT	RX1B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX1B_L2_TX2A.s4p
139	FEXT	RX1B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX1B_L2_TX3A.s4p
140	FEXT	RX1B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX1B_L2_TX4A.s4p
141	FEXT	RX1B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX1B_L2_TX5A.s4p
142	FEXT	RX1B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX1B_L2_TX6A.s4p
143	FEXT	RX1B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX1B_L2_TX7A.s4p
144	FEXT	RX1B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX1B_L2_TX8A.s4p
145	THRU	RX2B	L1	1, 3	TX2A	L2	2, 4	THRU_L1_RX2B_L2_TX2A.s4p
146	NEXT	RX2B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX2B_L2_TX1B.s4p
147	NEXT	RX2B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX2B_L2_TX2B.s4p
148	NEXT	RX2B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX2B_L2_TX3B.s4p
149	NEXT	RX2B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX2B_L2_TX4B.s4p
150	NEXT	RX2B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX2B_L2_TX5B.s4p
151	NEXT	RX2B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX2B_L2_TX6B.s4p
152	NEXT	RX2B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX2B_L2_TX7B.s4p
153	NEXT	RX2B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX2B_L2_TX8B.s4p
154	FEXT	RX2B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX2B_L2_TX1A.s4p
155	FEXT	RX2B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX2B_L2_TX3A.s4p
156	FEXT	RX2B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX2B_L2_TX4A.s4p
157	FEXT	RX2B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX2B_L2_TX5A.s4p
158	FEXT	RX2B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX2B_L2_TX6A.s4p
159	FEXT	RX2B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX2B_L2_TX7A.s4p
160	FEXT	RX2B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX2B_L2_TX8A.s4p
161	THRU	RX3B	L1	1, 3	TX3A	L2	2, 4	THRU_L1_RX3B_L2_TX3A.s4p
162	NEXT	RX3B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX3B_L2_TX1B.s4p
163	NEXT	RX3B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX3B_L2_TX2B.s4p
164	NEXT	RX3B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX3B_L2_TX3B.s4p
165	NEXT	RX3B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX3B_L2_TX4B.s4p
166	NEXT	RX3B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX3B_L2_TX5B.s4p
167	NEXT	RX3B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX3B_L2_TX6B.s4p

168	NEXT	RX3B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX3B_L2_TX7B.s4p
169	NEXT	RX3B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX3B_L2_TX8B.s4p
170	FEXT	RX3B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX3B_L2_TX1A.s4p
171	FEXT	RX3B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX3B_L2_TX2A.s4p
172	FEXT	RX3B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX3B_L2_TX4A.s4p
173	FEXT	RX3B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX3B_L2_TX5A.s4p
174	FEXT	RX3B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX3B_L2_TX6A.s4p
175	FEXT	RX3B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX3B_L2_TX7A.s4p
176	FEXT	RX3B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX3B_L2_TX8A.s4p
177	THRU	RX4B	L1	1, 3	TX4A	L2	2, 4	THRU_L1_RX4B_L2_TX4A.s4p
178	NEXT	RX4B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX4B_L2_TX1B.s4p
179	NEXT	RX4B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX4B_L2_TX2B.s4p
180	NEXT	RX4B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX4B_L2_TX3B.s4p
181	NEXT	RX4B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX4B_L2_TX4B.s4p
182	NEXT	RX4B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX4B_L2_TX5B.s4p
183	NEXT	RX4B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX4B_L2_TX6B.s4p
184	NEXT	RX4B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX4B_L2_TX7B.s4p
185	NEXT	RX4B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX4B_L2_TX8B.s4p
186	FEXT	RX4B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX4B_L2_TX1A.s4p
187	FEXT	RX4B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX4B_L2_TX2A.s4p
188	FEXT	RX4B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX4B_L2_TX3A.s4p
189	FEXT	RX4B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX4B_L2_TX5A.s4p
190	FEXT	RX4B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX4B_L2_TX6A.s4p
191	FEXT	RX4B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX4B_L2_TX7A.s4p
192	FEXT	RX4B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX4B_L2_TX8A.s4p
193	THRU	RX5B	L1	1, 3	TX5A	L2	2, 4	THRU_L1_RX5B_L2_TX5A.s4p
194	NEXT	RX5B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX5B_L2_TX1B.s4p
195	NEXT	RX5B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX5B_L2_TX2B.s4p
196	NEXT	RX5B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX5B_L2_TX3B.s4p
197	NEXT	RX5B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX5B_L2_TX4B.s4p

198	NEXT	RX5B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX5B_L2_TX5B.s4p
199	NEXT	RX5B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX5B_L2_TX6B.s4p
200	NEXT	RX5B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX5B_L2_TX7B.s4p
201	NEXT	RX5B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX5B_L2_TX8B.s4p
202	FEXT	RX5B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX5B_L2_TX1A.s4p
203	FEXT	RX5B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX5B_L2_TX2A.s4p
204	FEXT	RX5B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX5B_L2_TX3A.s4p
205	FEXT	RX5B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX5B_L2_TX5A.s4p
206	FEXT	RX5B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX5B_L2_TX6A.s4p
207	FEXT	RX5B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX5B_L2_TX7A.s4p
208	FEXT	RX5B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX5B_L2_TX8A.s4p
209	THRU	RX6B	L1	1, 3	TX6A	L2	2, 4	THRU_L1_RX6B_L2_TX6A.s4p
210	NEXT	RX6B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX6B_L2_TX1B.s4p
211	NEXT	RX6B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX6B_L2_TX2B.s4p
212	NEXT	RX6B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX6B_L2_TX3B.s4p
213	NEXT	RX6B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX6B_L2_TX4B.s4p
214	NEXT	RX6B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX6B_L2_TX5B.s4p
215	NEXT	RX6B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX6B_L2_TX6B.s4p
216	NEXT	RX6B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX6B_L2_TX7B.s4p
217	NEXT	RX6B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX6B_L2_TX8B.s4p
218	FEXT	RX6B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX6B_L2_TX1A.s4p
219	FEXT	RX6B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX6B_L2_TX2A.s4p
220	FEXT	RX6B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX6B_L2_TX3A.s4p
221	FEXT	RX6B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX6B_L2_TX4A.s4p
222	FEXT	RX6B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX6B_L2_TX5A.s4p
223	FEXT	RX6B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX6B_L2_TX7A.s4p
224	FEXT	RX6B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX6B_L2_TX8A.s4p
225	THRU	RX7B	L1	1, 3	TX7A	L2	2, 4	THRU_L1_RX7B_L2_TX7A.s4p
226	NEXT	RX7B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX7B_L2_TX1B.s4p
227	NEXT	RX7B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX7B_L2_TX2B.s4p

228	NEXT	RX7B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX7B_L2_TX3B.s4p
229	NEXT	RX7B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX7B_L2_TX4B.s4p
230	NEXT	RX7B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX7B_L2_TX5B.s4p
231	NEXT	RX7B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX7B_L2_TX6B.s4p
232	NEXT	RX7B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX7B_L2_TX7B.s4p
233	NEXT	RX7B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX7B_L2_TX8B.s4p
234	FEXT	RX7B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX7B_L2_TX1A.s4p
235	FEXT	RX7B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX7B_L2_TX2A.s4p
236	FEXT	RX7B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX7B_L2_TX3A.s4p
237	FEXT	RX7B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX7B_L2_TX4A.s4p
238	FEXT	RX7B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX7B_L2_TX5A.s4p
239	FEXT	RX7B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX7B_L2_TX6A.s4p
240	FEXT	RX7B	L1	1, 3	TX8A	L2	2, 4	FEXT_L1_RX7B_L2_TX8A.s4p
241	THRU	RX8B	L1	1, 3	TX8A	L2	2, 4	THRU_L1_RX8B_L2_TX8A.s4p
242	NEXT	RX8B	L1	1, 3	TX1B	L2	2, 4	NEXT_L1_RX8B_L2_TX1B.s4p
243	NEXT	RX8B	L1	1, 3	TX2B	L2	2, 4	NEXT_L1_RX8B_L2_TX2B.s4p
244	NEXT	RX8B	L1	1, 3	TX3B	L2	2, 4	NEXT_L1_RX8B_L2_TX3B.s4p
245	NEXT	RX8B	L1	1, 3	TX4B	L2	2, 4	NEXT_L1_RX8B_L2_TX4B.s4p
246	NEXT	RX8B	L1	1, 3	TX5B	L2	2, 4	NEXT_L1_RX8B_L2_TX5B.s4p
247	NEXT	RX8B	L1	1, 3	TX6B	L2	2, 4	NEXT_L1_RX8B_L2_TX6B.s4p
248	NEXT	RX8B	L1	1, 3	TX7B	L2	2, 4	NEXT_L1_RX8B_L2_TX7B.s4p
249	NEXT	RX8B	L1	1, 3	TX8B	L2	2, 4	NEXT_L1_RX8B_L2_TX8B.s4p
250	FEXT	RX8B	L1	1, 3	TX1A	L2	2, 4	FEXT_L1_RX8B_L2_TX1A.s4p
251	FEXT	RX8B	L1	1, 3	TX2A	L2	2, 4	FEXT_L1_RX8B_L2_TX2A.s4p
252	FEXT	RX8B	L1	1, 3	TX3A	L2	2, 4	FEXT_L1_RX8B_L2_TX3A.s4p
253	FEXT	RX8B	L1	1, 3	TX4A	L2	2, 4	FEXT_L1_RX8B_L2_TX4A.s4p
254	FEXT	RX8B	L1	1, 3	TX5A	L2	2, 4	FEXT_L1_RX8B_L2_TX5A.s4p
255	FEXT	RX8B	L1	1, 3	TX6A	L2	2, 4	FEXT_L1_RX8B_L2_TX6A.s4p
256	FEXT	RX8B	L1	1, 3	TX7A	L2	2, 4	FEXT_L1_RX8B_L2_TX7A.s4p

8 Literature

[1] IEEE Standard for Ethernet, IEEE 802.3-2018, Clause 92, Figure 92-17.

[2] IEEE Standard for Ethernet, IEEE 802.3-2018, Clause 92, Figure 92-18.

[3] IEEE Standard for Ethernet, IEEE 802.3-2018, Clause 92, Figure 92-2.

[4] IEEE Standard for Ethernet, IEEE 802.3-2018, Clause 92, Figure 93-2.

Rohde & Schwarz

The Rohde & Schwarz electronics group offers innovative solutions in the following business fields: test and measurement, broadcast and media, secure communications, cybersecurity, monitoring and network testing. Founded more than 80 years ago, the independent company which is headquartered in Munich, Germany, has an extensive sales and service network with locations in more than 70 countries.

www.rohde-schwarz.com

Certified Quality Management
ISO 9001

Rohde & Schwarz training

www.training.rohde-schwarz.com

PAD-T-M: 3572.7186.00/01.00/EN

Rohde & Schwarz customer support

www.rohde-schwarz.com/support

GFM356 | Version 0e | 03.2021
Application Note | Method of implementation (MOI) for IEEE up to 100 Gbps interface channel test
Data without tolerance limits is not binding | Subject to change