Application Note

TIPS & TRICKS ON DOUBLE PULSE TESTING

From designing a test setup to performing accurate measurements

Products:

- R&S®RTO2000
- R&S®RTE1000
- R&S®RTA4000
- R&S®RTM3000
- R&S®HMF2550

Jens Schweickhardt, Kevin Hermanns (PE-Systems), Dr. Markus Herdin (R&S) | GFM347 | Version 1.00 | 03.2021

ROHDE&SCHWARZ
Make ideas real

Contents

Abbreviations

DPT	Double Pulse Test
DUT	Device Under Test
AWG	Arbitrary Waveform Generator
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance

List of Nomenclatures

C_{B}	Capacitance of the capacitor bank
C_{DD}	Parasitic capacitance of freewheeling diode
C_{DS}	Drain-source capacitance of DUT
C_{GD}	Gate-drain capacitance of DUT
C_{GS}	Gate-source capacitance of DUT
$\mathrm{E_C}$	Energy of capacitor bank
$\mathrm{E_L}$	Energy of load inductor
E_{on}	Turn-on energy loss
E_{off}	Turn-off energy loss
E_{rr}	Reverse recovery energy
i_{D}	Drain current
i_{load}	Load current
i_{rr}	Reverse recovery current
I_{Test}	Test current
ΔI	Current drop
$L_{\mathrm{Bus,}}$	Parasitic inductance of bus bar / PCB connecting the capacitors with the DUT
L_{D}	Parasitic drain inductance
L_{G}	Gate inductance
L_{load}	Inductance of the load inductor
L_{S}	Parasitic source inductance
L_{sense}	Parasitic inductance of the measurement device
R_{G}	Gate resistance
R_{S}	Parasitic series resistance of load inductance
$t_{\mathrm{d(on)}}$	Turn-on delay time
$t_{\mathrm{d(off)}}$	Turn-off delay time
t_{f}	Fall time
t_{r}	Rise time
t_{rr}	Total reverse recovery time
V_{DC}	DC-link voltage (Test voltage)
V_{f}	Diode forward-voltage
v_{DS}	Drain-source voltage
ΔV_{DC}	DC-link voltage drop
τ_1	Duration of first pulse

τ_{break}	Duration of pulse break
τ_2	Duration of second pulse

1 Overview

In modern societies, a substantial amount of electrical energy is required for the operation of electronic circuits or controlled electrical drives. The requirement of electrical energy for these applications is fulfilled by power electronic converters. Power semiconductors (IGBT or MOSFET) are controlled devices, which are used to realize these converters. Even though the semiconductor industry has made a significant progress in the development of powerful and efficient components, power losses still occur in these components and cause them to heat up.

The junction temperature of a semiconductor has to be kept below a maximum permissible limit. Furthermore, heating up and cooling down have a strong influence on the lifetime of a semiconductor device. This so-called “thermal cycling” is another important aspect for the design of a cooling system. In order to design an effective cooling system, it is necessary to know the power losses occurring during the operation of a circuit as precisely as possible. These losses are composed of conduction and switching losses. While the conduction losses can be measured relatively easily, this is not so easy for switching losses.

Figure 1 depicts one phase of a typical two-level converter. During a fundamental cycle, the operation of the converter changes between buck and boost mode, depending on the direction of current flow. The switching operation of the converter creates commutation events from switch to diode or vice versa in each mode. If the converter operates in buck mode, S1 and D1 are active. In boost mode, the current commutates between S2 and D2. Consequently, a setup is required which allows the measurement of switching losses and switching times for all aforementioned commutations. Here the double pulse test comes into play.

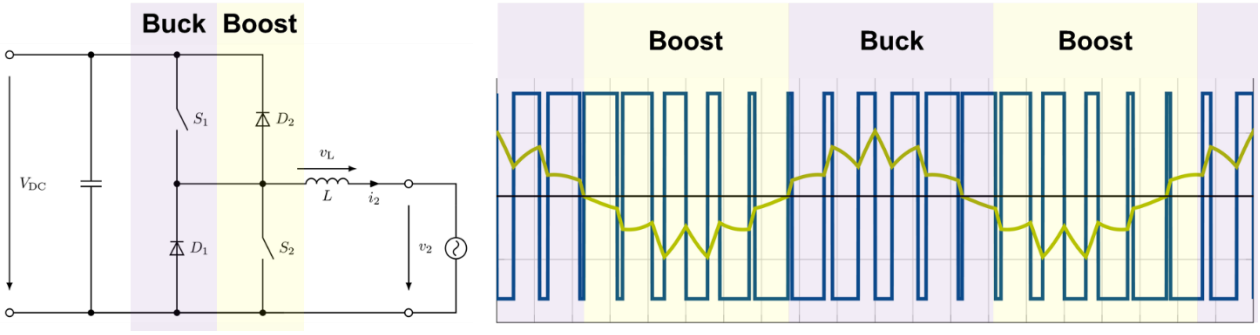


Figure 1: Two level converter and its operation modes.

This application note describes the basic concept of double pulse testing, the necessary measurement setup and gives an overview of the parameters influencing the measurement. Furthermore, practical tips for carrying out the measurement are presented. At this point, the reader is referred to the software application included in the application note, which allows to easily perform double pulse tests with Rohde & Schwarz instruments.

2 Double Pulse Test

The knowledge of the switching behavior of power semiconductor devices is crucial when it comes to the design of power converters. Double pulse tests are carried out to determine the switching times and switching losses as well as to ensure a proper switching behavior. For testing all converter states, the basic circuitry of the two-level converter is kept (DC-Link, switches and load inductor) but the load voltage source v_2 in Figure 1 needs to be replaced by a short circuit. For testing the switching events in the buck mode of the converter, the short circuit connects the load inductor between the mid-point (load terminal) and the minus rail (depicted in Figure 2). For the boost mode, the load inductor is connected to the plus rail. Figure 3 shows the basic circuit diagram for double pulse testing. The blue arrows between active and freewheeling state mark the commutations happening between these two states by each switching event. In the following, turn-on refers to the turn-on event of the switch (S_1 or S_2) which results in a commutation of the current from the diode to the switch (freewheeling to active state). Accordingly, turn-off refers to the turn-off of the switch and results in a commutation of the current from the switch to the diode (active to freewheeling).

Depending on the design of the DUT, measurements are to be performed on the high-side or low side-side device. S_1 or D_2 are the high-side devices while D_1 or S_2 are low-side. In a half-bridge module, for example, the current paths in the upper and lower part of the module are not necessarily symmetrical. In this case, the switching behavior of the two semiconductors deviates from each other. Therefore, measurements must be performed for both devices. The different causes for the deviation will be described in section 2.3

In a Double Pulse Test (DPT), the DUT can either be the switch or the diode. Additionally, the switch can either be a MOSFET or an IGBT. In this document, the test is performed using a MOSFET, however, if an IGBT is used, the drain and source in a MOSFET can be treated analogously to emitter and collector of IGBT.

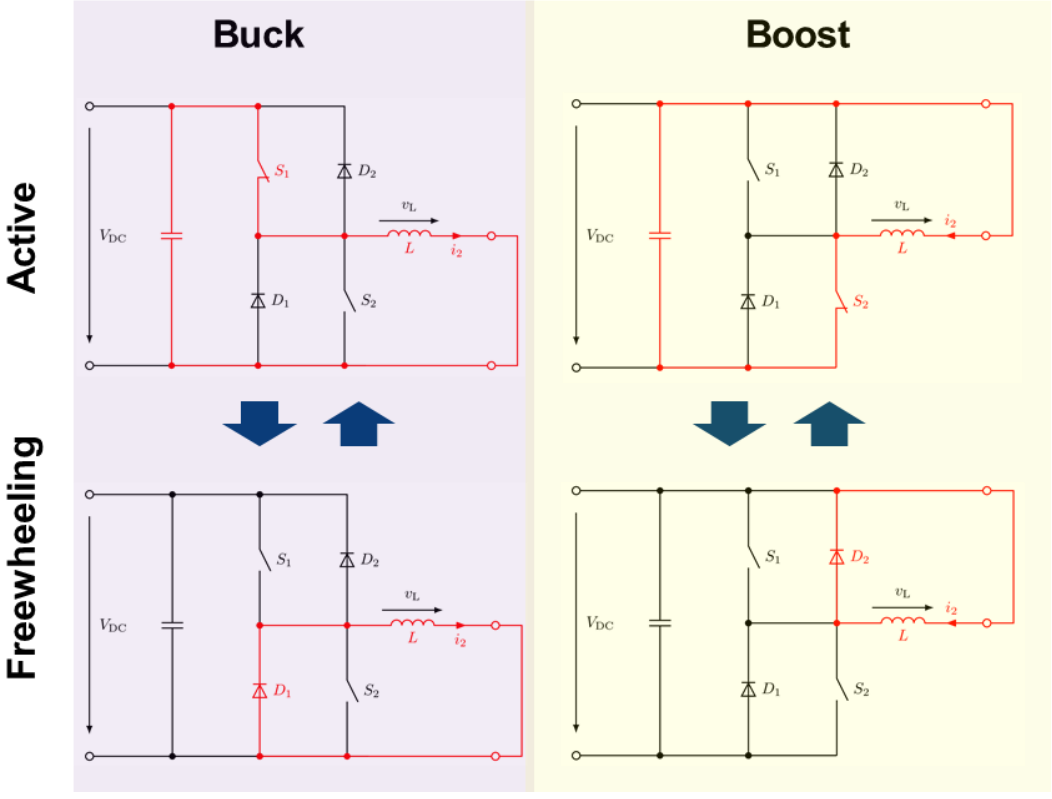


Figure 2: Overview of the double pulse test circuit-configuration for buck- and boost-mode test

A typical double pulse test setup consists of the following hardware components:

- Device under test (DUT)
- Freewheeling diode (D)
- DC supply
- DC link capacitor bank (C_{B})
- Load inductor (L_{load})
- Gate driver circuit
- Arbitrary Waveform Generator (AWG)
- Oscilloscope
- Measuring sensors for current
- Measuring probes for voltage
- Heating element

The basic setup including many of the components above can be found in Figure 3. It should be noted that the measuring circuit shown is at floating potential. This increases the flexibility of the measurement, but is not possible with all setups.

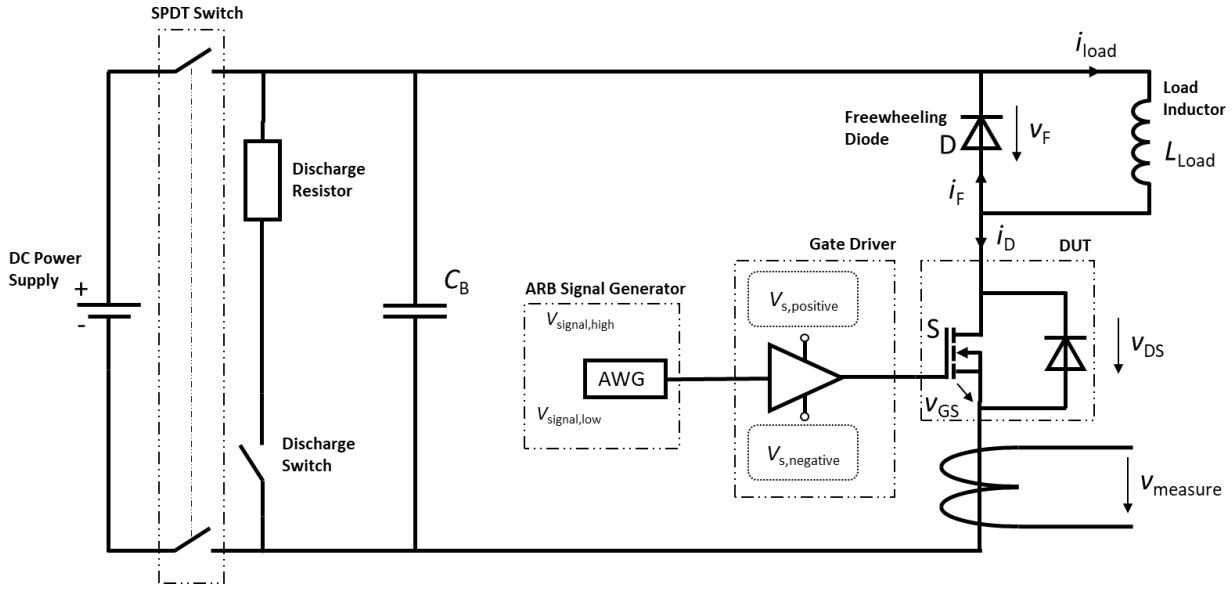


Figure 3: Circuit diagram of double pulse test

2.1 Test Procedure

In order to carry out the test, initially, the capacitor bank is charged to the desired test voltage via the power supply. The actual voltage has to be somewhat higher than the test voltage since the energy required to magnetize the inductive load must also be stored in the capacitor bank, resulting in some voltage drop during the first pulse. When the required voltage value is reached, the power supply is disconnected from the capacitor bank. The measurement circuit is now at a floating potential. The voltage reference is defined by the utilized measurement setup. This has the advantage that passive probes can be used for high-side measurements.

For the double pulse test, the necessary pulse sequence is calculated beforehand and is stored in the signal generator. The test consists of three phases, which can be seen in Figure 4. The phases are as following:

- first pulse with the duration τ_1,
- the pulse break with a duration τ_{break}
- the second pulse with duration τ_2

The corresponding voltage and current characteristics are depicted in Figure 4 as well. For each phase of the test, the current carrying components are marked inside the circuit diagram.

The first pulse turns on the DUT and thus, a closed loop circuit consisting of the capacitor bank, load inductance and parasitic series resistance (R_s) is formed (situation during τ_1). The pulse length is chosen such that the desired load current (test current) is reached. We note that it can be beneficial to use more than one pulse to reach the required test current [1]. The duration of the first pulse is defined according to the equation for the inductance,

$$v_{\text{load}} = L_{\text{load}} \cdot \frac{\mathrm{d}i_{\text{load}}}{\mathrm{d}t} \tag{1}$$

with the initial condition $v_{\text{load}} = V_{\text{DC}}$. After integrating equation 1, substituting $i_{\text{load}}$with the is the desired test current I_{Test} ($i_{\text{load}} = I_{\text{Test}}$) leads to the pulse duration (τ_1) for the first pulse (the parasitic series resistance R_{S} is neglected):

$$\tau_1 = L_{\text{load}} \cdot \frac{I_{\text{Test}}}{V_{\text{DC}}} . \tag{2}$$

During the pulse break τ_{Break}, the DUT is turned off and the current flows through the freewheeling diode. Due to the parasitic series resistances R_{S}, the inductor current drops slightly. By applying Kirchhoff's voltage law to the closed loop circuit, we get:

$$v_{\text{f}} = -(R_{\text{S}} \cdot i_{\text{load}} + L_{\text{load}} \cdot \frac{\mathrm{d}i_{\text{load}}}{\mathrm{d}t}) \tag{3}$$

where v_{f} is the forward voltage of the diode, which can be obtained from the data sheet. The duration of the first pulse is significantly longer than the duration of the break, in which the switch is off, and then the duration of the second pulse, in which the current through the inductance rises again. The length of the pulse break must be chosen such that the switching process starting the pulse break has decayed before the second pulse.

With the second pulse (τ_2), the DUT is turned on again, and energy is transferred from the capacitor bank to the load inductor. As a result, the voltage drops and the current continues to rise. The duration of the second pulse should be chosen so that the current through the DUT does not reach an impermissibly high value. The peak overshoot in the current observed in Figure 4 (top) is caused by the reverse recovery of freewheeling diode. Here, the stored charges of the diode add an additional current component which has to be taken by the switch. We note that both, turn-on and turn-off waveforms of the device under test, can be measured over the complete test period.

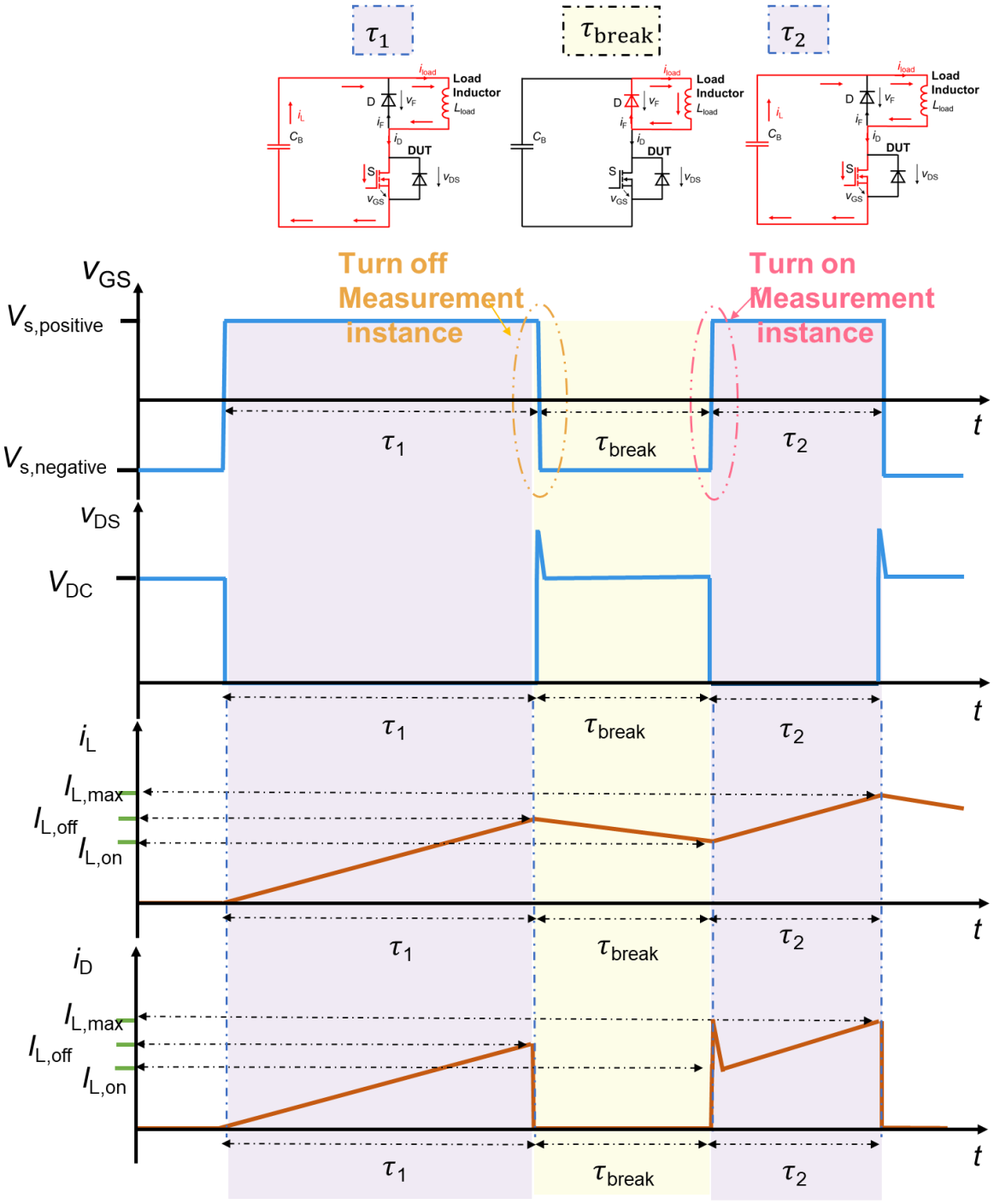


Figure 4: Voltages and currents in the three different phases of the double pulse test

2.2 Measurement Parameters

Figure 5 represent the standards to measure turn-on and turn-off times and switching energies for a MOSFET. Further information can be found in IEC 60747-8. If the switching behavior of an IGBT needs to be characterized, refer to IEC 60747-9.

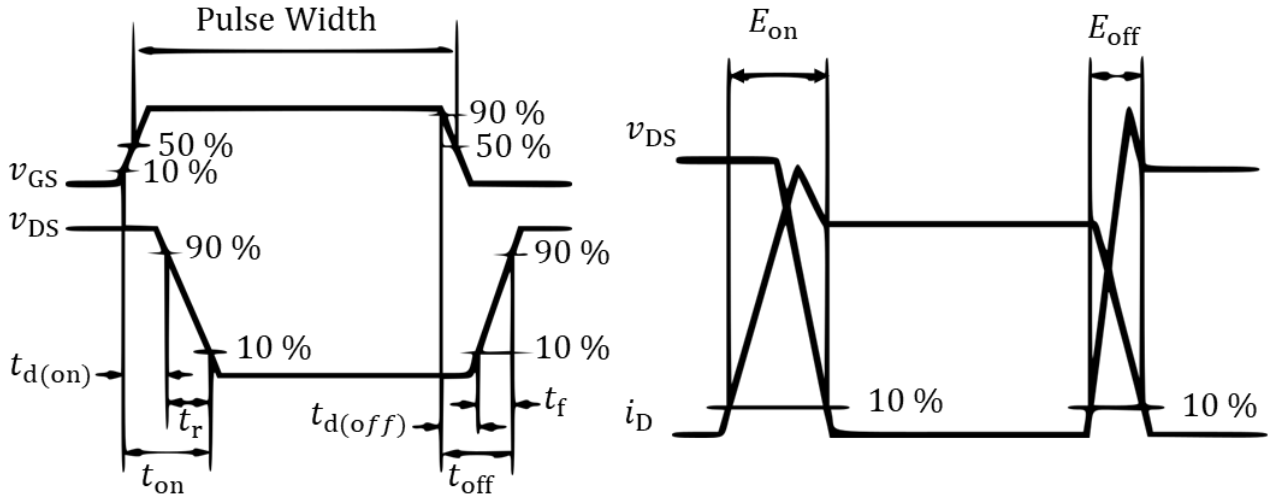


Figure 5: Turn-on and turn-off characteristics and switching energies of MOSFETs according to IEC 60747-8

2.2.1 Switching Times (t_d, t_r, t_f)

They are defined as follows,

$t_{d(on)}$: Turn-on delay time is the time interval between 10% of the rising v_{GS} and 90% of the dropping v_{DS}

t_r : Rise time (due to the rising current) is the time interval between 10% and 90% of the v_{DS}.

$t_{d(off)}$: Turn-off delay time is the time interval between 90% of the dropping v_{GS} and 90% of the rising v_{DS}

t_f: Fall time (due to the falling current) is the time interval between 10% and 90% of v_{DS}.

2.2.2 Switching Energy (E_{on}, E_{off})

The switching energy is the integral of the power dissipated during turn-on and turn-off of a semiconductor.

E_{on}: The energy loss for turn-on is assessed in the time interval between 10% of I_{test} and 10% of V_{DC} and can be evaluated by:

$$E_{on} = \int_{t_{I_{test10}}}^{t_{V_{DC10}}} v_{DS}(t) \cdot i_D(t)\ dt \qquad (4)$$

E_{off}: The energy loss for turn-off is assessed in the time interval between 10% of V_{DC} and 10% of I_{test} and can be evaluated by:

$$E_{off} = \int_{t_{V_{DC10}}}^{t_{I_{test10}}} v_{DS}(t) \cdot i_D(t)\ dt \qquad (5)$$

2.2.3 Reverse Recovery Characteristics of Freewheeling Diode (t_{rr}, E_{rr})

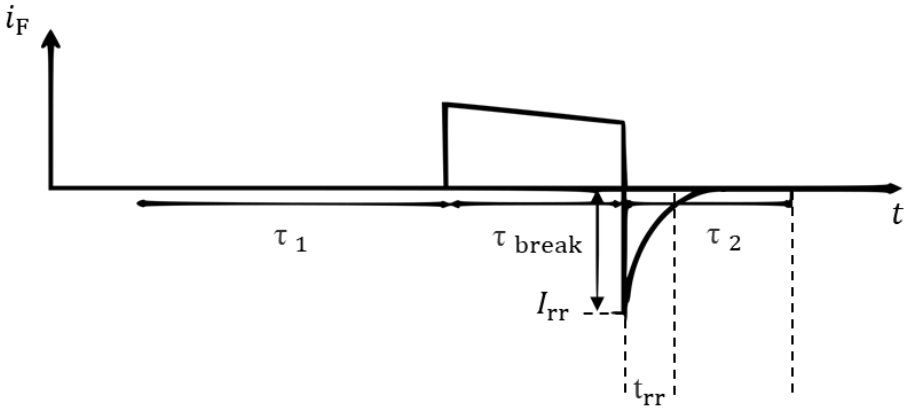


Figure 6: Current of freewheeling diode during double pulse test including reverse recovery

The freewheeling diode operates in forward conduction mode during τ_{break}, however, at τ_2, when the switch is turned on again, the freewheeling diode enters into a reverse blocking mode [2]. To be able to withstand the DC-link voltage, the charges stored in the diode have to be removed. During this removal, the current through the diode i_f gets negative for a short period of time – the reverse recovery time t_{rr}. Figure 6 gives an overview of the diode current during the double pulse test. The current I_{rr} is the peak current during the reverse recovery time interval.

$\boldsymbol{t_{rr}}$: The reverse recovery time is the time interval between the zero crossing of the diode current i_f and the point in time the current has decayed to 25 % of I_{rr}.

$\boldsymbol{E_{rr}}$: The energy loss for reverse recovery is assessed in the time interval between 10% of V_{DC} and 2% of I_{rr} and can be evaluated by:

$$E_{rr} = \int_{t_{V_{DC10}}}^{t_{I_{rr2}}} v_f(t) \cdot i_f(t)\ dt \qquad (6)$$

where v_f is the forward voltage and i_f is the diode current.

2.3 Effect of Parasitic Components

For power semiconductors, the parasitic components of the connected circuitry have an important impact on the switching behavior of the DUT. Figure 7 shows the equivalent circuit of the double pulse test with the parasitic components impacting the device's switching behavior. The parasitic components present in the power loop include the equivalent series inductance (ESL) of the capacitor bank, the parasitic inductance of the bus/PCB L_{Bus} , the parasitic inductances of the drain and the source terminals of the device L_D and L_S, the parasitic capacitance of free-wheeling diode C_{DD}, the equivalent parallel capacitance of the load inductor (EPC) and the parasitic inductance of the measurement device L_{sense}. For the sake of simplicity, the parasitic inductances L_{ESL} , L_{Bus}, L_D, L_S, and L_{sense} are summarized by L_σ in the following. The gate loop includes the parasitic inductance of the gate L_G and the parasitic inductance of the source terminal L_S. The capacitances C_{GD}, C_{GS} and C_{DS} are the devices internal inter-terminal capacitances governing the devices switching behavior.

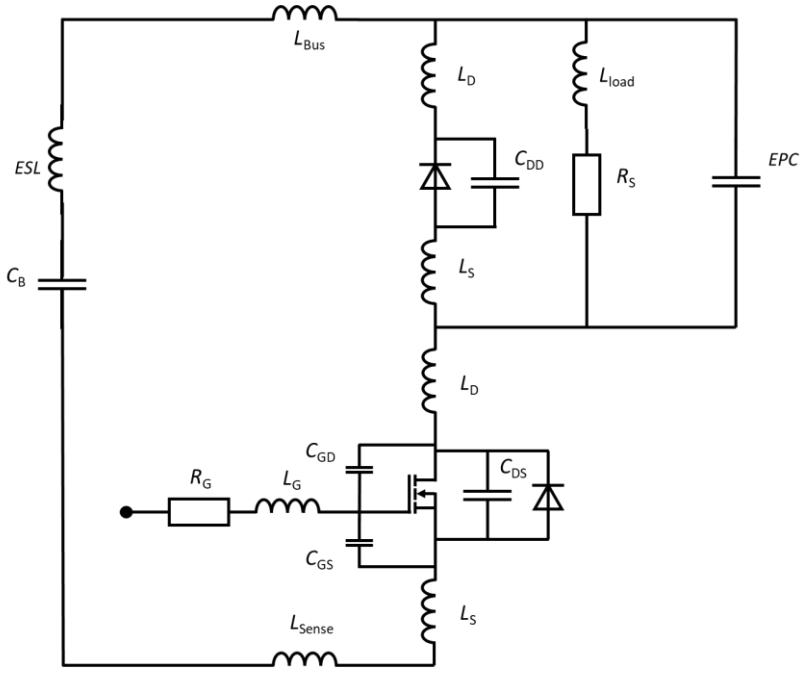


Figure 7: Equivalent circuit diagram of double pulse test setup with parasitics

To understand the impact of parasitics on semiconductors' switching behavior, a detailed view on the waveforms is necessary. Figure 8 shows the drain current i_D, the drain-source voltage v_{DS} and the gate-source voltage v_{GS} of a turn-on and turn-off event of a MOSFET. The switching can be sub-divided into ten phases starting with the events t_0 to t_9. Before t_0, the MOSFET is turned off.

Turn-on

$\boldsymbol{t_0}$: Driver turns on and charges the gate-source capacitance C_{GS} through the gate resistor R_G. The gate-source voltage v_{GS} increases.

$\boldsymbol{t_1}$: The gate-source voltage reaches the threshold voltage of the device which starts to conduct. Afterwards, the drain current i_D and the gate-source voltage are further increasing. At this phase, the first parasitic effect with a strong impact on the switching losses comes into play. The rising current in the power loop causes a voltage drop across the parasitic inductances (see Figure 9). This voltage drop decreases the voltage v_{DS} as given in

$$v_{DS} = V_{DC} - L_\sigma \cdot \frac{di_D}{dt} \qquad (7)$$

$\boldsymbol{t_2}$: The drain current reaches the load current for the first time. At this time instance, the load current is fully commutated to the MOSFET. Since then, the stored charges of the freewheeling diode are extracted. It is referred to as reverse recovery until the drain current reaches the load current again. In an ideal switching event, t_2 is the time instance when the drain-source voltage of the MOSFETs starts to decrease (depicted in Figure 10). The drain current keeps rising. The same applies for the gate-source voltage.

$\boldsymbol{t_3}$: The drain current reaches its maximum and starts to decrease to the test current. The gate-source voltage no longer increases and the drain-source voltage starts to collapse. While the drain-source voltage collapses, the voltage across the capacitance C_{GD}, which corresponds to the feedback capacitance C_{rss} given in the datasheet, changes accordingly. The capacitance C_{GD} is voltage dependent with an increasing value for lower voltages. This keeps gate-source voltage constant at the so called Miller plateau. Due to this effect the feedback capacitance is called the Miller capacitance.

t_4: The drain current reaches the test current in an ideal case. However, depending on circuit resonances (even from the used measurement equipment), oscillations may be observed. For finding the root cause, a detailed analysis is required. The drain-source voltage further decreases but the rate of voltage change is slowed down. This limits the change of the feedback capacitance and therefore the gate-source voltage starts rising.

t_5: The gate-source voltage reaches its on-value and the drain-source voltage is in on-state.

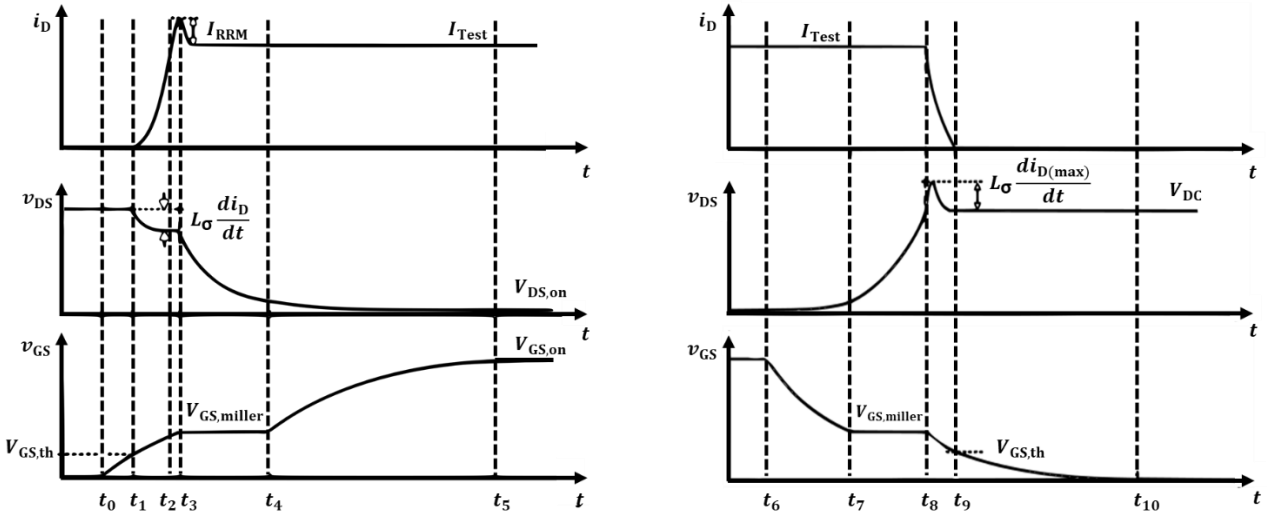


Figure 8: Turn-on (left) and turn-off (right) waveforms of a MOSFET

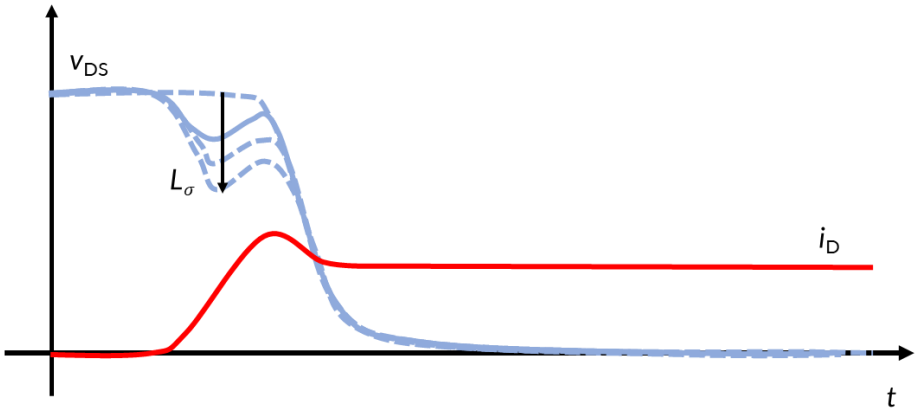


Figure 9: Impact of an increasing stray inductance during turn-on

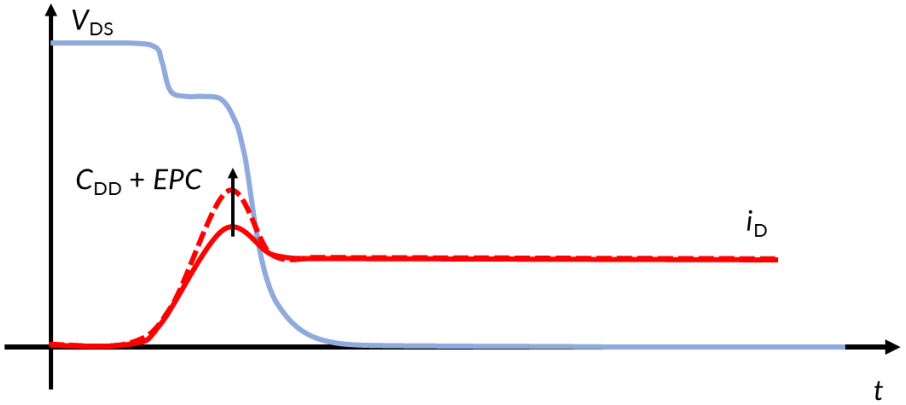


Figure 10: Impact of the parasitic capacitances of diode and load inductor on turn-on of a MOSFET

Turn-off

t_6: At this time instance, the driver circuit starts to discharge the input capacitance C_{iss}, which is the parallel connection of the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD}. The gate-source voltage starts decreasing according to the time constant given by $R_{\mathrm{g}} \cdot C_{\mathrm{iss}}$. The drain-source voltage starts rising slightly. The drain current remains unchanged.

t_7: The gate source voltage reaches the Miller plateau. The increase in drain-source voltage accelerates but the drain current is still constant.

t_8: Now the drain-source voltage reaches V_{DC}. The drain current starts to decrease. The same effect which generated the voltage dip in v_{DS} during the turn-on event is now generating a voltage overshoot. The decreasing current leads to an additional voltage component across the stray inductance summing up with the DC-link voltage and stressing the DUT. The impact of an increased stray inductance is shown in Figure 11. The gate-source voltage reaches the end of the Miller plateau and further decreases.

t_9: The drain current and the drain-source voltage reach the off-state. The gate-source voltage further decreases.

t_{10}: The gate-source voltage reaches the off-state.

The parasitic components cause voltage spikes and ringing, electromagnetic interference and reliability problems. The parasitic components L_{D} and L_{S} are inherent properties of the DUT and have a significant impact on the switching performance. The common source inductance L_{S} provides a negative feedback path between the power loop and gate loop during the switching transient $\frac{di}{dt}$ and increases the switching losses.

Because of the initial stored charges, the parasitic inductance L_σ acts as a current source during the turn-on, pushing the device to turn-on quickly. However, on the other hand, it is not beneficial for the turn-off period because it delays the device's turn-off [3]. This behavior especially becomes important if the device is facing a short circuit and has to be turned off quickly.

The parasitic components depicted in Figure 7 only covers the most important parasitic components. In practice, there are several other parasitic components arising from the setup and different measuring equipment in uses.

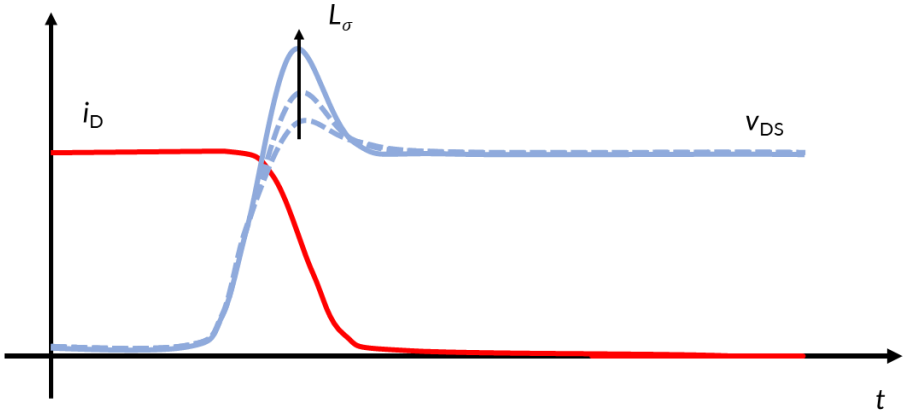


Figure 11: Impact of increasing stray inductance on the turn-off event

2.4 Design of Circuit Parameters

In the design of the circuit parameters, load inductor and the capacitor bank are given highest priority. For manufacturers, the performance of a component to be achieved is the main focus when preparing data sheets. Thus, optimized test setups are used as far as possible. However, the performance hardly corresponds to the values to be expected in practice for a converter to be produced in series.

Unfortunately, data sheets for power semiconductors still lack values, which makes it very difficult for a user to relate values from different manufacturers for comparisons on common grounds. Furthermore, series applications are systematically optimized for cost, mass, volume, etc., which leads to completely different designs. Additionally, the measuring circuit surrounding the DUT has a massive influence on the expected switching losses and switching times, which is why manufacturers of power electronic systems often compare components in an application-oriented design during the design phase.

Before the double pulse test is carried out, the boundary conditions to be covered by the design need to be defined. Here, the following points are of importance:

- ► Maximum voltage to be turned off
- ► Maximum test current
- ► Maximum rate of current and voltage change
- ► Permissible self-heating of semiconductor device
- ► Test temperature
- ► Possibility to perform a short circuit test on the setup

Based on the specifications, the necessary load inductor and the capacitor bank must first be dimensioned.

2.4.1 Dimensioning the Load Inductor

The load inductor is responsible to maintain the current as constant as possible between two switching events of the double pulse test. The turn-off and turn-on event should be measured close to the desired test current. Referring to the standards IEC-60747-8 and -9, a constant current is required for the test, demanding for a large load inductance. This in turn requires long durations of the first pulse to achieve the desired test current. On the other hand, a large pulse duration leads to self-heating of the semiconductor device. Therefore, both aforementioned criterions should be considered while designing the load inductor.

- ► Duration of the first and second pulse

  The duration of the pulse and the value of test current I_{test} depends on the load inductor. Higher values of load inductance result in a slower increase of currents. The operation of the semiconductor devices is highly dependent on the test temperature. Therefore, the duration of the first pulse τ_1 should not exceed 100 µs to avoid self-heating of the semiconductor [4]. Consequently, the higher limit to design the load inductor is given as:

$$\tau_1 = L_{\mathrm{load}} \cdot \frac{I_{\mathrm{test}}}{V_{\mathrm{DC}}} \tag{8}$$

$$L_{\mathrm{load}} \leq \tau_1 \cdot \frac{V_{\mathrm{DC}}}{I_{\mathrm{test}}} \tag{9}$$

- ► Constant current during pulse break

As mentioned previously, a constant current is desired during the pause. However, there is a decrease in the current due to the losses occurring in the parasitic resistance of the load and the free-wheeling diode. During the pause, this drop-in current ΔI can be kept small by using higher values for the load inductance. But as mentioned in criterion 1, higher values of load inductor might lead to self-heating of the semiconductor device. To guarantee that a certain limit is not exceeded, a minimum value of the inductance can be calculated.

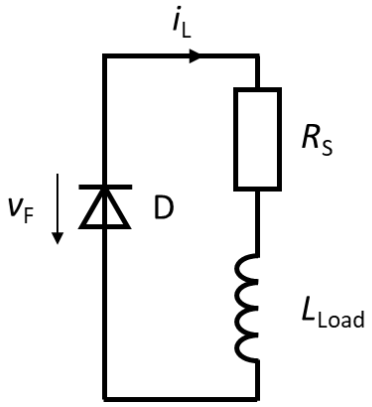


Figure 12: Direction of current during the pause

Figure 12 gives us the equivalent circuit valid for the pulse pause. To determine the current i_{load} during that period, the following equation is true:

$$i_{\mathrm{load}}(t) = I_{\mathrm{test}} \cdot e^{-\frac{R_S}{L_{\mathrm{load}}} \cdot t} + \frac{v_F}{R_S} \cdot \left(e^{-\frac{R_S}{L_{\mathrm{load}}} \cdot t} - 1\right) \tag{10}$$

The drop in current during the pause ΔI can be calculated by:

$$\Delta I = i_{\mathrm{load}}(\tau_{\mathrm{break}}) - I_{\mathrm{test}} = \left(I_{\mathrm{test}} + \frac{v_F}{R_S}\right) \cdot \left(e^{-\frac{R_S}{L_{\mathrm{load}}} \cdot \tau_{\mathrm{break}}} - 1\right) \tag{11}$$

Reshaping and taking the natural logarithm on both sides gives the required inductance whereas ΔI is specified by the designer. Typical values are 1 to 5 % of the rated load current:

$$L_{\mathrm{load}} \geq -\left[R_s \cdot \tau_{\mathrm{break}} \cdot \left(\frac{1}{\ln\left(\frac{\Delta I}{I_{\mathrm{test}} + \frac{v_F}{R_S}} + 1\right)}\right)\right] \tag{12}$$

Therefore, the minimum required inductance depends on the desired test current, parasitic resistance of the load, the pause duration and the forward voltage of the freewheeling diode. The forward voltage of the diode is mentioned in the data sheet and can be used for estimation.

The dimensioning of the inductance is based on the above-mentioned criteria and needs to be a tradeoff in order to have both, an optimum pulse duration τ_1 and a constant current during the pause. In double

pulse test, the impact of the parasitic parallel capacitance of the inductor increases with an increase of the rate of voltage change. Generally, there is a choice between an iron core and an air core inductor, which can either have a toroidal or a cylindrical shape. For the setup used in this application note, a cylindrical air core inductor was used. Advantage of using a cylindrical air core inductor is that the absence of capacitances to the core makes the parasitic capacitance smaller compared to an iron core inductor. The disadvantage in comparison to iron core inductor is that due to absence of the field reinforcing effect, a comparably larger size is required.

2.4.2 Dimensioning the Capacitor Bank

During the first pulse, the electrical energy is taken from the capacitor bank and then converted into magnetic energy in the load inductor. The voltage during this period should remain as constant as possible and the minimum required capacitance can be obtained by considering energy balance in between capacitor and the load inductor. The electrical energy stored in the capacitor bank is given by:

$$E_{\mathrm{C}} = \frac{1}{2} \cdot C_{\mathrm{B}} \cdot {V_{\mathrm{DC}}}^2 \tag{13}$$

whereas the magnetic energy in the load inductor is given by:

$$E_{\mathrm{L}} = \frac{1}{2} \cdot L_{\mathrm{load}} \cdot I_{\mathrm{test}}^2 \tag{14}$$

The energy drop of the capacitor ΔE_{C} is the difference in energy stored in the capacitor bank between the beginning and the end of the pulse. It represents the DC link voltage drop ΔV_{DC} and is given by:

$$\Delta E_{\mathrm{C}} = \frac{1}{2} \cdot C_{\mathrm{B}} \cdot {V_{\mathrm{DC}}}^2 - \frac{1}{2} \cdot C_{\mathrm{B}} \cdot (V_{\mathrm{DC}} - \Delta V_{\mathrm{DC}})^2 \tag{15}$$

The relation $E_{\mathrm{L}} = \Delta E_{\mathrm{C}}$ leads to:

$$\frac{1}{2} \cdot L_{\mathrm{load}} \cdot I_{\mathrm{test}}^2 = \frac{1}{2} \cdot C_{\mathrm{B}} \cdot {V_{\mathrm{DC}}}^2 - \frac{1}{2} \cdot C_{\mathrm{B}} \cdot (V_{\mathrm{DC}} - \Delta V_{\mathrm{DC}})^2 \tag{16}$$

Therefore, the capacitance C_{B} has to fulfil the following criterion to limit the voltage drop ΔV_{DC}:

$$C_{\mathrm{B}} \geq \frac{L_{\mathrm{load}} \cdot I_{\mathrm{test}}^2}{2 \cdot V_{\mathrm{DC}} \cdot \Delta V_{\mathrm{DC}} - \Delta V_{\mathrm{DC}}^2} \tag{17}$$

This DC-link capacitance requirement increases with the increase in the test current. For smaller intermediate circuit voltage, a significant large capacitance is required. For the double pulse test, a capacitance in a range of µF to a few mF is required. Most importantly, the DC link should be designed in such a way that it has a very low parasitic inductance. Generally, the choice is between the available types, electrolytic, film and ceramic capacitors. Its features and suitability are listed in Table 1.

Table 1: Different types of capacitors

Capacitor types	Features
Electrolytic capacitors	+High operating temperature range -High ESR and ESL
Film capacitors	+Low ESR and ESL +High ripple current density +Available in prismatic shapes - Low operating temperature range

Instead of using a single capacitor with a large value, multiple units with smaller capacitance should be used in parallel to achieve the total capacitance in order to have a low stray inductance design as shown in Figure 13.

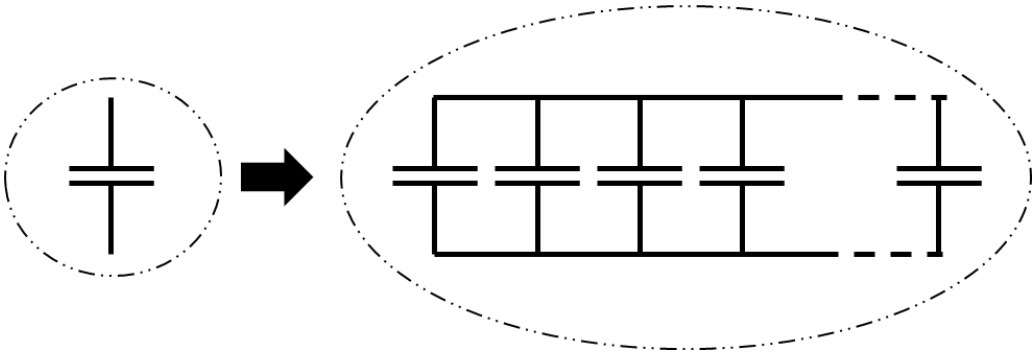


Figure 13: Low ESL design of capacitor bank

3 Voltage and Current Measurement

For the estimation of all the devices' switching characteristics, both voltages and currents have to be measured. The first challenge of the double pulse test setup is to obtain comparably large values with a large rate of change (v_{DS} and i_{D}). To tackle this, it is of importance that the applied probes have adequate bandwidth and a wide range of linearity to record the rising and falling edges of the switching waveforms [5]. The second challenge is that comparably small voltages have to be measured in the presence of large common mode voltages (v_{GS} vs. v_{DS}). Therefore, a large common mode rejection ratio over a wide bandwidth is required.

The test setup on a floating potential increases the flexibility of the measurements. Passive probes can be used to measure quantities even on the high-side. Care must be taken when inserting the probes, as the reference potential of the setup is defined by them.

Figure 14 depicts typical measurement setups (floating potential and grounded). The features of each of these measurement techniques are listed in Table 2.

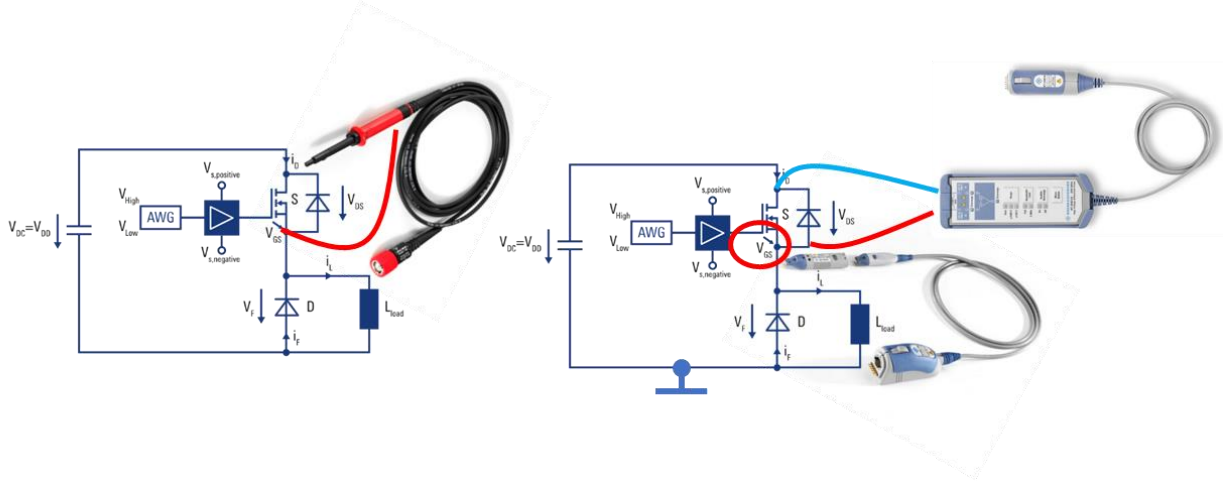


Figure 14: Different measurement setups. Left: floating setup and passive probe. Right: grounded setup with differential probes

Table 2: Features of different measurement setups

Setup	Features
Floating setup and passive probes	▶ No direct connection to the ground ▶ Bandwidth up to 500 MHz ▶ Simple and inexpensive probing solution
High-Voltage differential Probe	▶ Able to precisely measure small differential voltages in presence of large common mode voltages. ▶ Suitable for prototype setups where grounding of the DUT cannot be avoided ▶ Minimizes loading and measurement errors due to high input impedance ▶ Bandwidth limited to 200MHz.
Isolated channel oscilloscope	▶ No direct connection to the ground ▶ Excellent DC and lower frequency CMRR ▶ Bandwidth up to 500 MHz ▶ Isolated probes are not truely differential

The frequency range in which a measurement system provides reliable and accurate results is determined by its bandwidth. Thus, the rise and fall-time correspond to a spectrum which should be measured undamped. Therefore, bandwidth of the measurement system should be at least five times larger than the highest frequency component to be measured [5]. Referring to Figure 15, the switching edge with a rise time of 10 ns accurately corresponds to the edge of a sinusoidal signal of 35 MHz initially. However, when the required

DC-link voltage is reached, oscillations can follow which need to be measured as well. If the signal is measured using a probe and an oscilloscope, the rise time of the measured signal results in:

$$t_{\mathrm{r,meas}} \approx \sqrt{t^2{}_{\mathrm{r,sig}} + t^2{}_{\mathrm{r,probe}} + t^2{}_{\mathrm{r,osc}}} \tag{18}$$

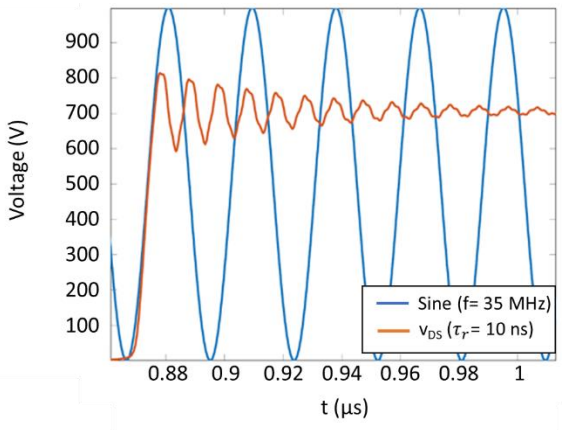


Figure 15: Sinusoidal signal with *f* = 35 MHz and drain to source voltage with t_r= 10 ns.

3.1.1 Voltage Measurement Probes

In order to measure the voltage for double pulse test, there are different types of voltage probes from Rohde & Schwarz available [6] [7]. Voltage probes should facilitate requirements such as high accuracy and high bandwidth. There are basically two categories of voltage probes, active differential probes and passive probes. Active differential voltage probes allow voltage measurement to be carried out independent of the oscilloscope's ground. Therefore, it can be flexibly used in the test setup as long as the maximum input voltage is not exceeded.

Passive probes on the other hand are robust and have no active components and do therefore not require a power supply. Figure 16 shows the passive voltage measurement probes R&S ® RT-ZI10 and R&S ® RT-ZH10. On the left, the probe with a longer ground lead is depicted which forms a comparably large inductance loop between the probe and the ground lead. Through this loop, parasitic coupling can occur. To minimize the coupling, the ground lead should be wrapped around the probe as can be seen in Figure 16 (center). Another counter measure to overcome unintended coupling to the probe is the usage of a ground spring, which can be attached to the sleeve of the probe. In that case, typically, a probe holder is required to position the probe.

As a general statement, it should be noted that long leads and pins increases the parasitic inductance which increases a parasitic coupling into the voltage signal. This causes ringing and overshoots in the pulse, which might not be part of the original signal. Therefore, it is of importance to apply counter measures. Different probes from Rohde & Schwarz along with their features are listed in Table 3.

Figure 16: DPT voltage measurement with passive probes with large loop(left) and counter measures (center) and (right)

For differential probes, the same unintended coupling can occur if long leads are attached to the amplifier. Figure 17 gives an overview for a Rohde & Schwarz differential probe used with large loop inductance on the left and the twisted leads as counter measure on the right.

Table 3: Different types of voltage probes [7]

Probe type	Model	Features
Active differential probe	R&S ® RT-ZHD07 R&S ® RT-ZHD15/-ZHD16 R&S ® RT-ZHD 60 R&S ® RT-ZD10 R&S ® RT-ZD20	▶ R&S ® RT-ZHDxx high-voltage differential probes with up to 200 MHz bandwidth, up to 6 kV input voltage range ▶ R&S ® RT-ZD10/20 broadband differential probes with up to 2 GHz bandwidth for up 50 V input voltage range (with external 10:1 attenuator), very low input capacity / high input impedance ▶ Low added noise
Passive probes	R&S ® RT-ZI10 R&S ® RT-ZI10C R&S ® RT-ZI11 R&S ® RT-ZH10 R&S ® RT-ZH11	▶ Bandwidth up to 500 MHz ▶ High linearity and low added noise ▶ Note: R&S ® RT-ZIxx probes are for usage with the isolated channel oscilloscope R&S ® Scope Rider (RTH), only

Figure 17: Ways to use differential probes. Using twisted leads provides usually the best measurement result as unintended noise coupling is minimized.

3.1.2 Current Measurement

Current sensors are used to measure the current of the DUT. There are various methods available to measure the current. The most suitable ones for DPTs are presented as follows

Coaxial Shunts: This method uses low ohmic resistances in the circuit where the current is to be measured and relies on the Ohm's law. For an ideal resistance, the current is proportional to the measured voltage. Therefore, measurement results can be obtained with the help of the voltage drop across these resistors. A limiting factor for measurement of current with coaxial shunt is the parasitic inductance L_{Shunt} of the measurement setup. This causes the current measurement to become frequency dependent and thus limits the bandwidth to:

$$f_{\mathrm{BW(Shunt)}} = \frac{R_{\mathrm{Shunt}}}{2 \cdot \pi \cdot L_{\mathrm{Shunt}}} \tag{19}$$

Current Transformer: This sensor consists of a transformer with a ferromagnetic toroidal core which has the secondary-side winding mounted on it. The wire, whose current is to be measured, leads through the core of the transformer and represents the primary winding. The magnetic field surrounding the conductor magnetizes the transformer core, thereby inducing a current in the secondary winding proportional to the conductor current. A burden resistor completes the circuit on the secondary side. The voltage drop across the burden is proportional to the primary side current and can be measured by an oscilloscope [8].

Rogowski Coil: A Rogowski coil has similar operation principle as a current transformer. However, the main difference is that it is wound on an air core (non-magnetic) instead of an iron core. A Rogowski coil encloses the current carrying conductor of which the current is to be measured. This method is based on the principle that the voltage induced in the Rogowski coil is proportional to the rate of change of current in the conductor. The voltage that is induced in the coil must be integrated in order to get the output voltage that is proportional to current in the conductor and in most cases magnified to meet oscilloscopes sensitivity requirements. This coil has a linear behavior as there is no saturation effect due to the absence of magnetic material.

Table 4 gives an overview about the different current measurement techniques with its features. Figure 18 shows the connection arrangement of different types of current measurement methods with the DUT.

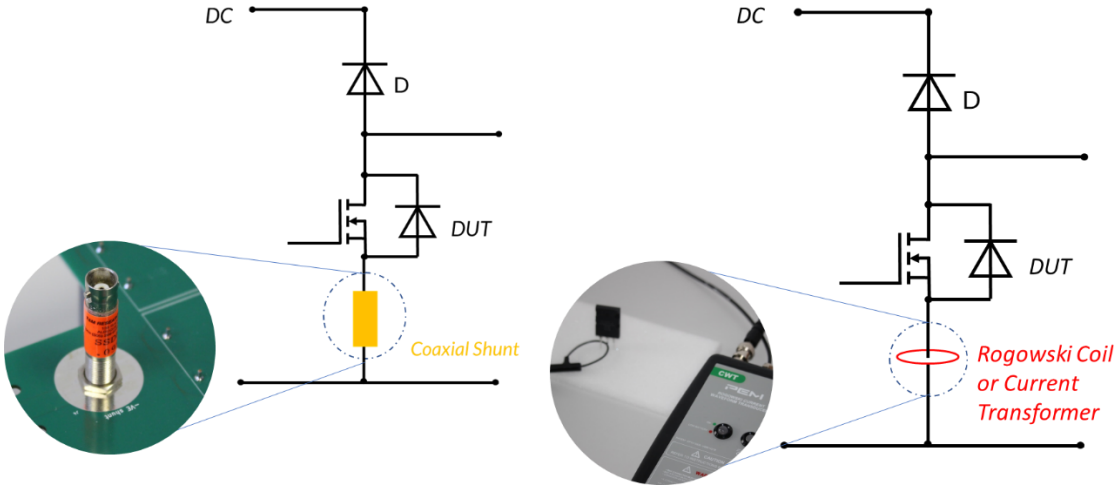


Figure 18: Arrangement of different current measurement techniques

Table 4: Different current measurement techniques for double-pulse testing applications

Current measurement	Maximum achievable bandwidth	Suitability	Features
Coaxial Shunt	2 GHz	AC/DC	+ High bandwidth and accuracy - no galvanic isolation, large in size, additional loop inductance
Current Transformer	200 MHz	AC	+ isolated measurement - large in size, saturation effect, additional loop inductance
Rogowski Coil	100 MHz	AC	+ Isolated measurements, no saturation effect - Additional integrator required, low bandwidth

3.2 De-skew

Using different types of measurement instruments leads to different signal propagation times, e.g. between voltage and current measurement. As can be seen in Figure 19 (left), a signal measured by two different probes shows different shapes and a different delay in time. This is caused by different probing properties, which can lead to incorrect measurements. Figure 19 gives an overview on the theoretical ways to align signals measured with different probes. A first option is to align the measured signals right at the beginning of the pulses, while a second option is to align at the ends of the pulses. Both options are marked in Figure 19 (left). Depending on the signal it might be hard to obtain the beginning or the end of the slope. A third option is to align the two signals at the 50 % value of its rising or falling edge (Figure 19 right).

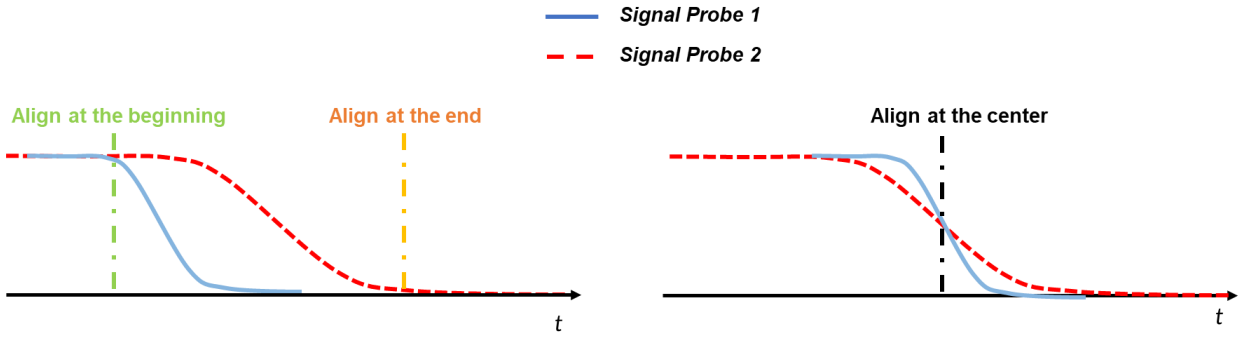


Figure 19: Voltage and current probe signals: Before de-skew (left) and after de-skew (right)

It is very important to note that the de-skew options described above can only be applied in case that two measured signals are of similar shape, e.g. voltage and current measured over a resistive load or two identical voltage signals. With the help of a configuration providing such signals, the de-skew can be performed before the measurement. The de-skew can also be performed directly with the DPT measurement setup if the setup is well known. Following are some of the methods which can be used for correct V-I misalignment.

Note that the signal propagation delays can even be slightly different for probes of same model type. Hence, whenever the probe is changed, the channels of oscilloscopes should be de-skewed. A time delay of 1 ns can lead to an error of 80 % with rise and fall times in the region of 20 to 40 ns by calculating switching energies, therefore the voltage and current signals must be de-skewed accurately [3].

- The V-I time misalignment can be eliminated with the help of a power de-skew fixture. One such example is R&S ® RT-ZF20 power de-skew fixture which can be used with the voltage and current probes from Rohde & Schwarz. The R&S ® RT-ZF20 generates pulses with different voltage swings, current swings and transit times. In order to align two probes, the delay time of the measurement signals is calibrated until it aligns the pulses on oscilloscopes display. For the usage of the de-skew fixture, the aforementioned methods for alignment can be applied. Further information about R&S ® RT-ZF20 can be found in [9]. It needs to be stated that de-skew fixtures are available for limited current and voltages only. In some cases, these can become insufficient.
- The characteristics of the DUT can directly be used for de-skew [10]. During the turn-on of the switch, the rise of the current leads to a voltage drop across the stray inductances according to $v = L_\sigma \cdot \frac{\mathrm{d}i}{\mathrm{d}t}$. This voltage drop can be observed as a dip in v_{DS} (see Figure 20). At the end of the current rise, the rate of change of current decreases and gets zero before the current starts to decrease. Hence, the voltage dip of v_{DS} gets a local maximum at the current peak value. Afterwards, the drain-source voltage collapses. Now, there are two ways to align voltage and current signals. Either the maximum of the current during turn-on can be aligned to the local maximum of the voltage v_{DS} or at the starts of voltage decay v_{DS} from V_{DC} and current rise (Figure 21). However, finding the right points in time for noisy signals might be quite troublesome. If the de-skew is set properly, it can be proved by further measurements [3].

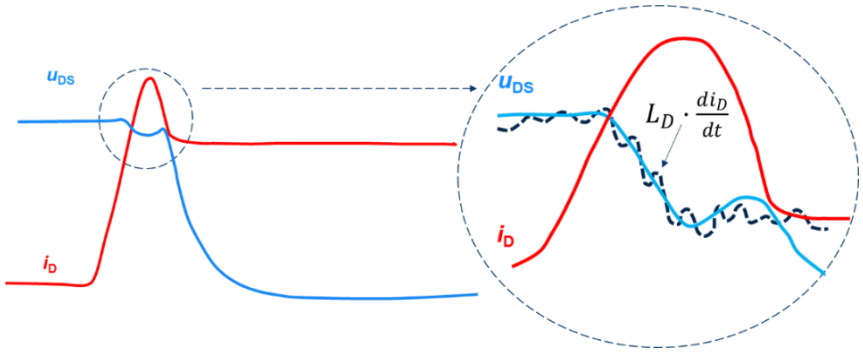
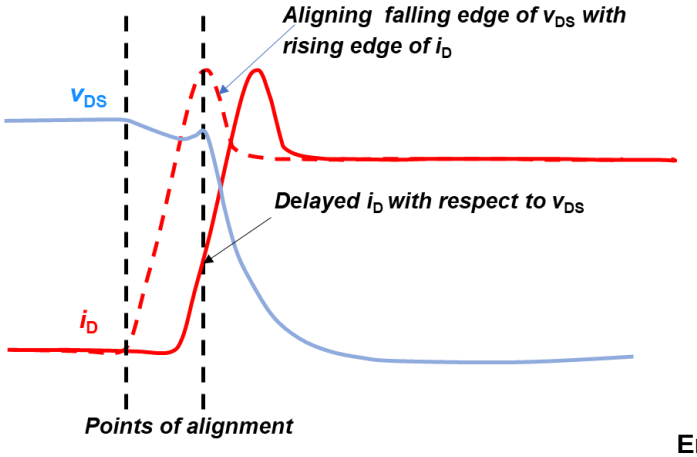


Figure 20: Graphical VI alignment using calculated voltage drop



Error! Reference source not found.

Figure 21: Manual de-skew of voltage and current probes

► The current and voltage probes can be de-skewed by removing the inductor and replacing the freewheeling diode with a resistor having low inductance [3] [11]. For ideal resistors, the voltage is proportional to the current and there is no phase shift between both signals. Utilizing this in practice, a parasitic series inductance of the resistor is unavoidable. Now, there are two ways: the series inductance can either be kept small and is neglected or the characteristics of the resistor are known and the phase shift can be determined. The maximum input voltage is dependent on the value of resistor and is usually in a range of several hundred volts. During the de-skew process, it should be ensured that the drain voltage is set below the maximum pulse rating of the resistor.

3.3 Common Mode Rejection Ratio (CMRR)

In order to make differential measurements (e.g. gate-source voltage on the high-side), it is important to eliminate the common mode voltage from the output since only the differential voltage is of interest. As can be seen in Figure 22, the voltage at node P is fluctuating between V_{DC} and zero if the minus rail is taken as reference. In case of differential probes, a differential amplifier is located between the oscilloscope and the probes as depicted in Figure 22. This differential amplifier is capable to attenuate the common mode voltage and thus, the ability to reject common mode voltage is referred to as Common Mode Rejection Ratio (CMRR). The CMRR is strongly dependent on frequency - as the signal frequency rises, the CMRR deteriorates.

Using two single-ended probes for differential measurements is cannot be recommended. Each probe differs slightly in frequency response, which would translate into reduced CMRR. Furthermore, the dynamic range of the measurement would be severely limited, as each oscilloscope channel would see the full common-mode signal.

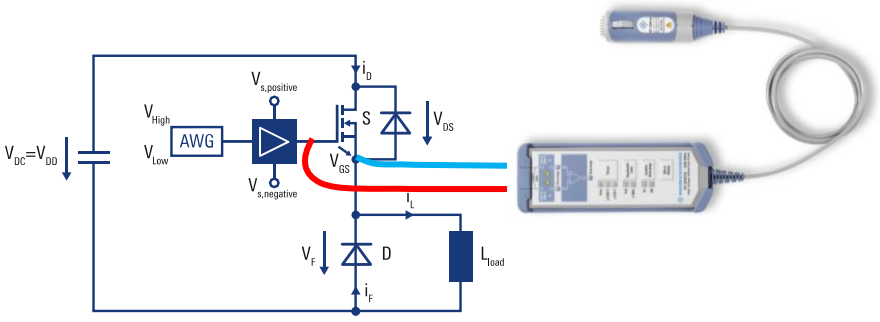


Figure 22: High-side gate measurement with a high-voltage differential probe. The switch node voltage swing is suppressed by the common mode rejection ratio of the probe.

The CMRR is decreasing over frequency. Hence, the rise/fall time of a pulse determines the bandwidth of the resulting spectrum and become the key parameter to be considered for an appropriate selection of the voltage probe. Figure 23 gives an overview about a typical CMRR performance of high voltage differential probes.

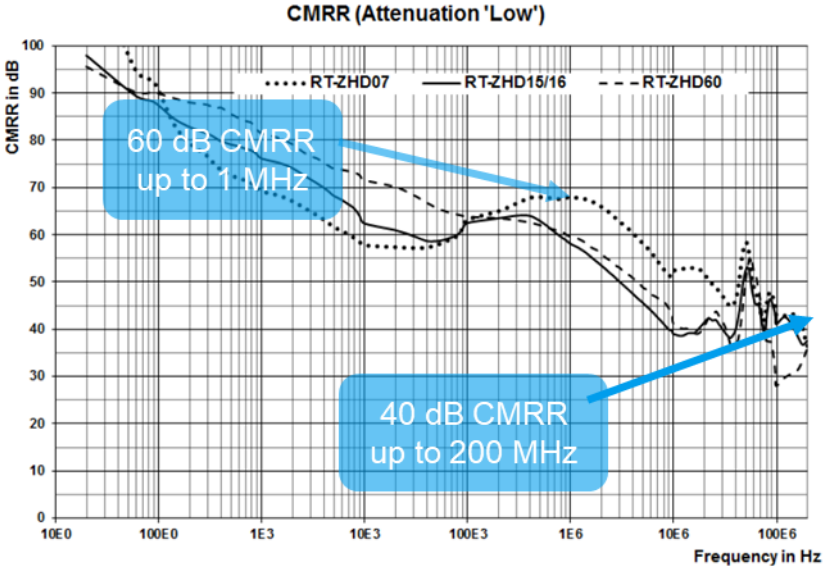


Figure 23: Typical CMRR performance of high voltage differential probes

4 Measurement Setup and Results

This chapter discusses the actual measurement setup and the results captured from the double pulse test. It also gives practical hints to obtain results from DPT.

For generating the gate drive ARB signal, it makes sense to use software tools as the one Rohde & Schwarz provides to avoid errors and make it easier to setup the test instruments. The Rohde & Schwarz GFM347 double pulse test tool guides the user from circuit parameters like the DC link voltage, inductor current and the load inductor to the necessary pulse lengths. Furthermore, a direct upload of the generated ARB signal to the generator is available. This is in particular useful since double-pulse testing is often an iterative approach, where the pulses have to be adapted many times. The double-pulse test tool is based on the LabView runtime environment and runs on Microsoft Windows.

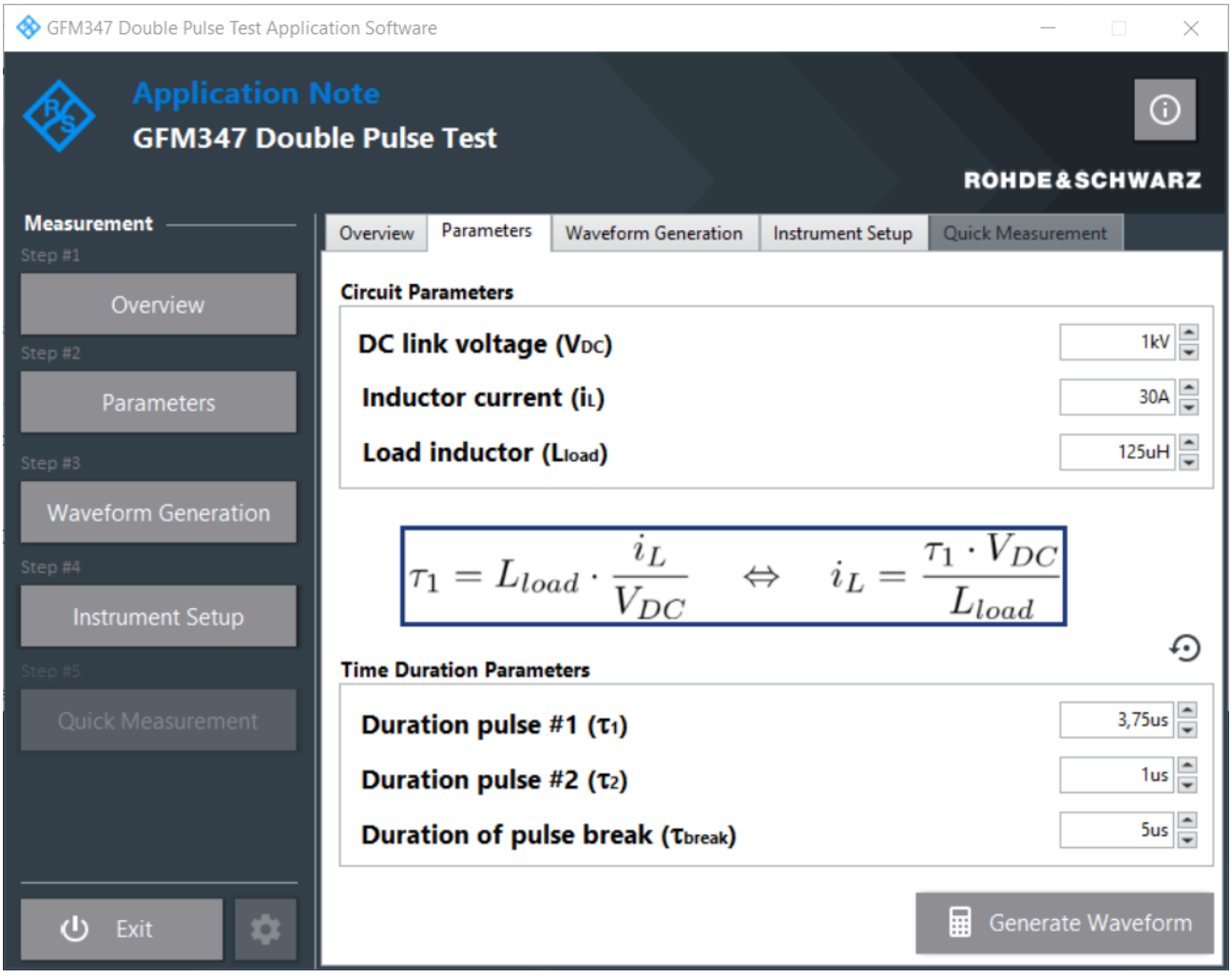


Figure 24: Parameter tab of the Rohde & Schwarz GFM347 Double-Pulse Test Tool to enter the main circuit parameters for generating a double-pulse test ARB waveform

4.1 Details of Measurement Setup

A SiC MOSFET is used as DUT. It provides a comparably fast switching time. The applied gate resistance of 14 Ω lets the device turn-on and off within 20 ns. This is a little bit slower than the 10 ns pulse shown in

Figure 15. The whole setup was chosen in a way that the 30 MHz bandwidth of the slowest current probe in use can still be applied. With a further decreasing switching time, the current probe becomes a limiting factor. The probes used for current and voltage measurement in addition to other equipment are listed in Table 5. As mentioned in the introduction of Section 3, a double pulse setup on floating potential is more flexible. Therefore, a floating setup was in use to create the following measurements.

Table 5: Probes and equipment used in the test setup

No.	Probes and Equipment	Model	Specification
1	Oscilloscope	R&S ® RTO2044	4 GHz, 20 GSa/s
2	Programmable Power Supply	R&S ® HMP4040	4 Channel, 348 W
3	Isolated Passive Probe	R&S ® RTZI10	1 kV, 500MHz
4	High Voltage Differential Probe	R&S ® RT-ZHD 07	750 V_{PK} Diff, 200 MHz
5	Coaxial Shunt	T&M SSDN-414-10	0.1 Ω, 2 GHz
6	Rogowski Coil	PEM CWT Mini 50 HF 06	120 A, 8 A/ns, 50 MHz
7	Rogowski Coil	PEM CWT Ultra-mini 06	120A, 8 A/ns, 30 MHz
8	DC Power Supply	FUG MCP 1400-2000	2000V, 600mA

4.2 Test Results

4.2.1 Switching Transients

Figure 25 depicts the waveform of the gate-source voltage, drain-source voltage and device current resulting from the double pulse test. Figure 26 and Figure 27 show the enlarged view of the turn-off and the turn-on instants. These instants are used to determine the switching energies, voltage and current overshoots, rise time, fall time and delay times. The current measurement is performed using a Rogowski coil (PEM CWT [12] Ultra-mini [13]) while the voltage measurement is performed using the high voltage differential probe R&S ® RT-ZHD07. As discussed earlier, the overshoots and voltage dip caused by parasitics can be observed on the drain-source voltage and on the drain current. Besides that, at the drain current shows some ringing during the turn-off event shown in the overview on Figure 25. This ringing is typical for an unintended coupling into the current probe. Be careful with the placement of the probes inside your circuit.

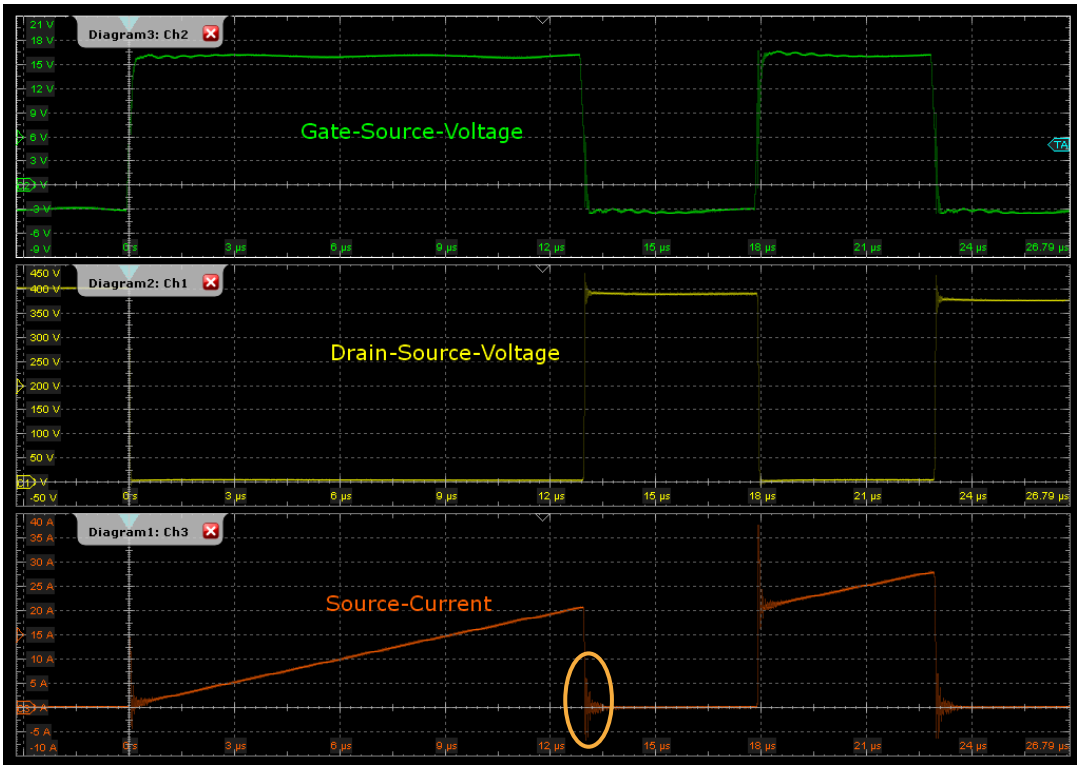


Figure 25: Double pulse test waveform

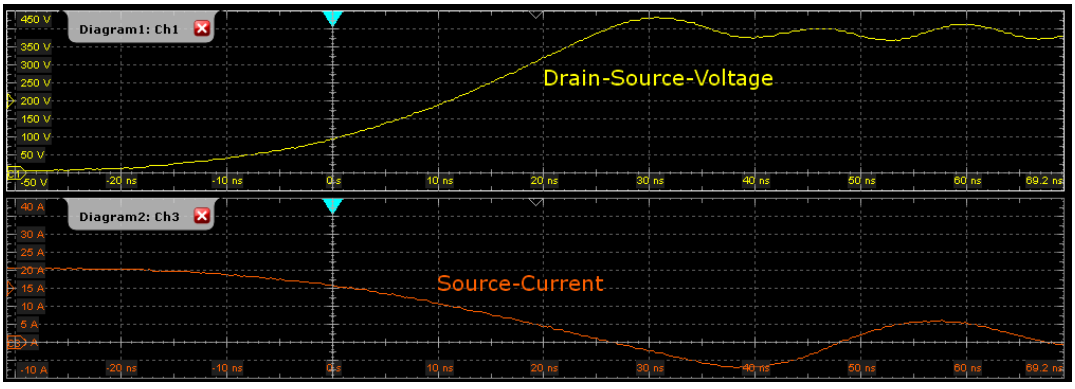


Figure 26: Turn-off transient

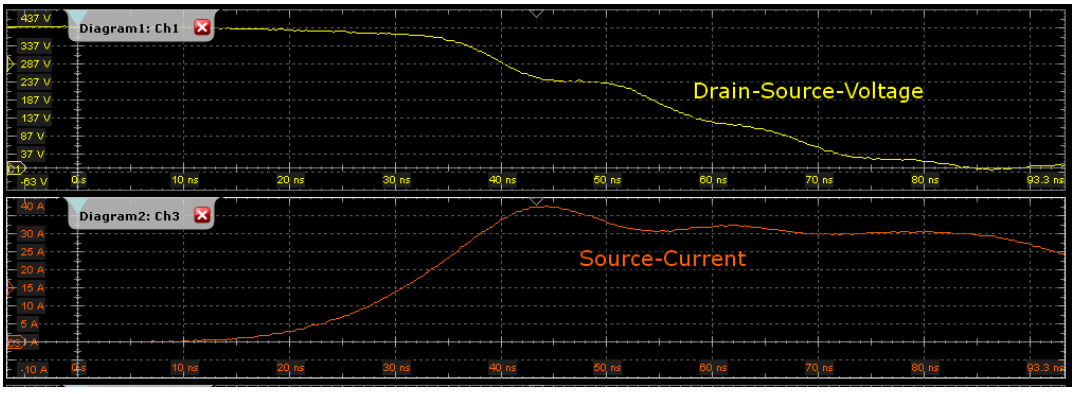


Figure 27: Turn-on transient

4.1.1 Current Measurement

Figure 28 gives an overview on the drain source voltage and the drain current measured with three different current probes. The applied probes are the ones listed in Table 5. On the left side of Figure 28, the measured currents are shown without a de-skew. The blue signal is the coaxial shunt which is the current probe with the highest bandwidth. The green signal on channel two is a PEM UK CWT mini HF Rogowski coil [14] while the third one is a PEM UK CWT ultra mini Rogowski coil. It can be seen that all sensors have a different group delay and a de-skew is required. After the de-skew shown on the right side of Figure 28, all probes deliver a comparable result.

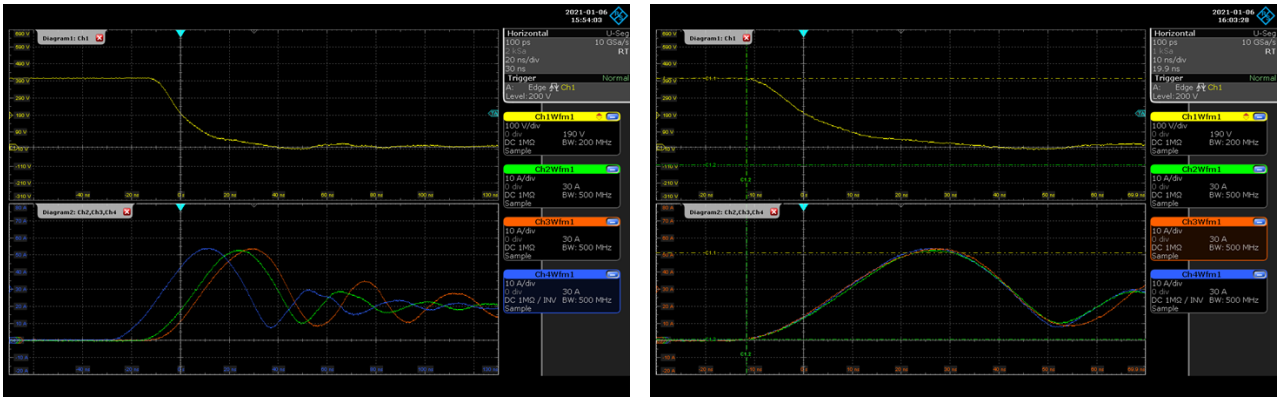


Figure 28: Measurement results of different current probes before (left) and after (right) de-skew. blue: Coaxial shunt of T&M, green: PEMUK CWT Mini HF, orange: PEMUK CWT ultra mini

4.1.2 Voltage Measurement

As mentioned previously in the document, long leads and pins add to the parasitic components which cause ringing and overshoots in the resulting waveforms. Therefore, the probe leads are twisted. This measure increases the capacitive loading by a few pF which is negligible for most devices. Figure 29 shows the drain-source voltages of a turn-on event and a turn-off event measured with two different probes. On channel 2 (green), an R&S ® RT-ZH10 passive probe was used and kept as the reference. In addition, an R&S ® RT-ZHD07 differential probe was connected to channel 3 (orange). For comparability reasons, the probes were connected to the same pin heads close to the device under test. For the turn-on event, it can be seen that both probes deliver comparable results after a de-skew was made with 1.5 ns on the differential probe (both signals were aligned at its 50 % value). For the turn-off, both signals follow the same behavior. However, the differential probe shows a higher magnitude of the resulting ringing of the signal. The ringing of the voltage can be kept as true. This resonance is caused by the stray inductance of the circuit, which forms a resonance circuit with the device's capacitances.

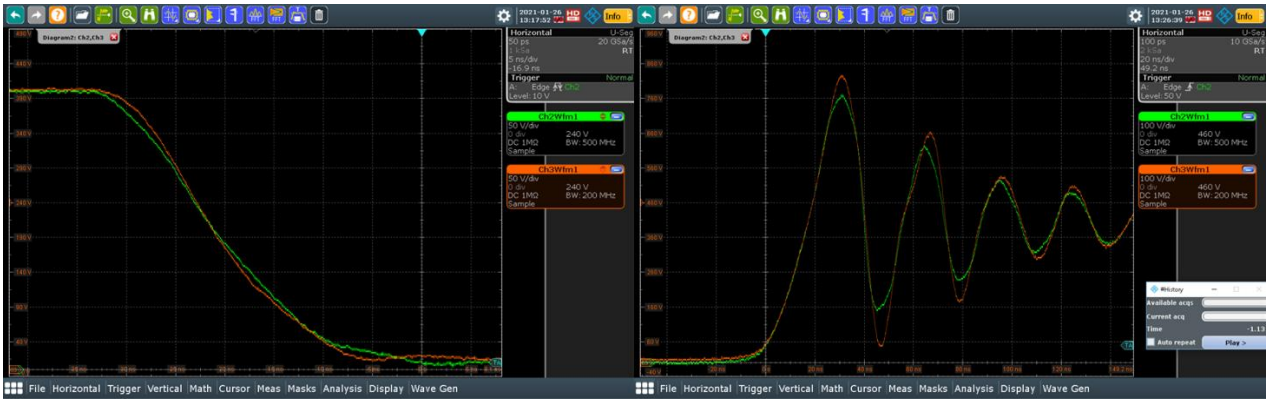


Figure 29: Turn-on (left) and turn-off (right) measurements of v_{DS} with different probes

4.1.3 Switching Energy Calculations and Switching Behavior

In order to determine the switching losses and the switching energy, the math functions of the oscilloscope can be used. As the power is determined by $P(t) = v_{\mathrm{DS}}(t) \cdot i_{\mathrm{D}}(t)$, it can be displayed by an additional math-trace showing the product of the corresponding channels. Note that the ratio of the probes needs to be set correctly in order to get proper results.

For the total energy dissipated during the switching process, $E_{\mathrm{switching}} = \int_0^T P(t)\mathrm{d}t$ holds and thus, it can be calculated by a second math channel integrating the first one. The settings for both channels are displayed in Figure 30, where the current i_{D} and the voltage v_{DS} are measured on C1 and C3.

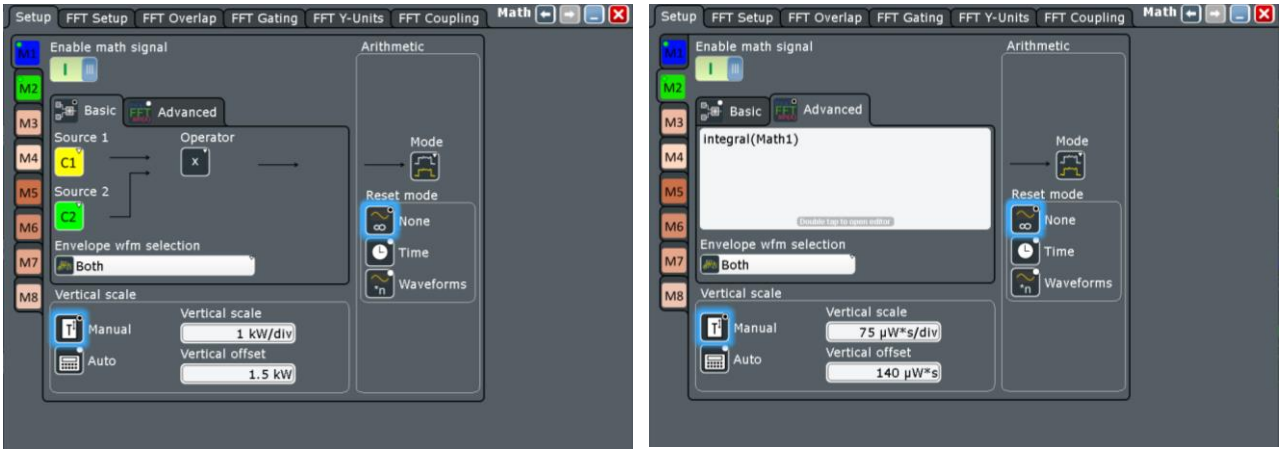


Figure 30: Setting up the math channels for the evaluation of the switching power (left) and the switching energy (right).

The resulting measurement curves can be seen in Figure 31 for the turn-on event.

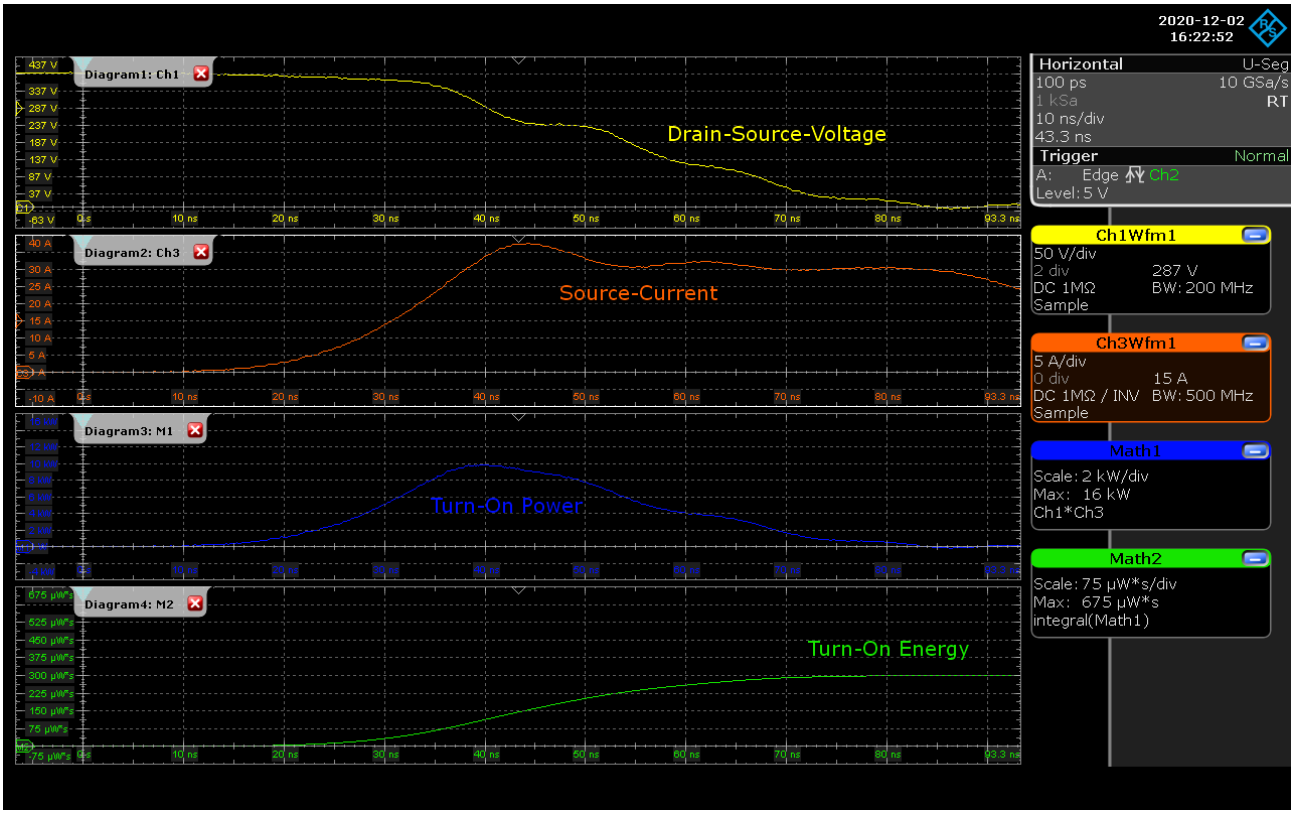


Figure 31: Screenshot of the turn-on event measured by the R&S ® RTO2000. In addition to the drain-source voltage (yellow) and the source current (red), the switching power (blue) and energy (green) evaluated by the math functions of the instrument are displayed (see section 4.1.3).

As explained in Section 2.2.2, the energy is evaluated between certain characteristic values only. For the turn-on process, the energy is to be evaluated between the 10 % value of the source current and the 10 % value of the drain-source voltage. With the oscilloscope, this can precisely be done using the cursor functionality (further explained in the next chapter). Here, a first cursor pair was used to determine the 10 % values of the drain-source voltage and the source current. Afterwards, a second cursor pair was aligned with the first pair to determine the difference in energy. For the measurement shown in Figure 31, 237 µWs were determined with the cursors, resulting in a deviation of 5.9 % from the total integral over the switching losses (251 µWs).

4.1.4 Actual De-skew Procedure

The screenshot in Figure 31 shows the turn-on measured low-side by an RTO oscilloscope without any de-skew measures. It will be shown that even this small misalignment between both curves does have a visible influence on the evaluated switching losses. A de-skew is performed in the following to show the process using an RTO and to show the influence on the evaluated switching performance. For the de-skew the device characteristics are used as described in Section 0.

In order to see the actual time offset between measured voltage and current, a horizontal zoom in combination with the cursor function can be used as shown in Figure 33. Here, cursor $C_{1,1}$ is placed at the current maximum while cursor $C_{1,2}$ is matched to the local minimum caused by the voltage across parasitic inductance L_D (as shown in Figure 21).

For the cursors, a combined cursor (horizontal and vertical) with two sources (one for the voltage and one for the current signal) is used with “Track waveform” enabled (see Figure 32).

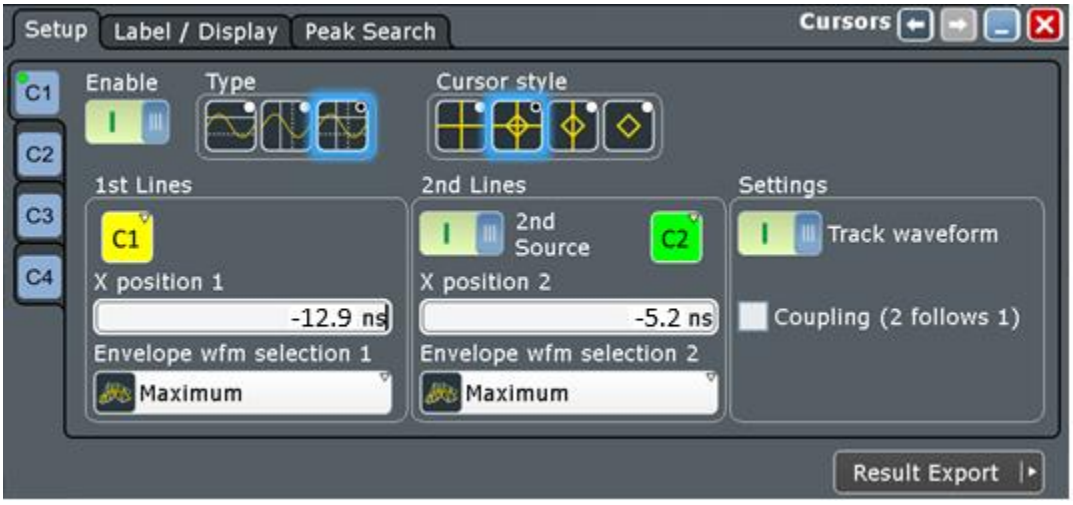


Figure 32: Cursor settings to evaluate the time offset between drain-source voltage and source current.

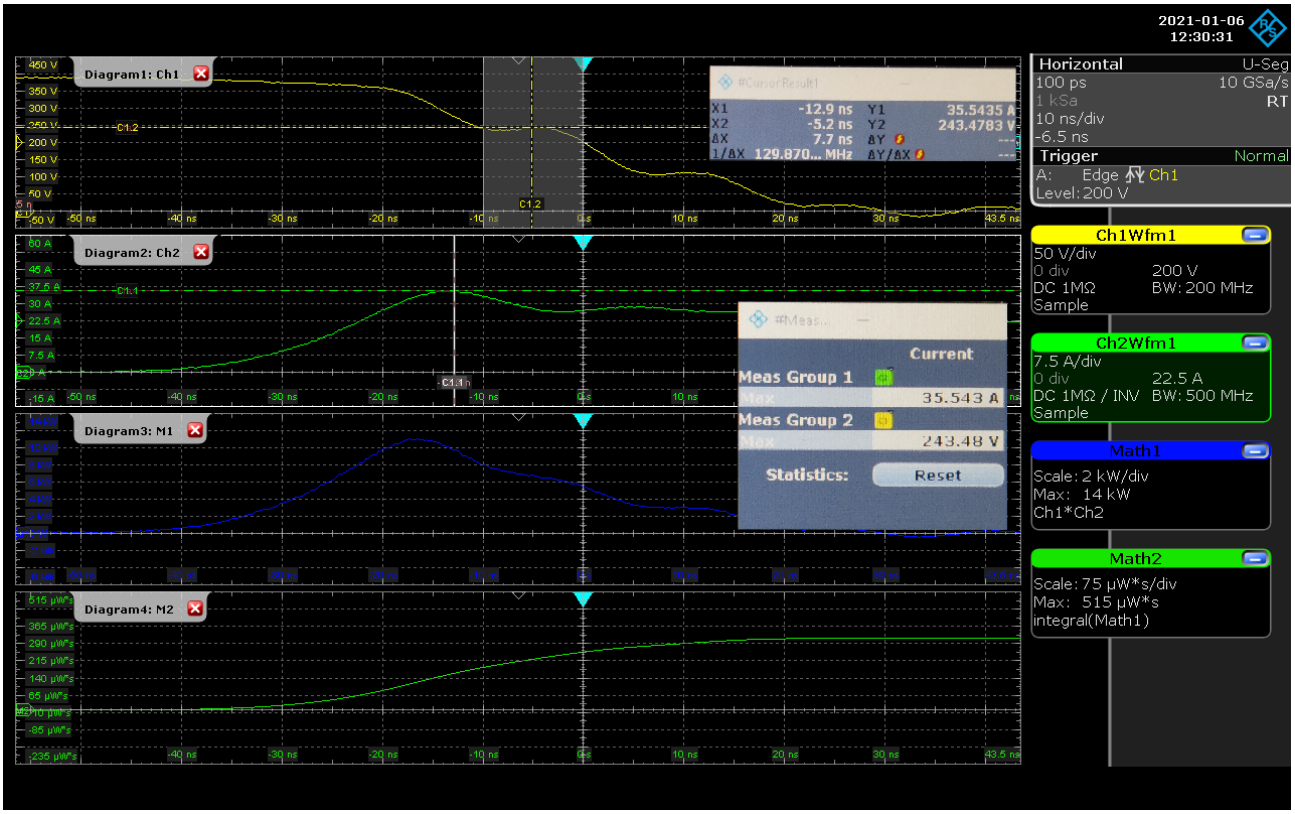


Figure 33: Resulting screen for the de-skew between drain-source voltage and the drain current. The cursors are placed on the current maximum and the local voltage maximum, caused by the parasitic inductances, making use of the oscilloscopes measure functions.

To find the exact cursor positions, the measure functions of the RTO were used. As the current peak is the global maximum during the turn-on, it can be determined by the Max-measurement (Meas → Meas Group → Category: Amp/Time. Active Measurements: Max). For the voltage, the local maximum needs to be measured. This can be achieved by “Measurement gating”. Using a new measurement group, “Max” needs to be chosen. In addition, the gating needs to be enabled (Meas → Gate/Display → Use Gate). The position of the gate can either be adjusted using the “Gate definition” in the “Gate/Display” menu (see right side of Figure 34) or by using the Touch-screen afterwards. To display the corresponding values, “Group result dialogs” needs to be enabled in the “Gate/Display” menu as well.

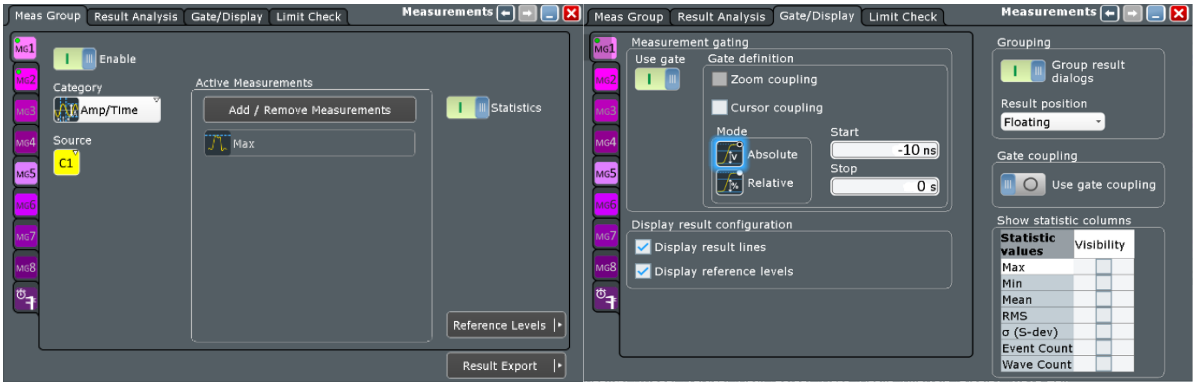


Figure 34: Measurement settings for maximum / minimum measurements (left) and the additional settings for the gating for the local voltage minimum (right).

Afterwards, the cursors can be adjusted until the evaluated current maximum and voltage minimum are met. The required time offset is now displayed as the Δx-value between both cursors, in our case 7.7 ns.

Knowing the time offset, the de-skew functionality of the oscilloscope can be used (Select Channel (i_D-channel) → Probe Setup → De-skew).

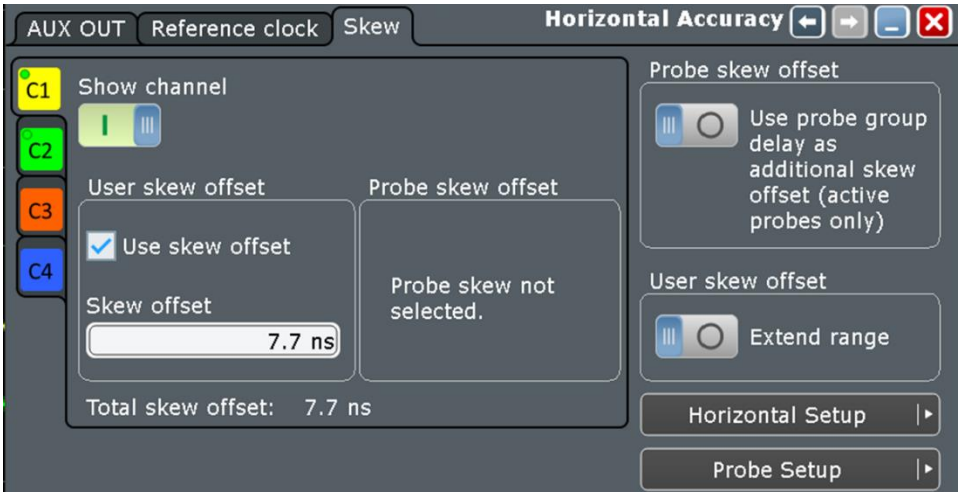


Figure 35: Correcting the time offset with the integrated de-skew function of the oscilloscope.

Figure 36 shows the resulting measurement after the de-skew. We note the time de-skew of 7.7 ns corrects the switching energy from 320 µWs to 221 µWs, corresponding to a deviation of almost 45 % from the de-skewed value.

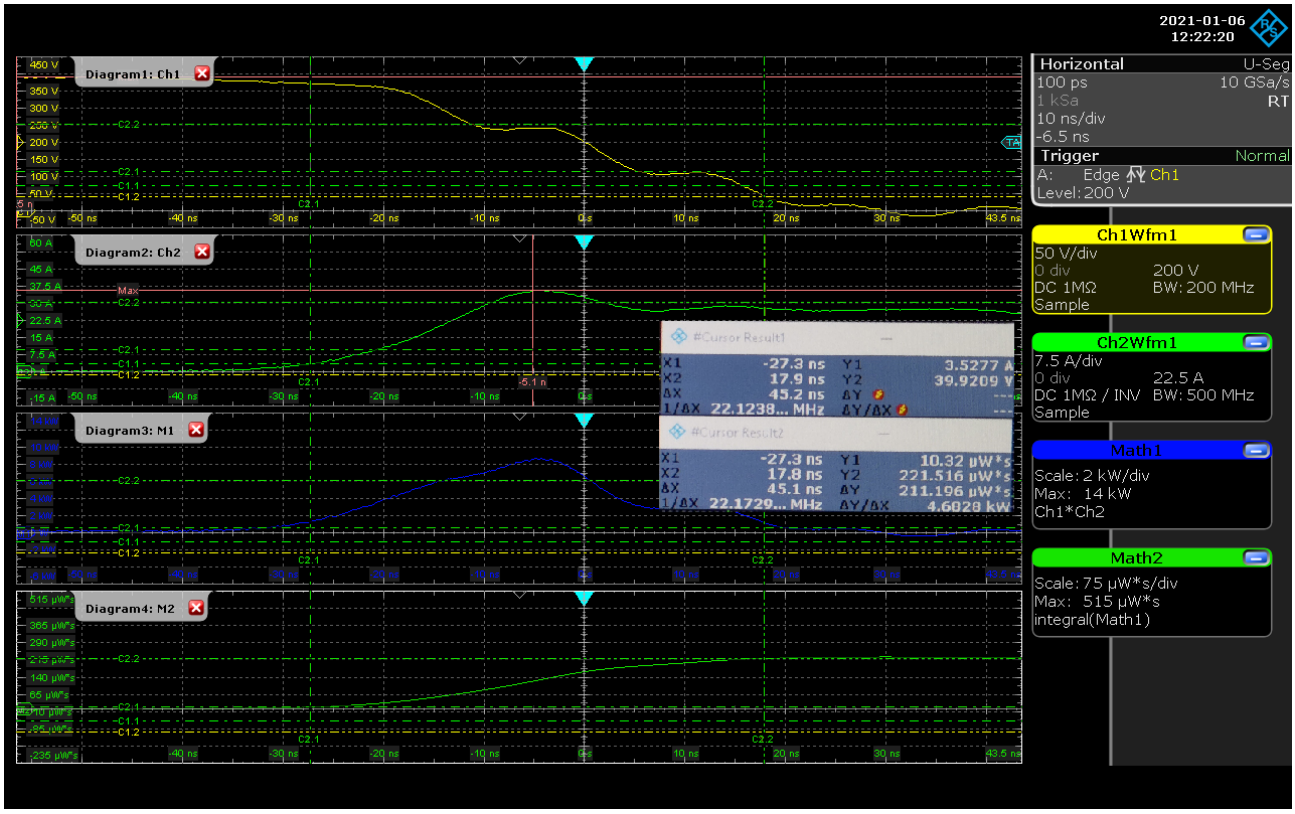


Figure 36: Turn-on energy measurement after de-skew

5 Conclusions

Double Pulse testing is a standard-testing method with many different use cases in power electronics design. In particular for device characterization, it is important to carefully design the test setup to avoid measurements errors due to excessive parasitics and ensure safe operation. Selecting the right probing solution and carefully considering de-skew are other elements essential for accurate measurements. Even small errors in de-skew can lead to large deviations in switching loss measurements leading to wrong conclusions. Since double-pulse testing is often done iteratively, it makes sense to use SW tools for generating the gate drive ARB signal as the one R&S provides.

6 References

[1] Johann Asam, et. al. (Danfoss Silicon Power GmbH, Germany), "Improved Double-Pulse Tests for Medium-Voltage Devices," in *PCIM Europe digital days*, 2020.

[2] VISHAY, "Application Note- Vishay General Semiconductor- Rectifier," 16 08 2011. [Online]. Available: https://www.vishay.com/docs/84064/anphyexp.pdf. [Accessed 22 01 2021].

[3] Zheyu Zhang, et. al., "Methodology for Wide Band Gap Device Dynamic Charaterization," in *IEEE Transactions on power electronics, Vol. 32, No. 12*, 2017.

[4] Andreas Volke, Michael Hornkamp (Infineon Technologies AG), IGBT Modules Technologies, Driver and Application - ISBN 978-3-00-040134-3, 2012.

[5] G. a. J. K. Laimer, "Accurate Measurement of the Switching Losses of Ultra High Switching Speed CoolMOS Power Transistor / SiC Diode Combination Employed in Unity Power Factor PWM Rectifier Systems.," 2002. [Online]. Available: https://www.pes-publications.ee.ethz.ch/uploads/tx_ethpublications/laimer_PCIM-PQC02.pdf. [Accessed 22 01 2022].

[6] Rohde & Schwarz, "Product Brochure, "PROBES AND ACCESSORIES", Version 15.00," [Online]. Available: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/Probes_and_accessories_bro_en_3606-8866-12_v1500.pdf. [Accessed 22 01 2021].

[7] Rohde & Schwarz, "High Voltage And Current Probes," 2020. [Online].

[8] Teridian Semiconductor Corp., "Application Note : Using Current Transformer with the 78M661," 2010. [Online]. Available: https://pdfserv.maximintegrated.com/en/an/AN4841.pdf. [Accessed 22 01 2021].

[9] Rohde & Schwarz, "R&S®RT-ZF20 Power Deskew Fixture Manual," 2019. [Online]. Available: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/pdm/cl_manuals/user_manual/1800_0040_01/RT-ZF20_UserManual_en_05.pdf. [Accessed 22 01 2021].

[10] E. Jones, et. al., "Characterization of an enhancement-mode 650-VGaN HFET," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015.

[11] CREE, "SiC MOSFET Double Pulse Fixture," [Online]. Available: https://dtsheet.com/doc/1318858/sic-mosfet-double-pulse-fixture?. [Accessed 21 01 2020].

[12] PEM, "CWT Technical notes- HF and Rise-time-01A," 2018. [Online]. Available: https://gmw.com/wp-content/uploads/2019/06/CWT-Technical-notes-HF-and-Rise-time-01A.pdf. [Accessed 22 01 2021].

[13] PEM, "CWT Ultra-mini Datasheet".

[14] PEM, "Datasheet on CWTMini50HF," 2020. [Online]. Available: http://www.pemuk.com/Userfiles/cwtmini50hf/CWT_Mini50HF_DS_Feb_2020.pdf. [Accessed 22 01 2021].

[15] Rohde & Schwarz, "Datasheet : R&S RT-Zxx High Voltage and Current Probes Specification," 2020. [Online]. Available: https://www.datatec.de/media/pdf/4e/7b/eb/Rohde-Schwarz-1333-0873-02-DB-1_DEFePF6BWjaZCV5.pdf. [Accessed 22 01 2021].

[16] Infineon Technologies AG - International Rectifier, "Application Note AN-983," 2012. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGBT_Characteristics-AN-v01_00-EN.pdf?fileId=5546d462533600a40153559f8d921224. [Accessed 22 01 2021].

[17] STMicroelectronics, "Application note : Current sensing in metering applications using a Pulse current sensor and ST metering devices," November 2010. [Online]. Available: https://www.st.com/resource/en/application_note/cd00289924-current-sensing-in-metering-applications-using-a-pulse-current-sensor-and-st-metering-devices-stmicroelectronics.pdf. [Accessed 23 01 2021].

[18] B. Callanan, "SiC MOSFET double pulse fixture 2011.," in *Available: http://www.cree.com*, 2011.

Rohde & Schwarz

The Rohde & Schwarz electronics group offers innovative solutions in the following business fields: test and measurement, broadcast and media, secure communications, cybersecurity, monitoring and network testing. Founded more than 80 years ago, the independent company which is headquartered in Munich, Germany, has an extensive sales and service network with locations in more than 70 countries.

www.rohde-schwarz.com

Certified Quality Management
ISO 9001

Rohde & Schwarz training

www.training.rohde-schwarz.com

PAD-T-M: 3572.7186.00/01.00/EN

Rohde & Schwarz customer support

www.rohde-schwarz.com/support

GFM347 | Version 1.00 | 03.2021
Application Note | Tips & Tricks on Double Pulse testing
Data without tolerance limits is not binding | Subject to change

www.rohde-schwarz.com