

Application Note

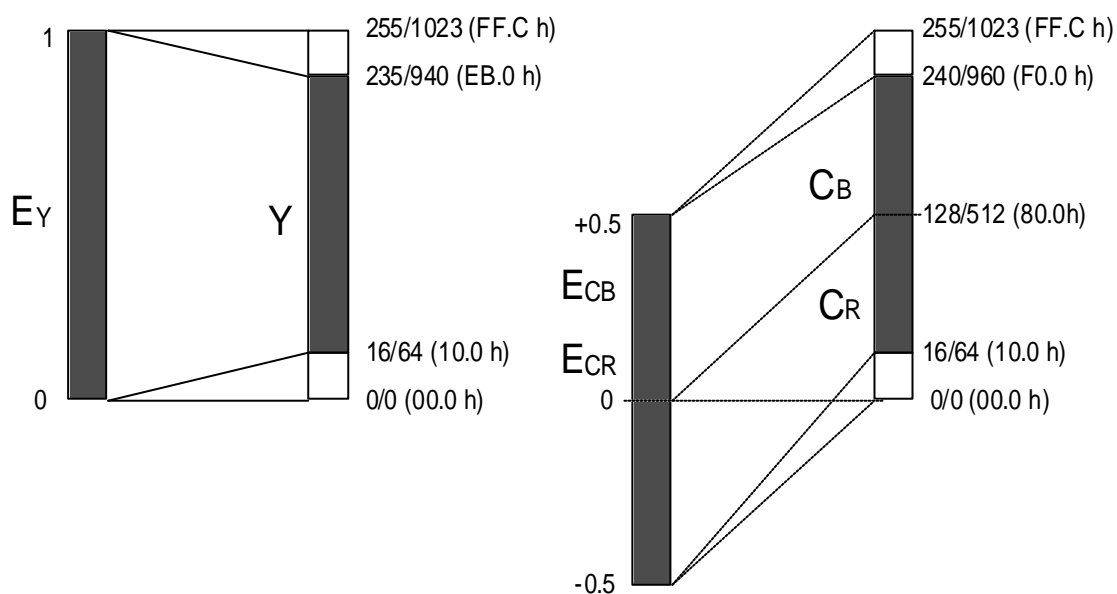
**The digital Video Standard
according to
ITU-R BT. 601/656**

Products:

<i>CCVS+COMPONENT GENERATOR</i>	SAF
<i>CCVS GENERATOR</i>	SFF
<i>DIGITAL VIDEO COMPONENT ANALYSER</i>	VCA

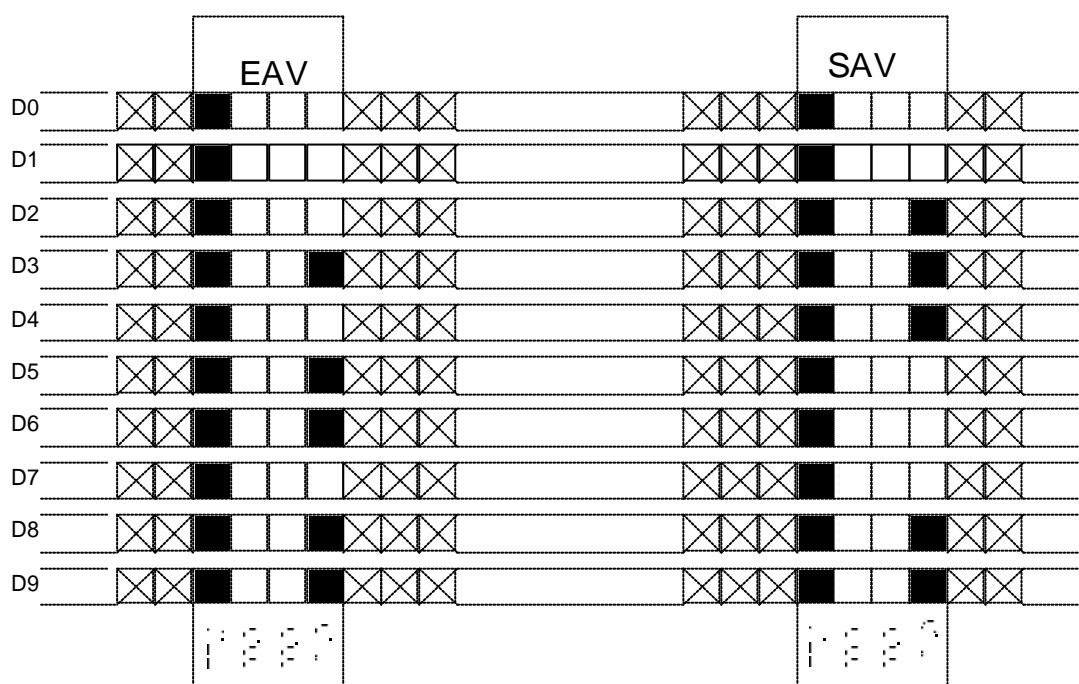
ITU-R BT. 601

Level diagram at the input of an A/D converter for the analogue component signals Y, C_B, C_R



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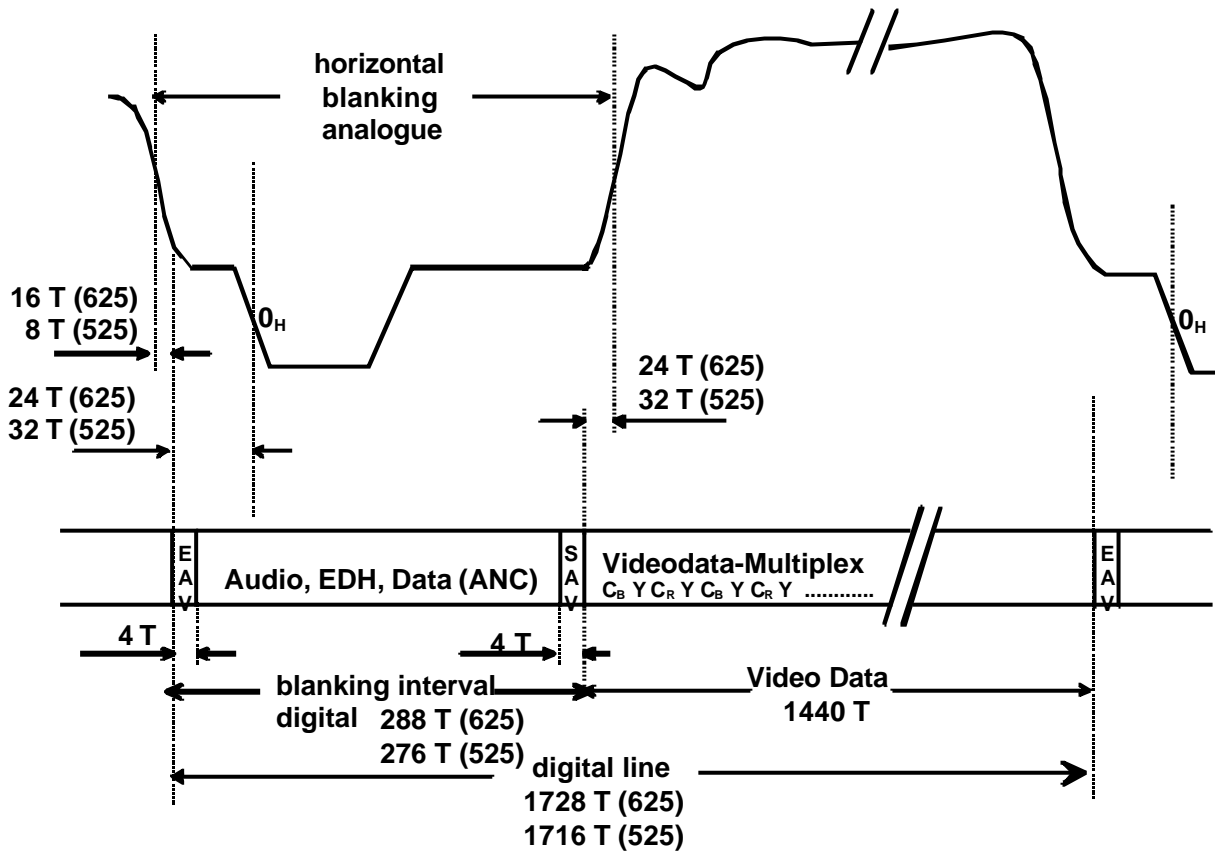
Example for digital synchronizing signals in the parallel interface (10 bit)



black points indicate the value 1 , white points 0
 XY within EAV is DA.0 (11011010 00)
 XY within SAV is C7.0 (1100011100) this signifies
 this line an active one in an even field

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Data format and timing relationship with the analogue video signal



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structure of digital synchronizing signals

code word			bit number											
			9	8	7	6	5	4	3	2	1	0		
first	word	(FF.C)	1	1	1	1	1	1	1	1	1	1	1	1
second	word	(00.0)	0	0	0	0	0	0	0	0	0	0	0	0
third	word	(00.0)	0	0	0	0	0	0	0	0	0	0	0	0
fourth	word	(XY.0)	1	F	V	H	P3	P2	P1	P0	0	0	0	0

F = 0 first field
 F = 1 second field
 V = 0 or 1 (in VBI)
 H = 0 in SAV
 H = 1 in EAV
 P0, P1, P2, P3 see table of control bits

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Table of values for V, F in VBI

interval to be marked	line number	
	system 525/60	system 625/50
digital vertical blanking interval		
field 1 start (V=1)	1	624
end (V=0)	10	23
field2 start (V=1)	264	311
end (V=0)	273	336
digital field		
field 1 start (F=0)	4	1
field 2 start (F=1)	266	313

The values of V and F change within the transmission of the EAV signal at the start of each digital line.

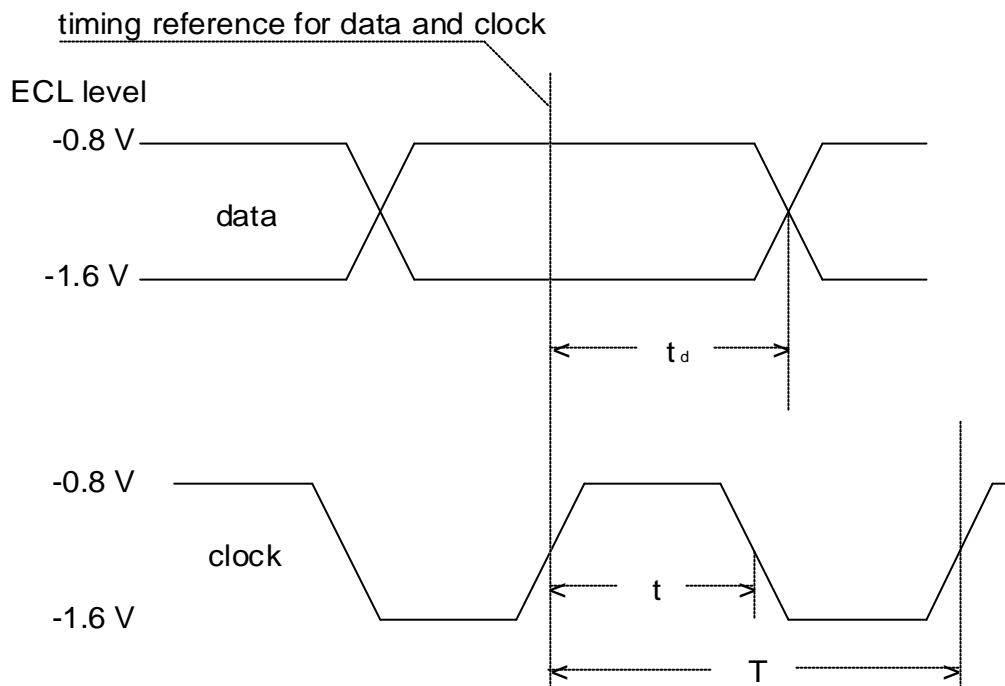
The line numbers count according to ITU-R BT. 470; the number of the digital line changes at the reference point 0_H.

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Table of controlbits

const.	F	V	H	P3	P2	P1	P0	const.	const.	XY.0	level dec.			
1	0	0	0	0	0	0	0	0	0	80.0	128.0	1st field	active picture	SAV
1	0	0	1	1	1	0	1	0	0	9D.0	151.0			EAV
1	0	1	0	1	0	1	1	0	0	AB.0	171.0		VBI	SAV
1	0	1	1	0	1	1	0	0	0	B6.0	182.0			EAV
1	1	0	0	0	1	1	1	0	0	C7.0	199.0	2nd field	active picture	SAV
1	1	0	1	1	0	1	0	0	0	DA.0	218.0			EAV
1	1	1	0	1	1	0	0	0	0	EC.0	236.0		VBI	SAV
1	1	1	1	0	0	0	1	0	0	F1.0	241.0			EAV

Signal Timing and Levels (parallel interface)



Clock-to-data Timing (at source)

clock period (625):	$T = 1 / (1728 \times f_H) = 37.037 \text{ ns}$
clock period (525):	$T = 1 / (1716 \times f_H) = 37.037 \text{ ns}$
clock pulse width:	$t = 18.52 \pm 3 \text{ ns}$
data timing - sending end:	$t_d = 18.5 \pm 3 \text{ ns}$
f_H = line frequency	

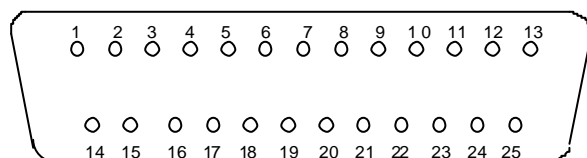
variation of data timing - sending end in SAF and SFF : $18.5 \pm 10 \text{ ns}$

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Connector contact assignments

The connector's contacts, numbered in the standard manner depicted below must be assigned in accordance with the following table

Contact	Assignment	Contact	Assignment
1	clock	14	clock return
2	system ground	15	system ground
3	data 9 (MSB)	16	data 9 return
4	data 8	17	data 8 return
5	data 7	18	data 7 return
6	data 6	19	data 6 return
7	data 5	20	data 5 return
8	data 4	21	data 4 return
9	data 3	22	data 3 return
10	data 2	23	data 2 return
11	data 1	24	data 1 return
12	data 0	25	data 0 return
13	chassis ground		



Connector containing male pins (plug)

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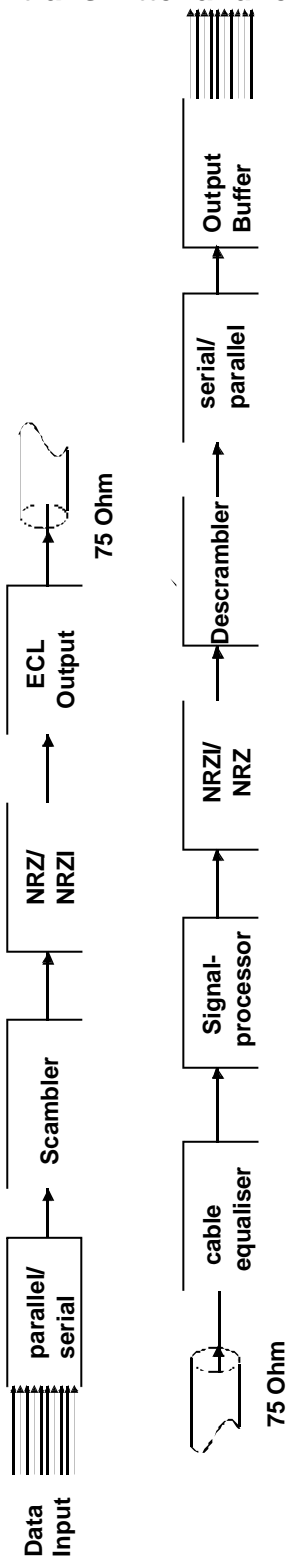
Serial System Parameters

ITEM	4 : 2 : 2 (D1)	4 x f _{SC} PAL (D2)	4 x f _{SC} NTSC (D2)
total bit rate Mb / s	270.0	177.3	143.2
resolution	10 (8) bit / word		
channel coding	scrambled NRZI by $G(x) = (x^9 + x^4 + 1)(x + 1)$		
serial sync word	3FF, 000, 000 hex (10 bit)		
order of transmission	LSB first		
nominal signal level	800 mV ± 10% (terminated)		
code limitation	000 through 003 and 3FC through 3FF shall not appear in any data words		

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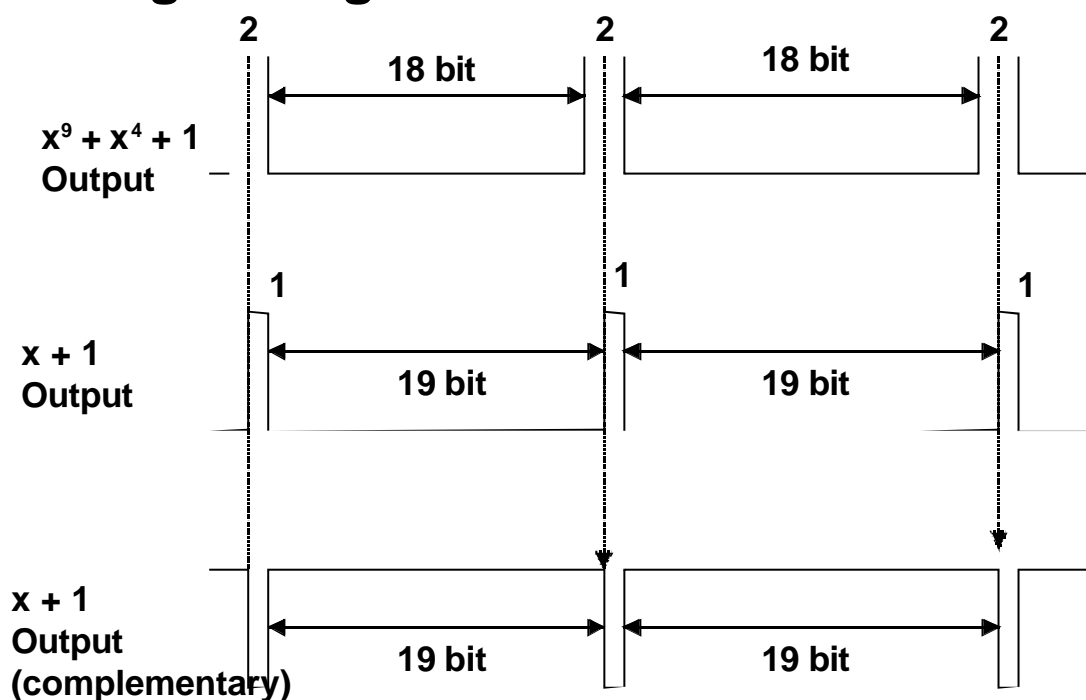
serial 270 Mbit / sec

Diagram of transmitter and receiver line



serial 270 Mbit / sec

Pathological Signals for 10 bit Serial Interface

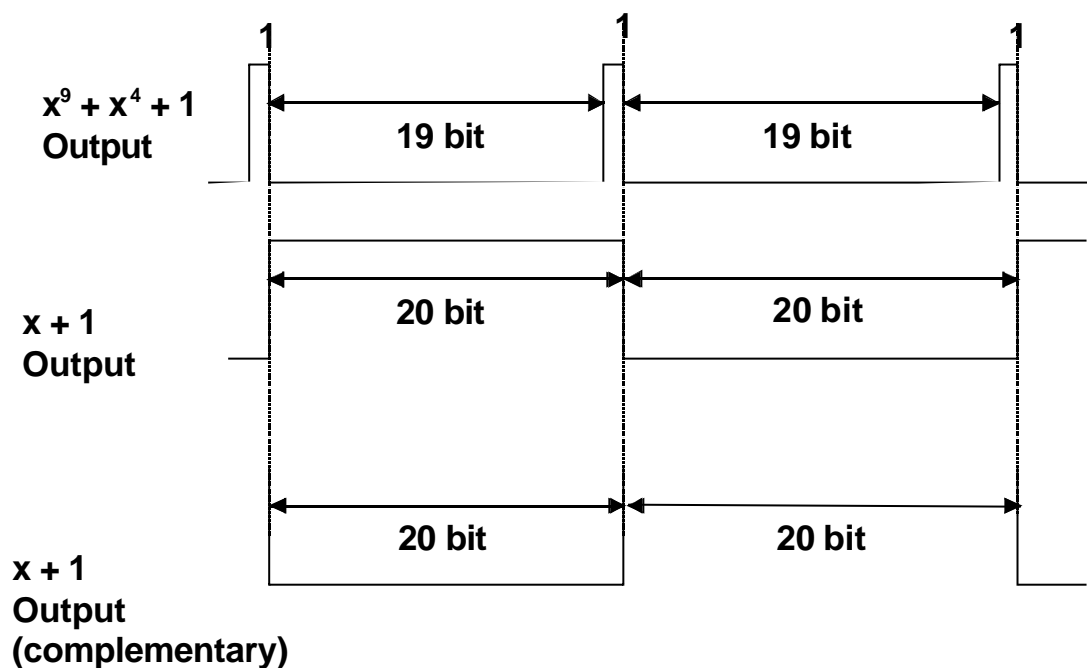


Signal for Testing the Cable Equaliser

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serial 270 Mbit /sec

Pathological Signals for 10 bit Serial Interface



Signal for Testing the PLL in the Receiver

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SAF / SFF Signalgroup ITU-R BT. 601 (Option)

Signaloverview

according to ITU-R BT. 801

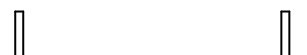
CCIR 601	
1 GREY LEVEL	21 PATHOL.SIGNAL Y=088h C=100h
2 ALTERNATING BLACK/WHITE	22 PATHOL.SIGNAL Y=044h C=080h
3 EOL PULSE	23 PATHOL.SIGNAL Y=022h C=040h
4 BLACK/WHITE	24 PATHOL.SIGNAL Y=011h C=020h
5 RAMP YELLOW/GREY	25 PATHOL.SIGNAL Y=008h C=210h
6 RAMP GREY BLUE	26 PATHOL.SIGNAL Y=198h C=108h
7 RAMP CYAN GREY	27 PATHOL.SIGNAL Y=004h C=300h
8 RAMP GREY RED	28 PATHOL.SIGNAL Y=0CCh C=180h
9 RAMP CB Y CR Y	29 PATHOL.SIGNAL Y=066h C=0C0h
10 EOL BAR WHITE	30 PATHOL.SIGNAL Y=033h C=060h
11 EOL BAR BLUE	31 PATHOL.SIGNAL Y=019h C=230h
12 EOL BAR RED	32 PATHOL.SIGNAL Y=00Ch C=318h
13 EOL BAR YELLOW	33 PATHOL.SIGNAL Y=006h C=18Ch
14 EOL BAR CYAN	34 DIG.COL.BARS 100/0/100/0
15 SEQUENCE 1010	35 DIG.COL.BARS 100/0/75/0
16 SEQUENCE 11001100	36 RAMP Y
17 SEQUENCE 111000111000	37 RAMP Y CB CR
18 SDI CHECK FIELD	38 RAMP CB
19 PATHOL.SIGNAL Y=198h C=300h	39 RAMP CR
20 PATHOL.SIGNAL Y=110h C=200h	



Pathological Signals

1. Pathological Signals for Cable Equalizers in the Serial Digital Interface

Possible word combinations to generate a stress pattern for cable equalization



No.	Hex		Validity	
	chroma 1st sample	luminance 2nd sample	4 : 2 : 2 D1	
			10 bit	8 bit
1	200 h	331 h	yes	no
2	300 h	198 h	yes	yes
3	180 h	0CC h	yes	yes
4	0C0 h	066 h	yes	no
5	060 h	033 h	yes	no
6	230 h	019 h	yes	no
7	318 h	0CC h	yes	yes
8	18C h	006 h	yes	no

2. Pathological Signals for Genlock of PLL in the Serial Digital Interface

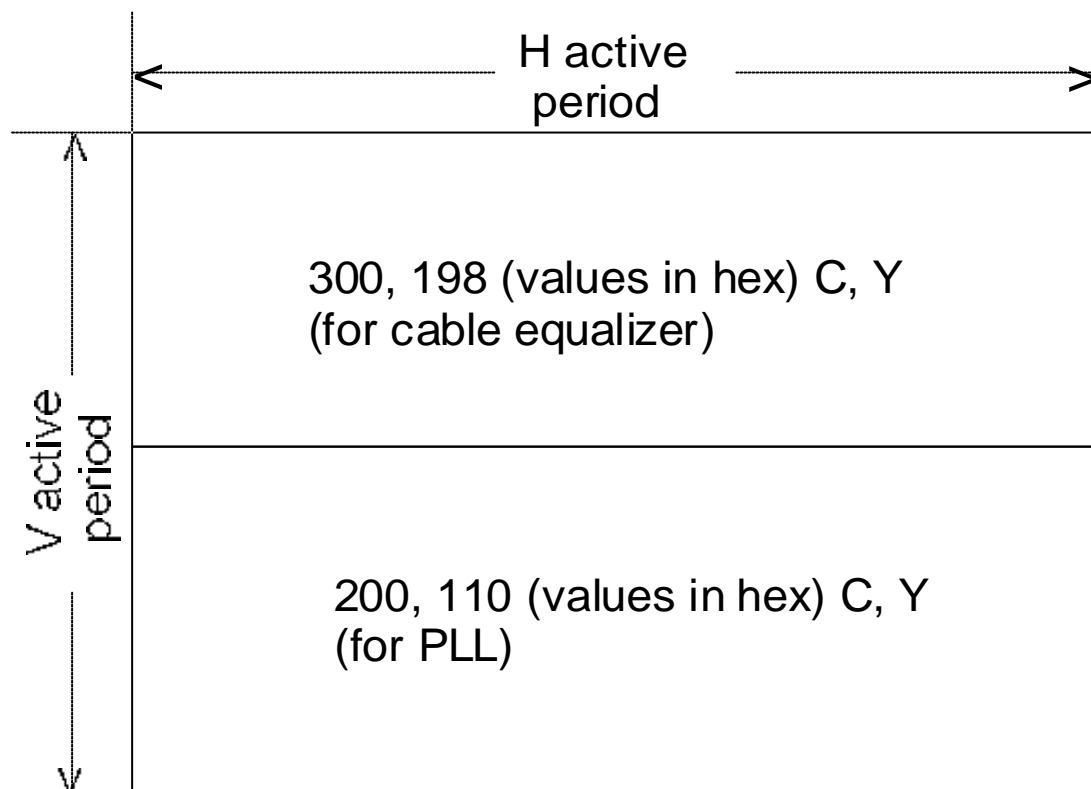
Possible word combinations to generate a stress pattern for genlock of PLL



No.	Hex		Validity	
	chroma 1st sample	luminance 2nd sample	4 : 2 : 2 D1	
			10 bit	8 bit
1	200 h	110 h	yes	yes
2	100 h	088 h	yes	yes
3	080 h	044 h	yes	yes
4	040 h	022 h	yes	no
5	020 h	011 h	yes	no
6	210 h	008 h	yes	yes
7	108 h	004 h	yes	yes

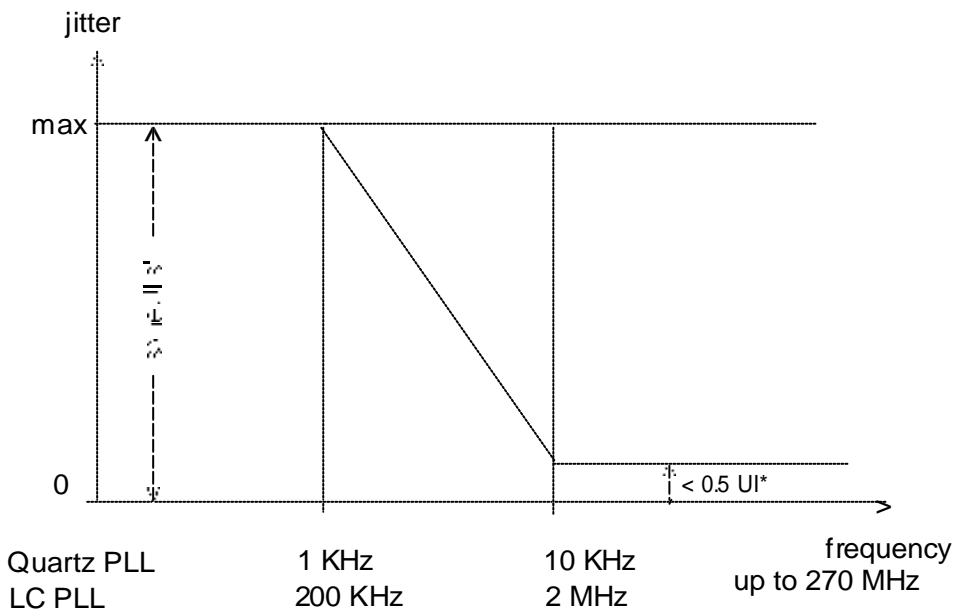
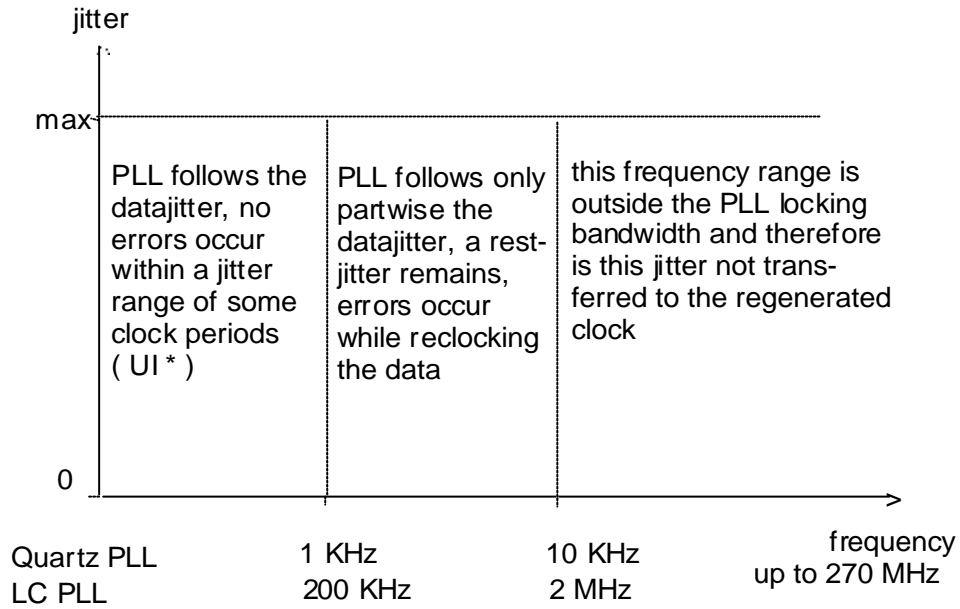
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SDI Check Pattern (serial digital interface)



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Jitter of a Serial Digital Interface Signal



* UI = Unit Interval (clock period), at 270 Mbit/s 1UI = 3.7 ns

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Technical Data for Option S.F - Z1

Standard	ITU-R BT. 601 / 656 (4:2:2) SMPTE 125M / 259 M
Systems	625 lines/50 Hz and 525 lines/60 Hz
Signals	according to ITU-R BT. 801 pathological signals for SDI all SAF/SFF signals
Parallel output	27 Msamples/sec
level	ECL level
rise/fall time (20/80%)	< 5 ns
clockpulse width	18.5 ns \pm 3ns
delay clock/data	18.5 ns \pm 3 ns
clock/data shifting	\pm 10 ns
connector	25 pin SUB D (ISO 2110 - 1980)
Serial output	270 Mbit / sec acc. D1 format
level	$V_{pp} = 800 \text{ mV} \pm 10\% @ 75 \Omega$
rise/fall time (20/80%)	0.75....1.5 ns
output impedance	75 Ω
return loss	$\geq 15 \text{ dB}$ within 10... 270 MHz
connector	BNC

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The SAF/SFF option "CCIR 601" has advanced possibilities:

- parallel and two serial outputs with 8 / 10 bit resolution and 27 Msamples / sec and 270 Mbit / sec
- the 10 th bit has additional funktion in all three components Y, Cb, Cr :
 - toggle bit for quantization noise measuring
 - settable to 0 or 1 for measuring the scaling factor mV / LSB
- adjustable rise / fall times of signaltransitions allow precise measurement of luma / chroma delay
- output and variation in amplitude, timing and phase of all SAF / SFF testsignals (testpatterns, ZONE PLATES, linearities...) including the self generated ones
- special ITU-R BT. 601 testsignals are
 - signals according to ITU-R BT. 801
 - all pathological signals
- no PC needed for changing the signals´
 - amplitude in Y, Cb, Cr independently from eachother
 - timing with the PHASE/TIME menu or using features of SIGNAL EDITSo you are able to test DSP machines (trick mixers, frame stores ...) also at the limits of the system.

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- the amplitude limits are
 - max. 254 dec / FE hex for 8 bit
1019 dec / 3FB hex for 10 bit
 - min. 1 dec / 01 hex for 8 bit
4 dec / 04 hex for 10 bit
- editing the H frequency allows changing the number of auxiliary data between EAV and SAV to check the synchronizing digital equipment.
- the onscreen comparison of the digital signal and the composite or component signal shows immediately defects and differences of the DSP
- the vertical blanking interval (VBI) is not influenced by the coding according to ITU-R BT. 601; the inserted VITS are part of the digital data. This is most useful for testing the influence of DSP in digital machines in the VBI.

Additional Information

Our Application Notes are regularly revised and updated. Check for any changes at <http://www.rohde-schwarz.com>.

Please send any comments or suggestions about this Application Note to:

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