Application Note

MIPI D-PHY: DEBUGGING AND COMPLIANCE TESTING

Products:

- R&S®RTO64
- R&S®RTO2000
- R&S®RTP064
- R&S®RT-ZS10
- R&S® RT-ZS60
- R&S®RT-ZD10
- R&S®RT-ZD40
- R&S®RT-ZM90
- R&S®RT-ZM130
- R&S®RTP-K27
- R&S®RTP-K136
- R&S®RTP-K140
- R&S®RTP-SIBNDL
- R&S®RTP-K134

Dhanshree Lade | 1SL410 | Version 0e | 12.2023

https://www.rohde-schwarz.com/appnote/1SL410

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1 Overview

MIPI D-PHY stands as a cost-effective, low-power physical layer interface, making it an ideal choice for mobile device architectures. It serves as a high-speed, source-synchronous interface utilized in various hardware systems: smartphone cameras and displays, smartwatch displays, drones, in-car entertainment and dashboard displays, automobile cameras, and radar sensors.

This application note aims to delve into the key features of MIPI D-PHY, its functionality, and best practices for testing D-PHY device compliance while addressing common issues. Additionally, it highlights Rohde & Schwarz's extensive range of equipment and automated test solutions, aiding users in ensuring compatibility and resolving common issues associated with the widely used MIPI D-PHY interface. Importantly, the MIPI D-PHY information in this application note aligns with the MIPI D-PHY specification version 2.5, with further details available at mipi.org.

2 MIPI D-PHY Features

The MIPI Alliance developed the D-PHY standards to meet the demand for a high-speed, low-power, and cost-effective solution in mobile devices and advanced technology systems. The D-PHY physical layer establishes a synchronous connection between the camera and display to a host processor using the Camera Serial Interface (CSI-2) or Display Serial Interface (DSI) protocols, respectively. D-PHY exhibits an asymmetrical design owing to the primary-secondary relationship between the two sides of the link, significantly reducing the complexity of the link. Some notable aspects of MIPI D-PHY include:

- A unidirectional clock, originating from the Primary and terminating at the Secondary. The clock is in quadrature phase with the data.
- The data signals can be either unidirectional or bi-directional.
- The reverse direction data rate in half-duplex operation is one-fourth of the forward direction data rate.
- There is point-to-point communication between the transmitter and receiver PHY environment.
- A MIPI D-PHY Link consists of a High-Speed (HS) signaling mode for fast data traffic and a Low-Power (LP) signaling mode for control purposes.
- The PHY can switch between the two modes depending on the application, i.e., to either transfer large amounts of data in HS mode or preserve battery life in the LP mode.
- In HS mode, MIPI D-PHY operates with differential signaling and a line impedance of a 100 Ω differential or 50 Ω single-ended
- In High-Speed mode, the transmission lines are AC coupled.
- In Low-Power mode, the data lanes of a MIPI D-PHY interface operate in a single-ended manner with high impedance termination.

Characterizing and debugging a flexible interface can pose challenges, often leading to a time-consuming process. To aid in overcoming these challenges, this application note offers an overview of critical features, techniques, and solutions from Rohde & Schwarz. These solutions empower users to verify the conformance of the D-PHY board with MIPI Alliance standards. Additionally, they offer decoding options for protocol validation purposes.

2.1 Operational modes of MIPI D-PHY

Over the years, MIPI DPHY as a standard has evolved and enhanced the possible features set. This document is based on MIPI D-PHY specification version 2.5 which supports the following operational modes:

1) High-Speed (HS) mode
2) Low-Power (LP) mode
3) Alternate Low-Power (ALP) mode

In this document, we will solely focus on the single-ended Low-Power (LP) signaling mode used for control purposes and the differential High-Speed (HS) signaling mode for fast data traffic.

In HS mode, data is transmitted in bursts to reduce the power consumption. Specifically, within each burst, an arbitrary number of payload data bytes are sent. The differential HS mode offers several advantages for High-Speed data transmission in mobile and embedded systems. These include efficient data transmission, improved signal integrity due to increased noise immunity, and better Electromagnetic Compatibility (EMC). Differential signaling helps prevent data degradation and allows for longer trace lengths without significant

signal loss. It is scalable and supports various data rates, thus making it suitable for a wide range of applications as the data rate can be adjusted as needed.

As per the MIPI D-PHY specification version 2.5, a maximum bit rate is not specified because it is determined by the performance of transmitter, receiver, and interconnect implementations. Instead, the D-PHY 2.5 specification outlines data ranges for which additional features, such as deskewing and equalization, need to be implemented – refer to Table 1.

Bit Rate Range	Supported Features
80 to 1500 Mbps per lane	Deskew calibration optional
Up to 2500 Mbps per lane	Deskew calibration mandatory
Up to 4500 Mbps per lane	Equalization mandatory

Table 1: Data rate dependent PHY requirements

The single-ended LP mode on the other hand, minimizes power consumption since the signals in LP mode are transmitted at a considerably lower frequency. LP mode aids in extending battery life in mobile devices and battery-powered applications, which is crucial for prolonged device usage. The maximum data rate in Low Power mode is 10 Mbps, utilized specifically for control purposes.

2.2 Understanding D-PHY LANE modules

The D-PHY configuration comprises a clock lane module and one to four data lane modules. The PHY utilizes two wires for the clock lane plus two wires per data lane, resulting in a minimum of four wires for the PHY's basic configuration. For a fixed clock frequency, the available data capacity of a PHY configuration can be increased by using more data lanes. The transmitter data lane connects to the receiver through D_p and D_n lines, while the clock connects through the Clk_p and Clk_n lines. D-PHY employs the D_p and D_n interconnect wires for both HS and LP modes. Within the PHY configuration, each lane module communicates using two lines with its counterpart. Additionally, the lane module incorporates control and interface logic (see Figure 1).

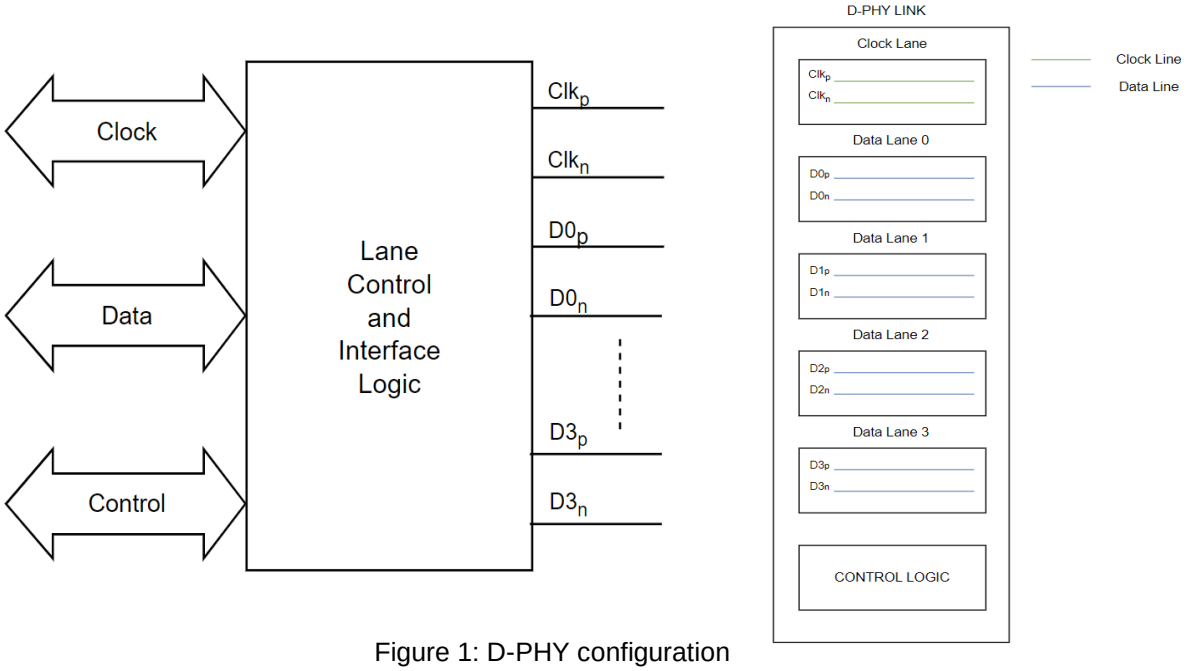

Figure 1: D-PHY configuration

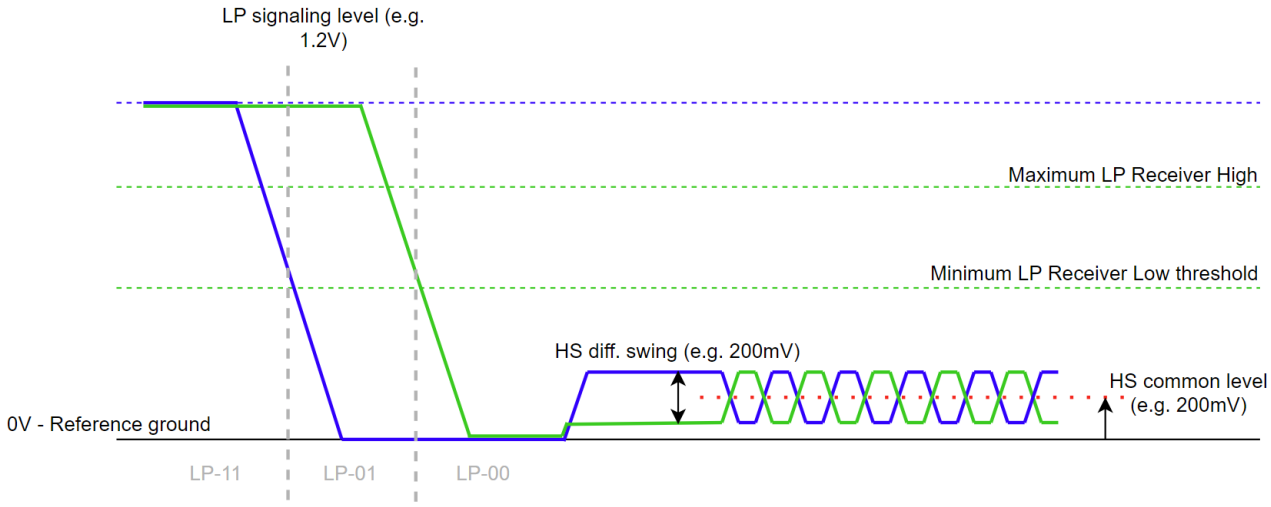

Figure 2: MIDI D-PHY signaling levels

The MIPI D-PHY data lane is driven by the transmitter in either High-Speed (HS) or Low-Power (LP) mode. In HS mode, the HS transmitter drives the lane differentially, resulting in two HS lane states: HS-0 and HS-1. The HS mode has a differential swing of 200 mV, as depicted in Figure 2. In LP mode, the two lanes are independently driven and single-ended, resulting in four LP lane states: LP-00, LP-01, LP-10, and LP-11. LP mode operates with a swing of 1.2 V. Low-Power signaling mode serves both Escape mode and Control mode. Additionally, there are several more states beyond these key ones, and the D-PHY link shifts from LP to HS (and vice versa) by traversing these states. Figure 2 illustrates the MIPI D-PHY signaling levels and the LP state sequence followed by the PHY before entering the HS state.

In LP mode, a clock signal can be reconstructed by exclusive ORing (X-ORing) the D_p and D_n lines. This technique proves particularly useful during data transmission in LP mode as it facilitates self-clocking without requiring a dedicated clock lane (CLK), resulting in even greater energy savings. Within LP mode, Escape mode represents a special operational mode offering additional functionality. In this mode, the PHY employs Spaced-One-Hot bit encoding for asynchronous communication, independent of the Clock Lane.

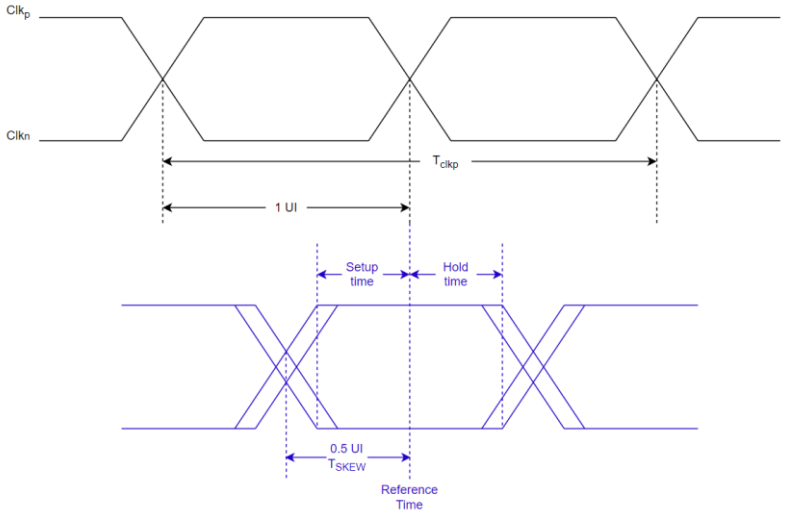

Figure 3: Data to Clock timing relation

In HS mode, a dedicated clock signal plays a crucial role in synchronizing data transmission and reception between the transmitter and receiver. Specifically, within the differential HS mode, a dedicated clock lane carries a low-swing, differential Double Data Rate (half-rate) clock signal from Primary to Secondary. Notably, the unidirectional clock lane signal is in quadrature phase with respect to a toggling bit sequence on a Data Lane in the forward direction, and a rising edge appears in the center of the first transmitted bit of a burst, as illustrated in Figure 3. The setup time illustrated in the figure represents the minimum time the data must be present before a rising or falling clock edge. The hold time is the minimum time that data shall remain in its current state after a rising or a falling clock edge. These hold and setup times are important parameters for ensuring proper timing and data integrity in MIPI D_PHY systems. The specifications provide guidelines for their measurement and verification.

2.3 Communication between transmitter and receiver

Let's assume that image data needs to be transmitted. The MIPI D-PHY transmitter utilizes the data lanes to transmit the image data. Depending on the count of data lanes, the transmitter parallelizes the data across these lanes before transmitting it to the receiver. For example, with four data lanes in use, the initial byte of payload data goes through data lane 0, the second byte through data lane 1, the third via lane 2, and the fourth across lane 3. Upon reception, these parallelized data bits are serialized and converted back into their original byte format.

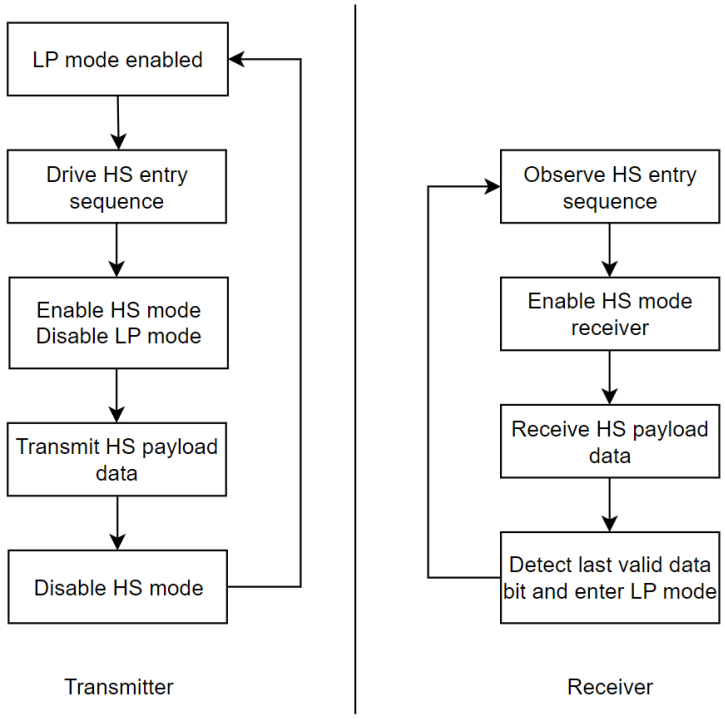

Figure 4: Transmitter and Receiver State Diagram for High Speed Data Transmission

The data lane switches continually between LP and HS modes during data transmission through the PHYs. To enter HS mode, the sequence LP-11, LP-01, LP-00 must be transmitted, as shown in Figure 2. Once in HS mode, the data lane remains in that mode until an LP-11 signal is received. Before each HS burst, the transmitter sends a sync sequence of '00011101'. The receiver D-PHY recognizes the Leader sequence ‘011101’ and synchronizes accordingly. Subsequently, the HS transmitter continues transmitting High-Speed payload data, and the HS receiver continues to receive data until encountering the LP-11 state, which returns

the data lane to LP mode. At a minimum, a payload data unit consists of one byte. As shown in Figure 4, the state diagram for a D-PHY transmitter and receiver illustrates this behavior.

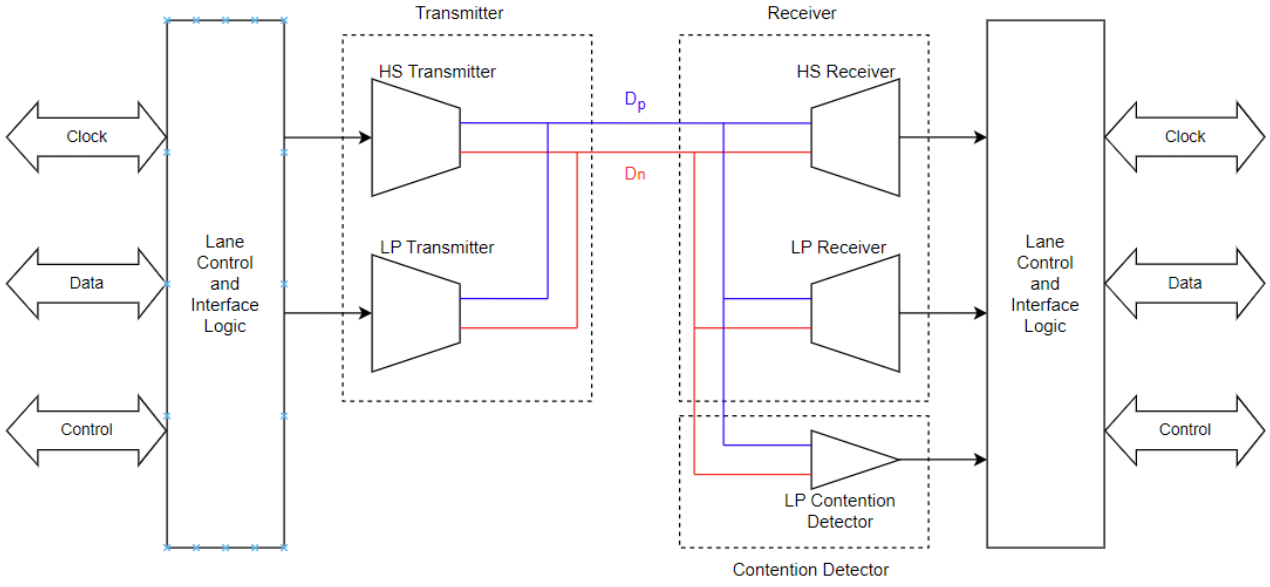

Figure 5: Communication between two PHYs

Figure 5 illustrates the abstract architectural connection between two PHYs for data communication. During data transmission, a High-Speed (HS) transmitter is used, while a HS receiver is employed for reception. If the HS feature is disengaged within the lane module, the PHY enters a high-impedance condition. Activation of the LP transmitter occurs through driving Low-Power states. When the LP receiver is activated in a lane module, it remains active and continuously monitors line levels. A LP contention detector becomes necessary for bi-directional operation, as it detects contention situations while the LP transmitter drives Low-Power states.

3 Testing challenges and best practices

This section illustrates the device measurement setup and discusses potential challenges encountered during testing. Several test setups are feasible, depending on your environment. The setups might significantly vary depending on whether you're a PHY developer or a system integrator. Here are two generic setups presented: first, the setup for characterizing a PHY using a reference setup, and second, a chip-to-chip interface representing a typical everyday scenario. Figure 6 depicts both types of setups available.

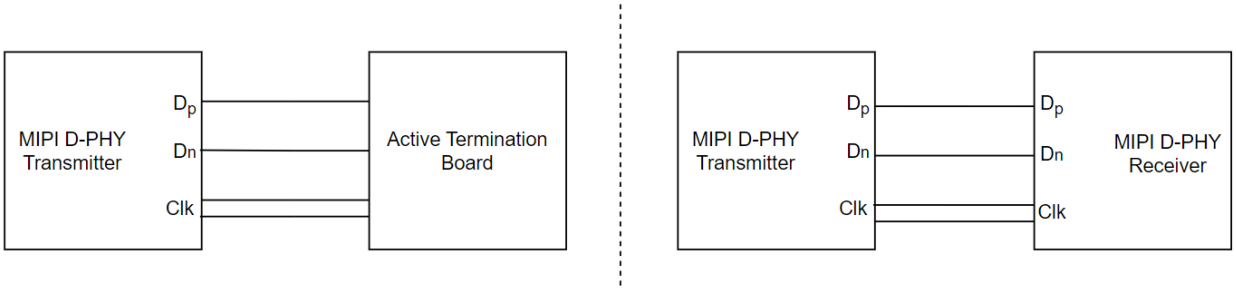

Figure 6: Device measurement setup

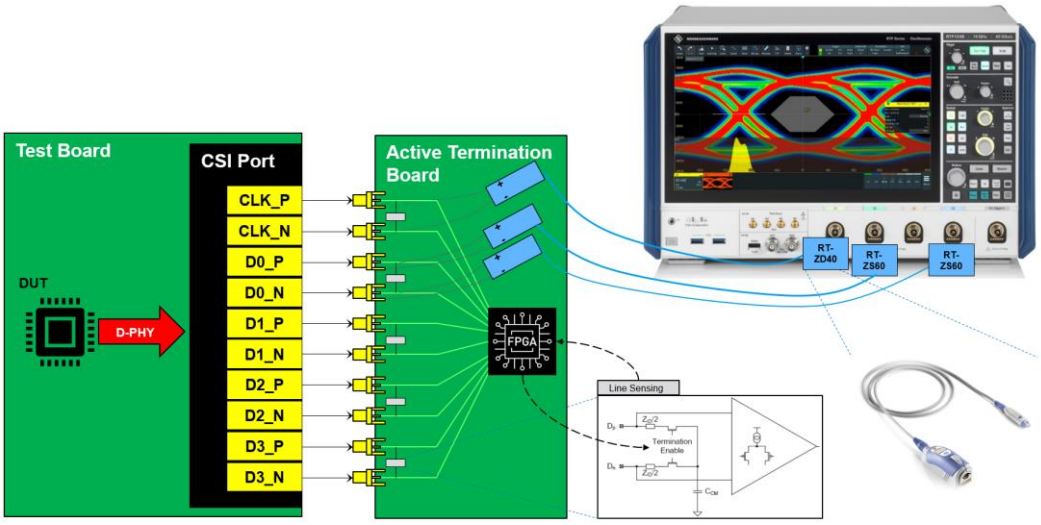

Figure 7: Rohde & Schwarz test setup

Figure 7 displays the Rohde & Schwarz test setup, incorporating a D-PHY Transmitter alongside a termination board. This board serves the purpose of meeting the impedance requirements, maintaining a high impedance in LP mode, and adhering to 100Ω (differential)/50Ω (single-ended) in HS mode.

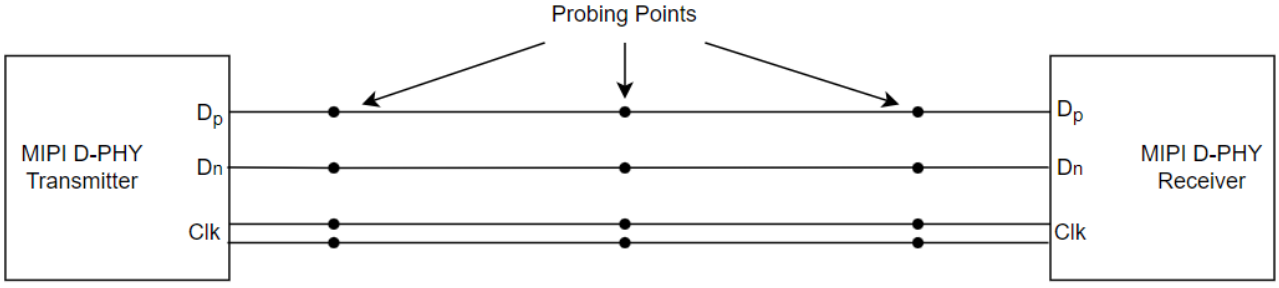

Figure 8: Probing points

In addition to the test setup, the probing points play a crucial role in achieving accurate measurements, particularly when testing High-Speed digital interface technologies like D-PHY. The data rates in the HS mode can vary depending on the D-PHY module, and deskew analysis and equalization might be necessary, as outlined in Table 1. When the PHY operates above 1.5 Gbps or transitions to any rate above 1.5 Gbps, an initial deskew sequence is transmitted before normal High-Speed data transmission. Skew in the MIPI D-PHY transmitter can stem from various factors, including mismatches in the delay of the data and clock signals, variations in signal path lengths on the printed circuit board (PCB), fluctuations in the PCB material's dielectric constant, and differences in the rise and fall times of the signals. To ensure reliable and precise results, careful selection of testing points is essential to meet the signal integrity requirements (refer to Figure 8).

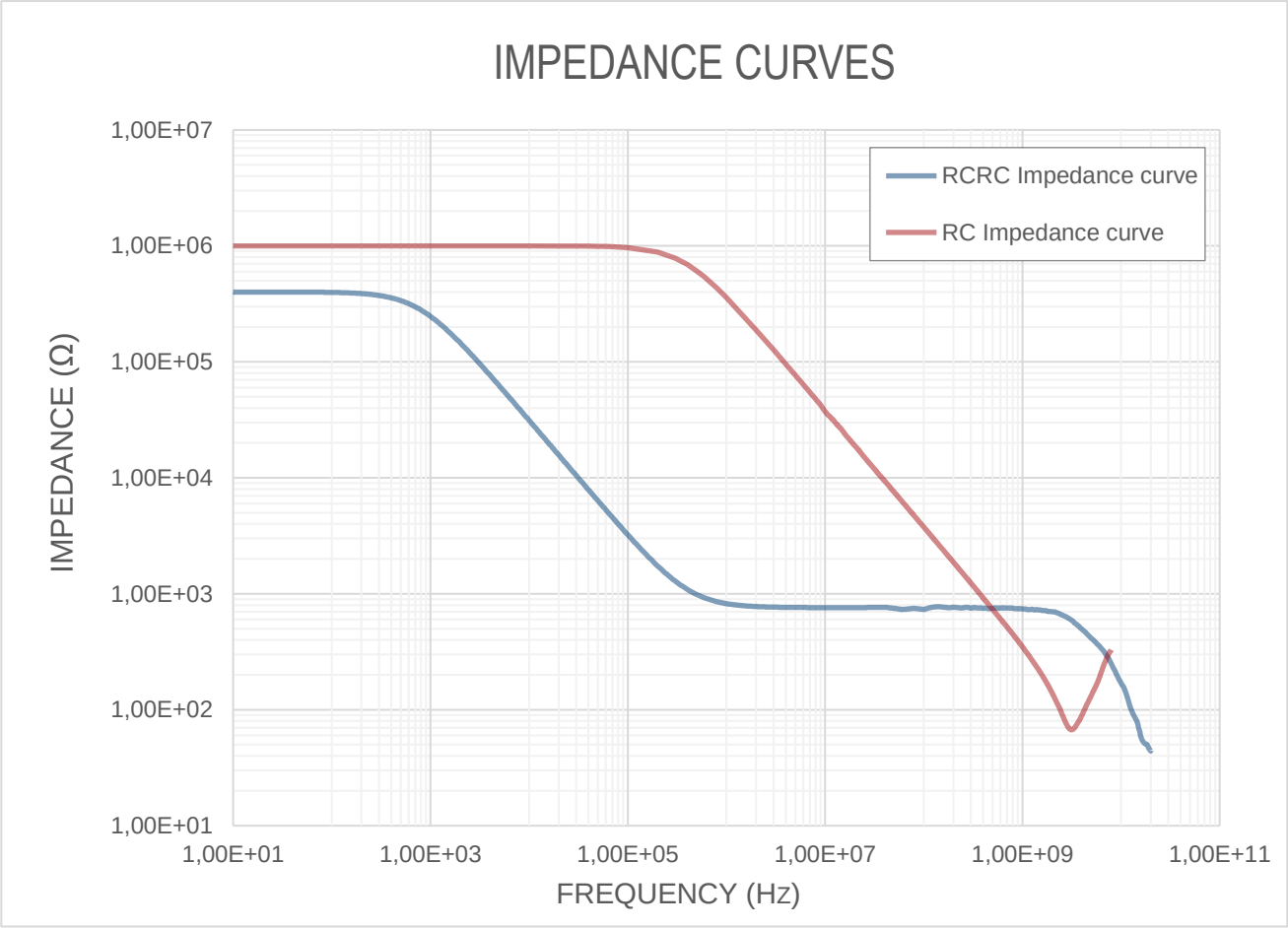

Figure 9: Impedance Profile of RC vs. RCRC Probe

MIPI D-PHY switches between high impedance and 100Ω (differential) / 50Ω (single ended) termination. This behavior necessitates careful consideration when selecting the appropriate probe for measurement tasks. Another crucial consideration for probe choice in MIPI D-PHY testing is the probe's impedance profile, which should align with the interface's impedance requirements. An RC impedance profile in a probe maintains consistent high impedance across frequencies, reducing loading and signal distortion. Conversely, an RCRC profile offers higher impedance at low and high frequencies but lower mid-band impedance, depicted in Figure 9 (using the RT-ZD probe for the RC curve and the RT-ZM probe for the RCRC curve).

Notably, D-PHY operates at varying speeds, transitioning between the 100Ω impedance (AC coupled to ground) HS mode and the unspecified high impedance LP mode per specification version 2.5 in Table 33. The bus impedance in D-PHY is manipulated by pulling it up or down with a high-value resistor, resulting in extended time constants and noticeable signal amplitude changes. This introduces loading that can cause amplitude distortions in RCRC probes, unlike RC probes. The subsequent section will detail instrument and probe selection based on the operating mode and data rate.

3.1 Instrument selection

Rohde & Schwarz provides an extensive range of instruments catering to diverse testing applications. To identify the suitable instrument and probe combination, the initial step involves determining the bandwidth requirement. A useful guideline is to ensure that the scope and probe bandwidth are at least three times the clock frequency or half the data rate of the system under test; ideally, a recommendation of five times the system bandwidth is preferred. When testing MIPI D-PHY interfaces, the selection of instrument and probe is contingent upon the operational mode and data rate.

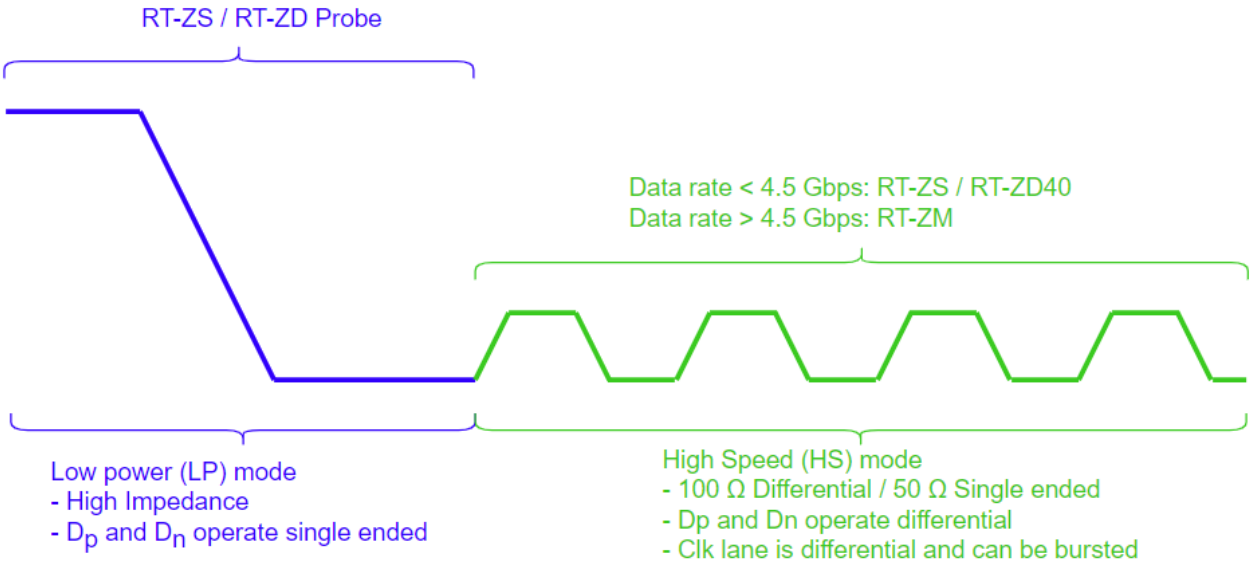

Figure 10: Probe Selection

Figure 10 depicts a representation of a MIPI D-PHY signal, aiding in understanding the optimal R&S probes for PHY testing. LP analysis can be conducted using the cost-effective RT-ZS Probes, while HS analysis benefits from the versatile RT-ZM Probes, providing the highest probe head flexibility. Depending on the operating data rate, the following probes can be utilized:

1) HS mode data rate < 4.5 Gbps:

   For testing in LP and HS modes, it's recommended to utilize two RT-ZS60 probes and one RT-ZD40 probe. The RT-ZS60 is a single-ended active voltage probe designed with high input impedance. Optimized for single-ended measurements in environments characterized by 50 Ω impedance, it excels in ground-referenced voltage measurements from DC to 6 GHz, providing accuracy for LP mode measurements. On the other hand, the RT-ZD40 probe is specifically used for the D-PHY clock and HS mode. This differential probe is capable of measuring differential voltage from DC to 4.5 GHz, catering to the requirements of HS mode within the D-PHY setup.

2) HS mode data rate > 4.5 Gbps:

   It's recommended to use two RT-ZS10 probes and one RT-ZD probe. Subsequently, depending on the speed grade required for HS testing, one can opt for either three RT-ZM90 modular probes or two RT-ZM90 probes alongside one RT-ZM130 probe.

According to previous discussion following configurations are recommended:

	Model	Quantity	Description
HARDWARE			
Data Rate < 4.5 Gbps			
Oscilloscope	RTO64 / RTO2000	1	Bandwidth: 600 MHz to 6 GHz
Probes	RT-ZS60	2	Up to 6 GHz (LP mode)
	RT-ZD40	1	Up to 4.5 GHz, differential probe (HS mode and clock)
Data rate > 4.5 Gbps			
Oscilloscope	RTP	1	4GHz to 16 GHz
Probes	RT-ZS10	2	Up to 1 GHz (LP mode)
	RT-ZD10	1	Up to 1 GHz, differential probe
Choice 1	RT-ZM90	3	9 GHz modular probe (HS mode)
Choice 2	RT-ZM90	2	9 GHz modular probe (HS mode)
	RT-ZM130	1	13 GHz modular probe (HS mode)
SOFTWARE			
Compliance	RTP-K27	1	MIPI D-PHY 2.1/2.5 compliance test suite
Debugging	RTP-K136	1	8 Gbps Advanced Eye analysis option (for lock delta UI, Clock Jitter)
	RTP-K140	1	8 Gbps Serial Pattern Trigger (for Clock and Data Eye)
Optional	RTP-SIBNDL	1	Signal Integrity Bundle (incl. Deembedding, 16 Gbps serial pattern trigger with HW-CDR, etc.)
	RTP-K134	1	Jitter & Noise decomposition option
External test Fixtures (not from R&S)			
Optional When using Chip-2-Chip Interface	UNH-IOL-DPHY-RTB	1	Active Termination Board (order from https://license.unh.edu/products/iol/mipitestfixtures)
	CLOAD	1	MIPI D-PHY Capacitive Load Fixture

Table 2: List of hardware and software

3.2 Rohde & Schwarz Scope Suite

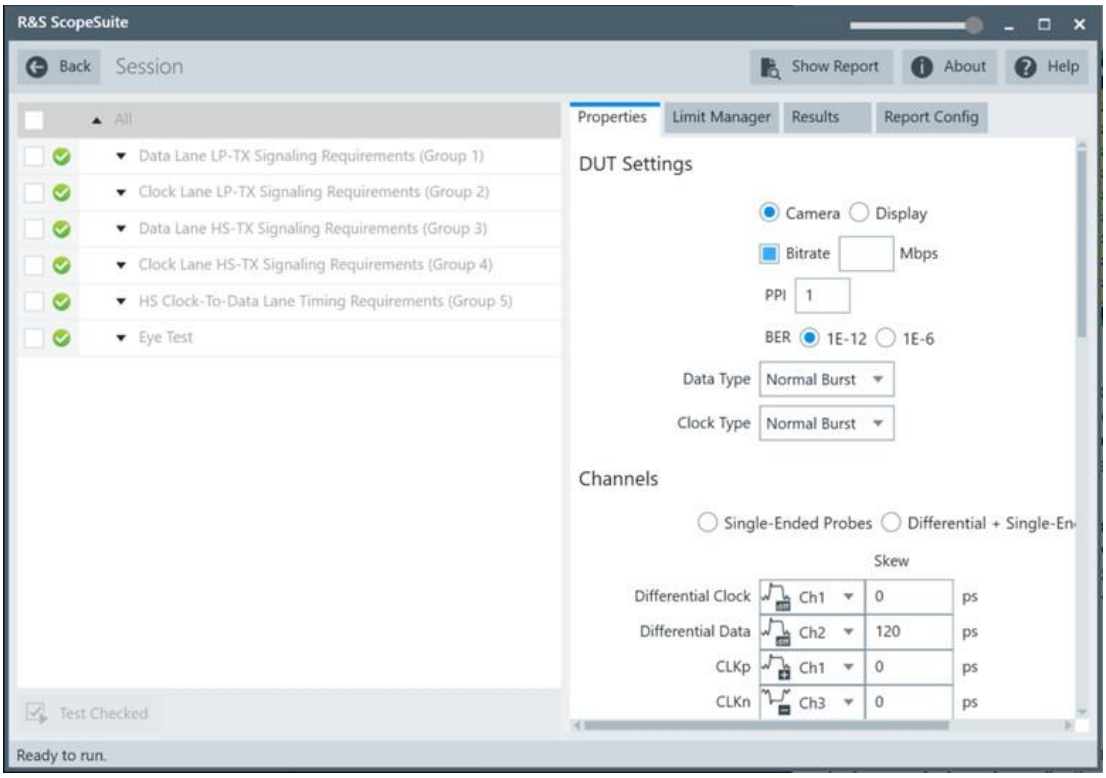

Figure 11: Rohde & Schwarz scope suite for MIPI D-PHY

The Rohde & Schwarz Scope Suite encompasses all the conformance test groups outlined by the MIPI Alliance. Illustrated in Figure 11, the suite covers tests for the transmitter across various modes, encompassing data lane and clock lane tests, along with timing requirements and eye diagram assessments. This suite supports versions v1.1, v1.2, v2.0, v2.1, and v2.5 of the MIPI standard.

Notably, LP mode tests within the suite assume the implementation of Ultra-Low Power Sequence (ULPS) in the Device Under Test (DUT). In cases where ULPS isn't implemented, configurable test patterns should be employed to operate the DUT solely at logical "1" and "0" levels within the LP sense (typically 1.2V and 0V, respectively).

3.3 MIPI D-PHY SIGNAL view and EYE diagram

Assisted by edge triggering, it becomes remarkably straightforward to observe the MIPI D-PHY transmitter waveforms and distinctly discern the transitions between LP and HS modes, and vice versa, using the Rohde & Schwarz oscilloscope. Illustrated in Figure 12, this feature facilitates a clear view of the transmitted signal, enabling a detailed examination of the PHY's behavior across various operating modes.

Figure 12: MIPI D-PHY waveforms display on oscilloscope

The HS entry mode sequence, briefly discussed in section 2.3 of this paper, can be readily explored using the zoom-in feature provided by Rohde & Schwarz oscilloscopes. This functionality permits a more detailed examination of the HS start sequence utilized by the MIPI D-PHY transmitter, showcased in Figure 13. By utilizing this feature, engineers can acquire valuable insights into the precise timing and protocol dynamics of the MIPI D-PHY interface.

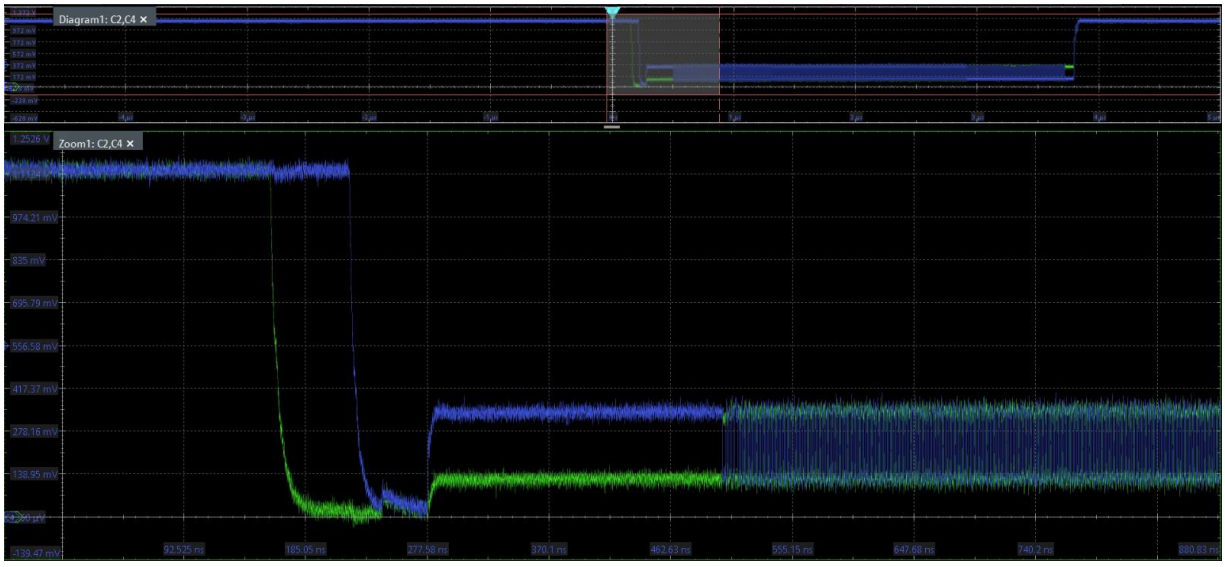

Figure 13: HS start sequence

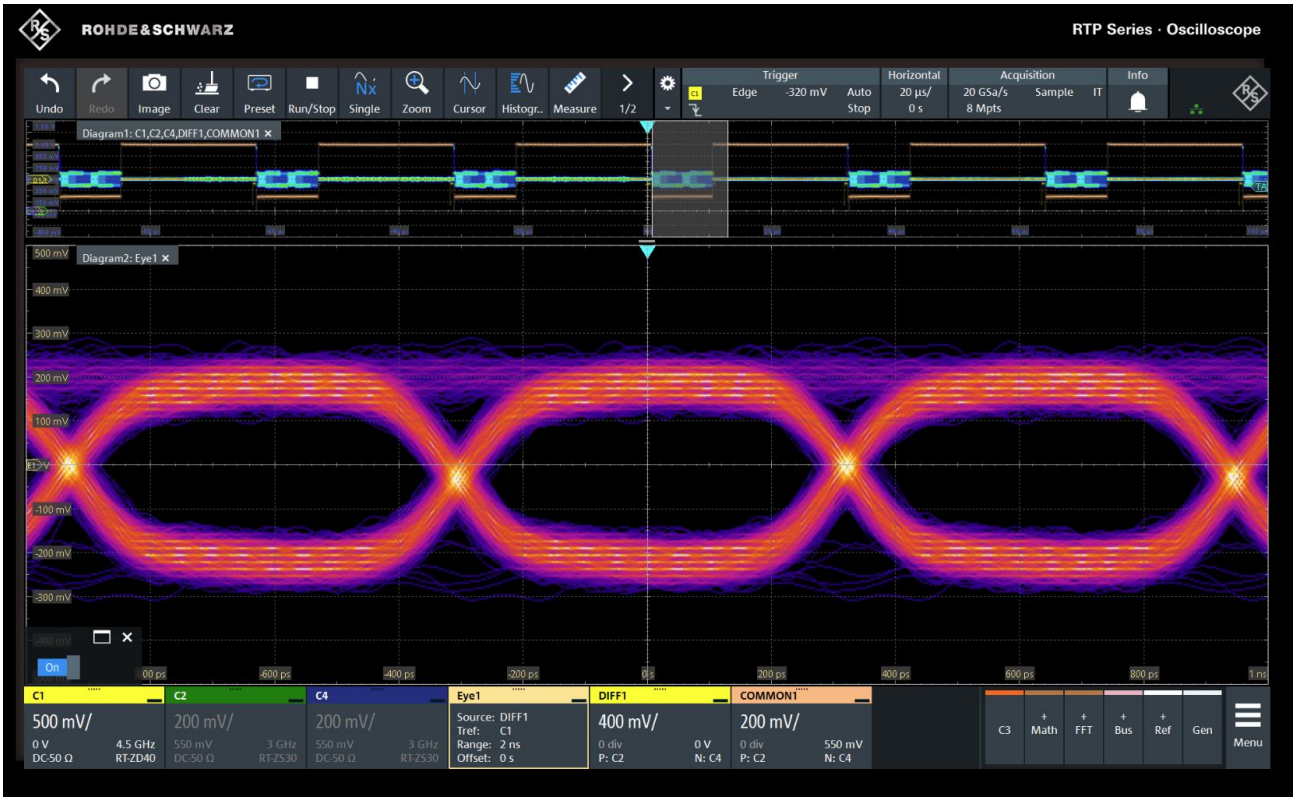

Figure 14: MIPI D-PHY Eye Diagram

Figure 14 displays the eye diagram obtained through edge triggering, showcasing the PHY's operation in burst mode, seamlessly transitioning between low power (LP) and high-speed (HS) modes. To attain a clear eye diagram, Rohde & Schwarz oscilloscopes offer a gating function within the advanced eye option, enabling the capture of a specific portion of the waveform.

3.4 Decoding options

Decoding the signals transmitted by the MIPI D-PHY can prove beneficial in specific situations, contingent upon use cases and requirements. Signal decoding aids in identifying issues like data transmission errors, signal integrity problems, protocol development, compliance testing, and more. R&S offers two decoding options, as follows:

- R&S RTP-K26 for D-PHY v1.1 and v1.2
- R&S RTP-K27 for D-PHY v2.1 and v2.5

To access the decoder option, navigate to the menu, select "Apps," then "Protocol," and finally choose the "D-PHY" option. Please note that for this feature to work properly, the PHY must be probed single-ended, meaning only the $D0_p$ and ground pins for the data lane and Clk_p and ground pins for the clock lane should be connected.

Figure 15 displays a snapshot of the R&S scope presenting the decode function. Multiple physical configurations are available, allowing users to customize the number of data lanes based on their specific needs. Additionally, the decode layer and data format can be selected in the display options. Furthermore, the R&S Scope Suite offers abundant triggering options, as demonstrated in Figure 15, where the transmitted data is triggered based on a user-defined payload value (0x33). This versatility ensures optimal testing and analysis of MIPI D-PHY signals.

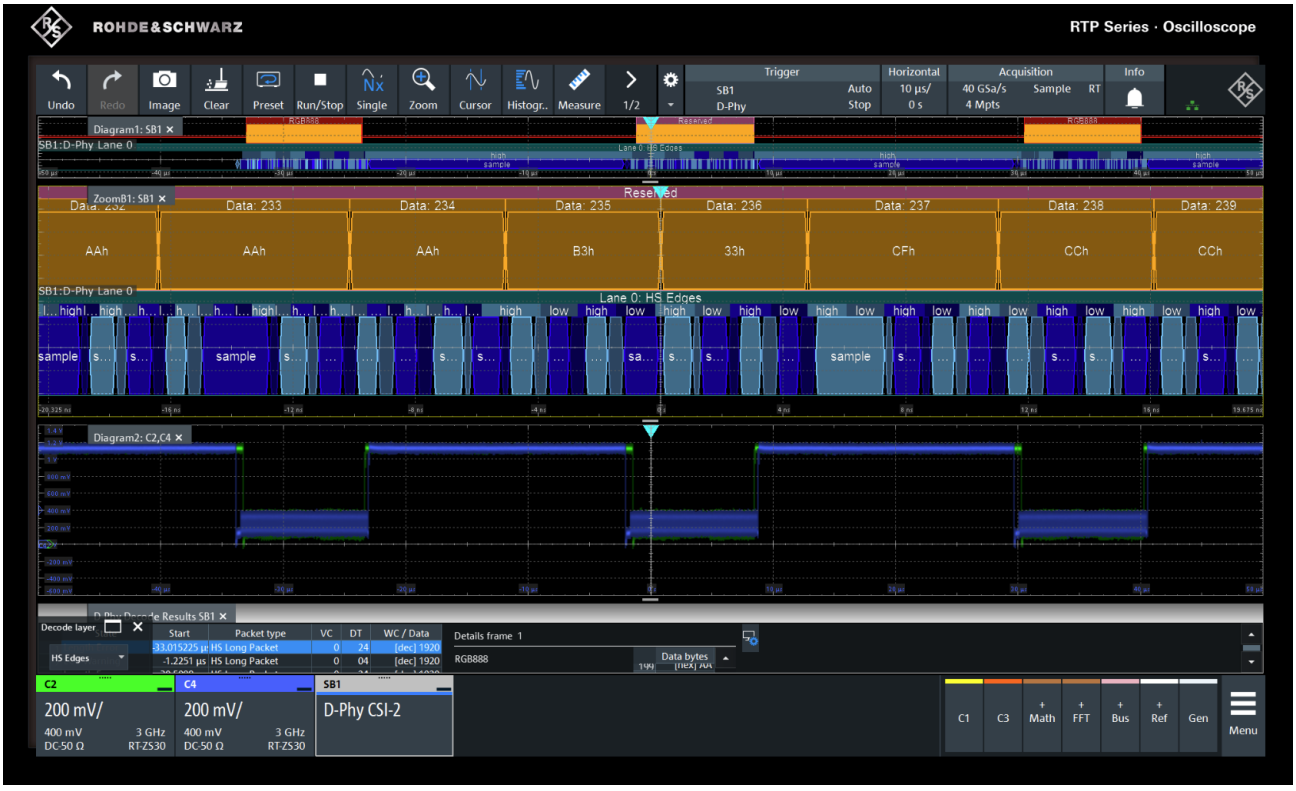

Figure 15: MIPI D-PHY trigger decode

4 Conclusion

The MIPI Alliance D-PHY standards provide standardized camera and display interfaces, along with communication using CSI-2 and DSI protocols. With distinct specifications such as continuous switching between high impedance single-ended low power mode and differential high-speed mode (with an impedance of 100 Ω AC-coupled to ground), the D-PHY standard offers a range of benefits, including increased bandwidth and reduced power consumption. Depending on the number of data lanes used (up to four), the available bandwidth can vary, necessitating thorough testing and verification of these systems. Fortunately, Rohde & Schwarz offers a comprehensive oscilloscope portfolio with R&S RTP and RTO models, which, with additional software licenses, can support Trigger and Decode functionality, as well as compliance analysis and debugging of MIPI D-PHY busses.

5 Ordering information

Designation	Type	Order No.
Oscilloscope 4 channels, 6 GHz BW	R&S®RTO64	1802.0001.04
Oscilloscope 4 channels, 600 MHz BW	R&S®RTO2000	1329.7002.04
Oscilloscope 4 channels 6 GHz BW	R&S® RTP064B	1803.7000.06
Active single ended voltage probe, 1GHz BW	R&S®RT-ZS10	1410.4080.02
Active single ended voltage probe, 6GHz BW	R&S®RT-ZS60	1418.7307.02
Active differential voltage probe, 1GHz BW	R&S®RT-ZD10	1410.4715.02
Active differential voltage probe 4.5 GHz BW	R&S® RT-ZD40	1410.5205.02
Modular probe amplifier, differential 9.0 GHz BW	R&S®RT-ZM90	1419.3205.02
Modular probe amplifier, differential 13.0 GHz BW	R&S® RT-ZM130	1800.4500.02
Software option for MIPI D-PHY V1.1 and V1.2	R&S®RT-K27	1803.6584.02
Software option for noise and jitter decompensation	R&S®RTP-K134	1800.6977.02
Software option for Advanced Eye Diagram analysis 8Gbps	R&S®RTP-K136	1803.6561.02
Software option for High Speed Serial Trigger pattern	R&S®RTP-K140	1326.4560.02

Rohde & Schwarz

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Application Note | MIPI D-PHY: Debugging and compliance testing
Data without tolerance limits is not binding | Subject to change

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