Application Note

VERIFICATION METHODS OF SNUBBER CIRCUITS IN FLYBACK CONVERTERS

Products:

- R&S®RTA4004
- R&S®RT-ZHD07
- R&S®RT-ZD10
- R&S®RT-ZC20B
- R&S®RTO2064
- R&S®NGL202
- R&S®HM8118 LCR Bridge

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1 Overview

In general, most of the existing electronic devices are connected to the AC mains and require a power conversion stage to convert the AC-Voltage to a smaller DC-Voltage. Voltages and frequencies of the power grid differ between different regions. However, different types of AC-DC conversion stages exist to supply the electronic equipment with adequate DC-power.

In AC-DC conversion combined with power levels less than 50W, the flyback converter is a commonplace chosen topology because of its simplicity and its low cost. The majority of consumer products make use of this converter type like wall brick power supplies or power adapters for any consumer application and other type of stand-by auxiliary power supply like used in white and brown goods. In AC to DC converter application, an electrical isolation between input and output is mandatory. The flyback topology provides this galvanic barrier.

Beside the common advantages of a flyback converter, it has inherently parasitic components, which typically produce ringing waveforms with considerably high voltage spikes. Without suppressing this unwanted ringing, it may have some negative effect on other components like the switching elements. This ringing can also influence the EMI emissions adversely. Therefore, it is an important task to adequate suppress and damp the ringing effect. This damping circuit is known as snubber circuit and provides this functionality. In the flyback converter, different snubber structures can be applied and each of the structure has its advantage and disadvantage.

The demand having a snubber circuit in the power supply topology leads to specific verification methods during the design to obtain a proper and reliable design. These verification methods are the main focus of the discussions within this document.

2 Isolated Flyback Converter

The flyback converter is based on the buck-boost principle and provides in addition an isolation between input and output terminals. Furthermore, this topology can be utilized as active power factor correction circuit to enhance the power factor required in specific applications. Furthermore, it is popular because of its ability to provide multiple outputs with one key element, the transformer.

2.1 Working Principle

The flyback converter and its main components is arranged in a structure shown in Figure 1. The flyback converter is constructed by using a transformer or coupled inductor, a switch which is typically a MOSFET, a rectifier diode on the secondary side and a capacitor at the input and output. In applications where AC-Power is used, an additional rectifier connected to a bulk capacitor is placed in front of the flyback converter's input to convert the AC-Voltage to a rectified pulsating DC-Voltage.

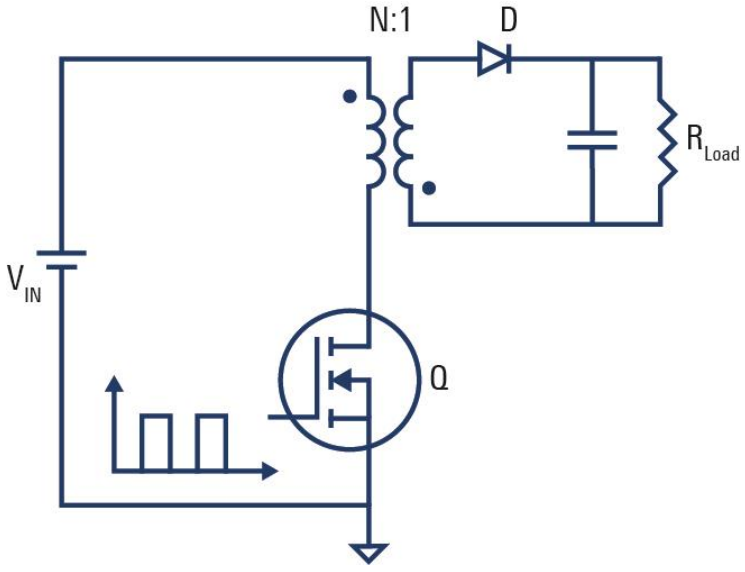

Figure 1 Flyback Structure

The main switch is controlled by a PWM signal and thereby energy is transferred from the primary to the secondary by means of the magnetic field of the transformer. During the normal operation, the main switch conducts during the on-time (t_{on}). During the on-time, the primary current flows from the input source to the primary ground while the energy is stored within the magnetizing inductance. At the same time, the secondary current flow is blocked due to the opposite winding polarity of the secondary winding and by means of the secondary rectifier diode. During off-time (t_{off}), the stored energy in the magnetizing inductance is transferred to the secondary side through the output rectifier diode into the capacitor and to the load. The primary to secondary turns ratio of the transformer influences the ratio between input and output voltage. Therefore, the output voltage is reflected to the primary winding during the off-time and is defined by the turn's ratio $n = N_p/N_s$. As a consequence, the maximum voltage at the switch node to ground is the input voltage plus the reflected voltage (sometimes also called flyback voltage).

2.1.1 Discontinuous Conduction Mode (DCM)

In case that the current flowing in the secondary circuit reaches zero during the off-time, there is no energy left to transfer to the output. This third period after on-time and off-time represents a non-conducting time of the converter and is also called dead-time (t_{dt}). During this time, the load is supplied only by the output capacitor. This operation mode of the converter is called Discontinues Conduction Mode (DCM). The primary current, secondary current and the voltage across the primary switch device are illustrated in Figure 2.

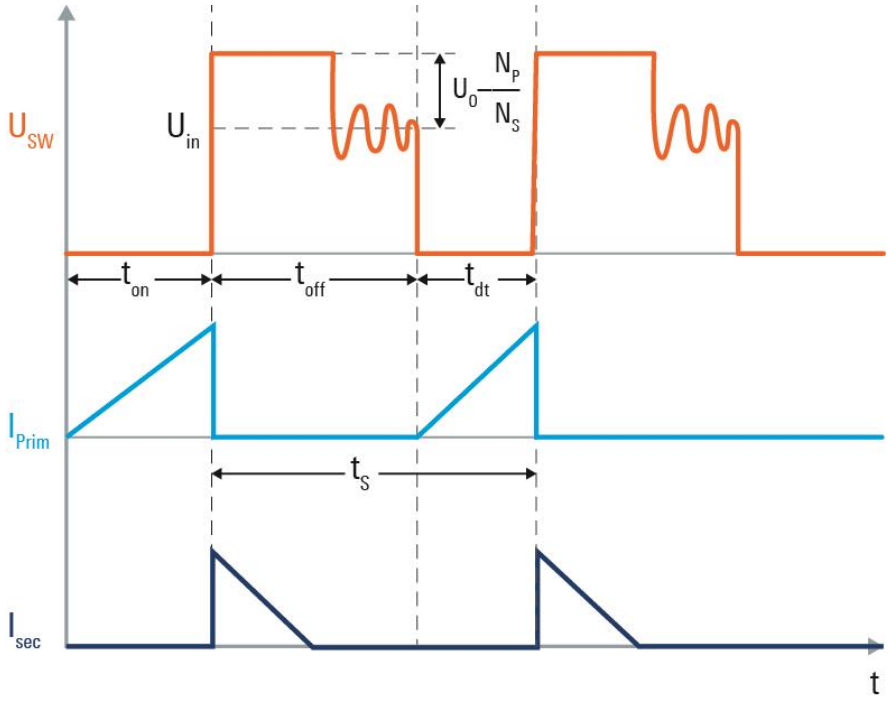

Figure 2 Flyback DCM Waveform

After the secondary current reaches zero, the impedance of the inductor on the primary side changes and therefore oscillation appears in the voltage waveform of the switch node. This oscillation is caused by a resonant circuit, which is created by the magnetizing inductance and the parasitic output capacitance of the main switch device. These parasitic components and their effects will be discussed in more detail in the next chapter.

2.1.2 Converter Operation Modes

Beside the DCM described in the previous chapter, two other operation modes exist which are the Critical Conduction Mode (CRM) and the Continuous Conduction Mode (CCM). In the literature, the Critical Conduction Mode is also called Transition Mode or Boundary Conduction Mode.

► Continuous Conduction Mode Definition

The main switch is switched on during the ramp down cycle, before the current flowing through the secondary winding reaches zero.

► Critical Conduction Mode

If the current through the secondary coil reaches zero and the switch turns ON immediately (no dead-time; $t_{dt} = 0$), the converter operates in BCM. In this case, the converter operates at the boundary between Continuous Conduction Mode and Discontinuous Conduction Mode.

2.2 Parasitic components and their effects

As described previously, the transformer and all other components were considered more or less ideal for simplicity, which is not true in reality. The transformer also consists of parasitic components like the leakage inductance L_{Lk} and the primary winding capacitance C_{Prim}. For the switching element, typically a MOSFET is used. This element has an inherent output capacitance C_{OSS} between drain and source terminal. The output capacitance of the MOSFET in combination with the leakage inductance and the winding capacitance have remarkable impact on the performance of the converter. The basic flyback structure including their major parasitic components is illustrated in Figure 3.

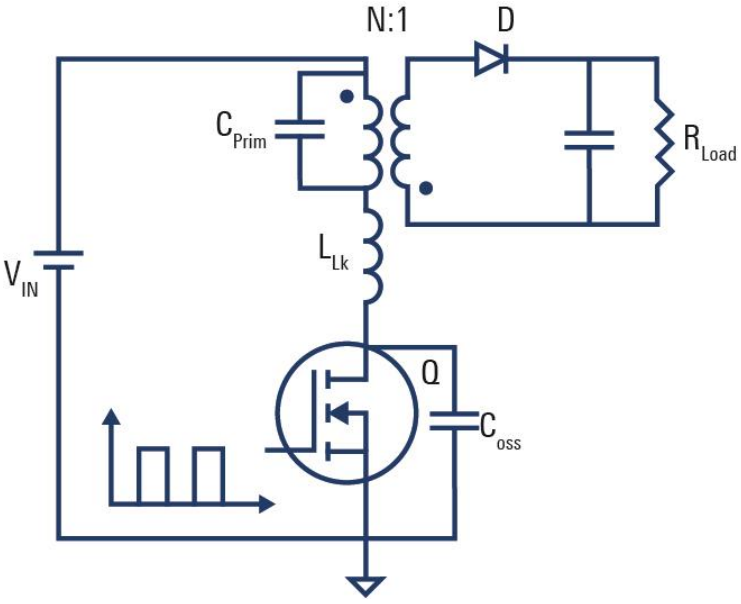

Figure 3 Flyback Structure with Parasitic Components

The primary leakage inductance L_{Lk} in a flyback converter does not participate in the primary to secondary energy transfer like the magnetizing inductance L_M. This energy is lost and generates a voltage spike at the beginning of the turn-off time at the drain terminal of the MOSFET switching element. The leakage inductance and winding capacitance in the transformer, the peak current magnitude and the output capacitance of the switch determine the magnitude of this voltage spike. Furthermore, the voltage spike also delays the transfer of power from the primary to the secondary side, which limits the maximum switching frequency of the converter.

The primary leakage inductance, the primary winding capacitance and the output capacitance of the MOSFET form a parasitic LC network. The peak voltage at the switch node is given by:

$$V_{Peak} = I_{Peak} * \sqrt{\frac{L_{Lk}}{C_{Prim}+C_{Coss}}} + V_{In} + V_{Flyback} \quad (1)$$

Where the flyback voltage is given by the turn's ratio and output voltage:

$$V_{Flyback} = V_{out} * \frac{N_{Primary}}{N_{Secondary}} \quad (2)$$

Of course, the described parasitic components change the voltage waveform at the switch node accordingly. The influence of the parasitic components is illustrated in the Figure 4.

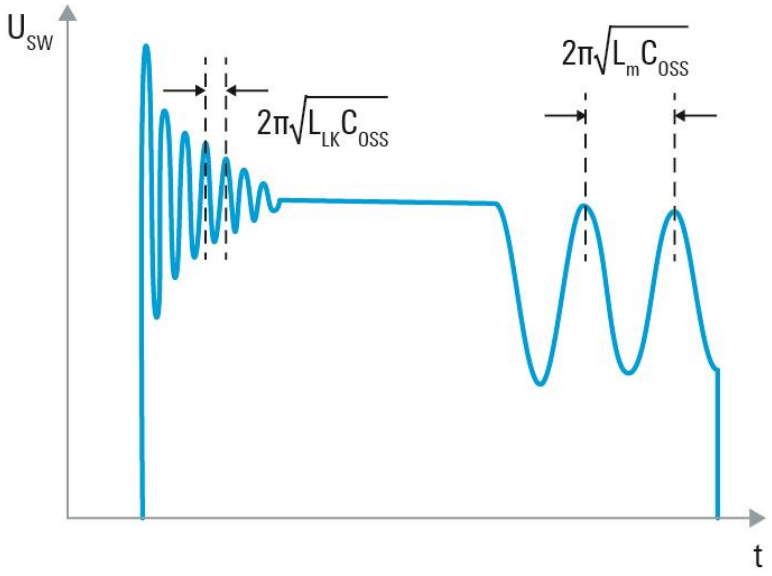

Figure 4 Switch Node Voltage Waveform

The high voltage spike caused by the leakage inductance L_{LK} and the output capacitance of the switch C_{OSS} right after switch-off of the switch is clearly visible. Unfortunately, the damping effect is not very effective in this resonance circuit and the oscillation typically in the frequency range of several MHz last for several periods which also may degrade the EMI performance.

The second resonance, which occurs after the energy transfer to the output has finished, is determined by the magnetizing inductance L_M and the output capacitance of the switch C_{OSS} and therefore the frequency is much lower. Sometimes, the flyback controller operate in way to detect the valley before the MOSFET will switch on again. This can decrease the switching losses of the MOSFET and thus increase the overall converter efficiency.

However, if the high voltage spike created by the switch-off mechanism is not properly clamped or damped, the maximum breakdown voltage of the MOSFET may be exceeded and the MOSFET will be destroyed. In some cases, the MOSFET will operate in the avalanche mode where the energy is dissipated into heat. Avalanche condition occurs when a voltage spike exceeds the device's breakdown voltage. Some semiconductor devices are designed to withstand a certain amount of avalanche energy for a limited time and can, therefore, be avalanche rated. Others will fail very quickly after operating in avalanche mode. This has to be considered when a suitable MOSFET is selected.

2.3 Suppressing voltage spikes

As described earlier, the maximum voltage across the main switch is the sum of the input voltage, the reflected or flyback voltage and the oscillation caused by the leakage inductance. While the switching device has to be selected to withstand the input voltage plus the flyback voltage, a snubber is typically required to clamp or damp the oscillation and convert the leakage energy into heat.

Snubbers are circuits which are placed across semiconductor devices or transformers for protection purpose and to improve performance. Snubbers can reduce or even eliminate voltage or current spikes, limit dI/dt or dV/dt and can reduce EMI by damping the voltage and current ringing. There are many different kinds of snubbers, but the two most common ones are the resistor-capacitor (RC) damping network and the resistor-capacitor-diode (RCD) turn-off snubber circuit.

However, adding a snubber circuit to the converter has a negative impact on the overall efficiency. Therefore, the snubber design needs to be optimized for the converter to obtain the best overall performance in EMI, efficiency and also total system cost. In chapter 3.1, different passive circuits are discussed to limit this voltage spike and to protect the main switch. In chapter 3.2, an enhanced active clamping method will be described which can decrease or even eliminate the losses caused by the passive snubber circuit.

3 Flyback Snubber Design

As previously described, using snubber circuits in a flyback converter design are essential to obtain a proper and reliable design. Snubbers can be designed either as passive or as active circuit. Passive snubber circuit elements are restricted to resistors, capacitors, inductors and diodes. Passive snubbers may be either dissipative or non-dissipative. If the energy in the snubber is dissipated in a resistive element, it is classified as a dissipative snubber. In case the energy is returned to the input or the output, it is classified as non-dissipative.

3.1 Passive Snubbers Circuits

The mostly used snubber circuits in cost sensitive designs are the passive dissipative snubber circuits.

3.1.1 Primary RCD-Snubber Circuit

Figure 5 shows a passive snubber circuit in parallel to the primary winding. It consists of a diode, capacitor and a resistor.

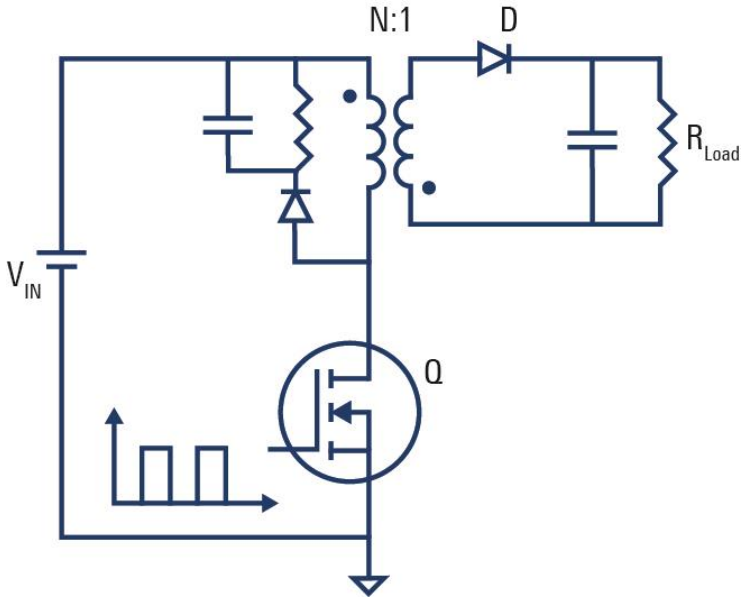

Figure 5 Passive RCD Snubber

This solution is simple and inexpensive, since no additional control circuit is needed. The circuit belongs to the class of the dissipative snubber and absorbs the energy in the leakage inductance in two steps. Firstly, the current generated by the leakage inductance flows into the clamping capacitor when the switch node voltage is above the clamping voltage. Secondly, the resistor discharges the clamping capacitor and dissipated the power into heat. In some designs, an additional resistor in series to the diode is used to reduce EMI emissions.

3.1.1.1 Design Considerations

The designer needs to consider and measure different parameters to obtain a proper snubber design. First, the relevant leakage inductance has to be measured. It is important to measure this with an impedance analyzer or an LCR bridge like the R&S®HM8118 ideally at the relevant switching frequency of the converter. The primary leakage can be measured when all other secondary windings are shorted. Of course, a low leakage inductance is desired to avoid high voltage spikes at the switch node. Therefore, a proper design of the transformer, the core element of the flyback converter, is essential.

The second important determination is to define how much voltage can be tolerated at the MOSFET drain switch node. However, it is important to limit the reduction of the clamp voltage rise at the switch to avoid massive overall dissipation within the snubber resistor. A conservative design for the peak voltage V_{Peak} is to be equal to ½ of the flyback voltage. However, in offline designs (switched mode power supply which is connected to the AC-Line voltage directly, no line transformer is used) which are often constrained to use a MOSFET with a maximum voltage of 650V, the peak voltage will have a hard limit set by the maximum input line, and FET breakdown voltage.

The value of the snubber resistor is given by the following equation:

$$R_{Snubber} = \frac{2\,V_{Clamp}*(V_{clamp}-V_{Flyback})}{L_{Lk}*F_{Switch}*\hat{\imath}_{Primary}{}^{2}} \quad (3)$$

With

$$V_{Clamp} = V_{Lk} + V_{Flyback} \quad (4)$$

The value of the clamp capacitor is not critical and depends on how much ripple voltage the design can tolerate:

$$C_{Snubber} = \frac{V_{Clamp}}{V_{Ripple}*F_{Switch}*R_{Snubber}} \quad (5)$$

The snubber capacitor should be ceramic or a material that offers low ESR at higher frequency. In this case, the capacitor provides an impedance curve which fits to the application.

The diode selection depends on the maximum input voltage and the maximum current caused by the snubber.

This snubber circuit is simple and relatively inexpensive, but the passive clamp circuit reduces the converter efficiency, because it dissipates the energy stored in the leakage inductance into heat. The power loss increases with switching frequency and can be calculated according the following equation:

$$P_{Clamp} = \frac{V_{Clamp}}{V_{Clamp}-V_{Flyback}} * \frac{1}{2} * L_{Lk} * I_{Primary}^{2} * f_{SW} \quad (6)$$

3.1.1.2 RCD-Snubber Simulation

In this simulation the flyback circuit is simulated at a fixed working point and is performed without snubber components, and in addition with optimized snubber components calculated according to the design flow in the previous chapter.

3.1.1.2.1 Simulation without Snubber Circuit

The first simulation illustrates the flyback voltage waveform of the switch node (red trace) and the primary current (blue trace), when no snubber circuit is used to damp the oscillation caused by the primary leakage inductance and output capacitance of the switching element. The input voltage was set to 325V DC to simulate the peak voltage of the AC RMS voltage of 230V. It is obvious that without using any snubber technique, it is a challenge to find a suitable MOSFET device. It has to tolerate a maximum voltage of approximately 1100V when a leakage inductance of about 2,6uH is used in the simulation. With a maximum voltage of above 1000V it is not possible to find a suitable switch device based on common silicon, which is the MOSFET. Therefore, applying a snubber is a common technique to reduce the peak voltage, and in addition to improve EMI emissions.

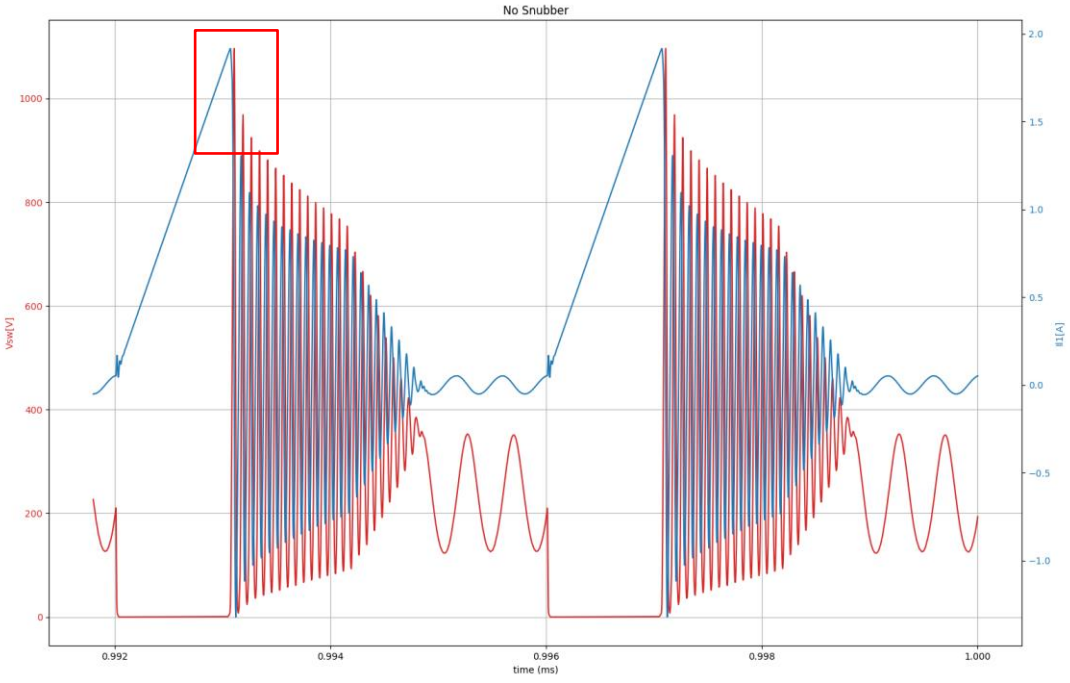

Figure 6 No Snubber Simulation

3.1.1.2.2 Simulation with Snubber Circuit

The previous simulation was extended with an added RCD Snubber circuit and illustrates the reduction of the maximum voltage at the drain of the switching device to half of the previous voltage spike.

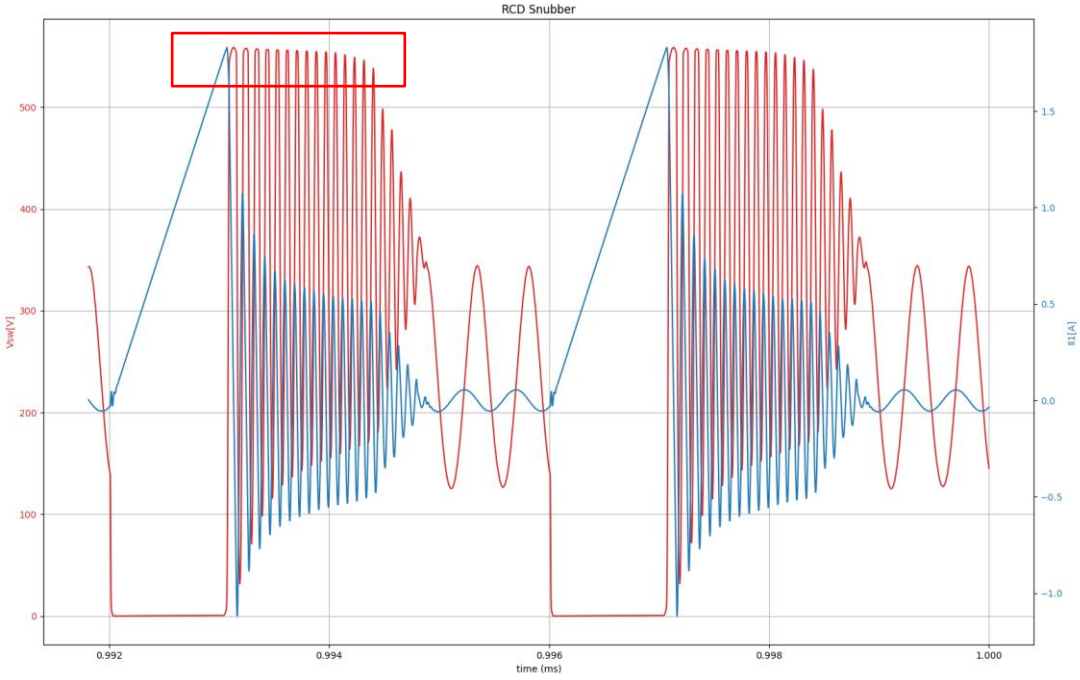

Figure 7 Simulation with RCD-Snubber

The maximum voltage is about 550V, which is a manageable voltage to find a proper MOSFET, which would be a 650V type. The existing oscillations during the off-time of the switch will create EMI noise, because the resonance circuit is not damped by the introduced clamping circuit. Therefore, an additional RC-Damping circuit may be added to damp the high frequency oscillation. This RC-Damping circuit will be discussed in chapter 3.1.2.

3.1.1.3 RCD-Snubber Measurement

In addition to the previous simulation results, a real device under test was used to demonstrate the effect of the snubber circuit. The focus of the measurements is to highlight the effect of the snubber used in the circuit to reduce a high voltage peak at the drain of the switching element.

3.1.1.3.1 Measurement without Snubber Circuit

The measurement illustrates a situation where a snubber circuit was disabled to measure the highest peak voltage. This measurement was performed at lowest input voltage to ensure that the MOSFET will not be exposed to more than 650V.

Figure 8 Maximum Drain Source Voltage (No Snubber)

The measurement shown in Figure 8 shows the voltage between drain and source (switch node) on channel 1 (yellow trace) and the primary current (measured across a shunt resistor) on channel 2 (green trace).

Remark: The voltage on channel 2 is the measured voltage across a shunt resistor of 1,075Ω. A math channel within the oscilloscope can be used to calculate the equivalent current values which is more convenient to read out the current values directly according the vertical scale of the math channel.

It is remarkable that the peak voltage reached almost 490V even at a lower input voltage of 115V RMS and 1A output current. However, this margin is enough for a MOSFET with 650V break-down voltage to survive, but this is only true because of the reduction of the input voltage down to 115V. When an input voltage of 230V RMS is applied, the device would exceed the break-down voltage of 650V and would fail with a high

probability. Therefore, a snubber is essential, even if the measured leakage inductance of 4uH has a pretty small value. The leakage inductance value was measured with the LCR bridge.

3.1.1.3.2 Measurement with Snubber Circuit

The following measurement illustrates how an effective snubber design according to the design flow described in chapter 3.1.1.1 can limit the voltage peak at the drain of the switching element.

Figure 9 Maximum Drain Source Voltage with Snubber

The measurement shown in Figure 9 shows the voltage between drain and source (switch node) on channel 1 and the primary current on channel 2. The same working point (V_{in} = 115V, I_{out} = 1A) was used to demonstrate the functionality of the snubber circuit.

Remark: The voltage on channel 2 is the measured voltage across a shunt resistor of 1,075Ω. A math channel within the oscilloscope can be used to calculate the equivalent current values which is more convenient to read out the current values directly according the vertical scale of the math channel.

It is clearly visible that the voltage spike caused by the leakage energy is limited to a value of approximately 228V by the snubber components. In this case, the margin to the break-down voltage of 650V is increased. Even an operation of the converter at its nominal input voltage of 230V RMS does not violate the maximum allowed voltage. A quick estimation would lead to a maximum peak voltage of 390V.

3.1.1.3.3 Conclusion

The usage of a snubber and its validation process is essential in flyback converters to obtain a reliable design. Of course, this snubber design example is a dissipative solution, and thus the energy is wasted into heat. The snubber design is always a tradeoff between the maximum allowable voltage of the switching device and the dissipated energy caused by the snubber. However, a validation process performed with an oscilloscope is mandatory, to ensure that the maximum peak voltage under all circumstances does not exceed the device limits.

3.1.2 Primary RC-Damping Circuit

When the reverse recovery period of the clamp diode of the RDC-Snubber is completed, the primary winding is unclamped and leakage inductance will now ring with the parasitic capacitances connected to the drain of the main switch. The RDC-Clamp does not eliminate all primary circuit ringing, and an additional snubber circuit would be beneficial in order to optimize EMI emissions. The ringing that occurs after reverse recovery of the clamp diode can be eliminated with the use of an additional RC-Damping circuit connected at the switch node.

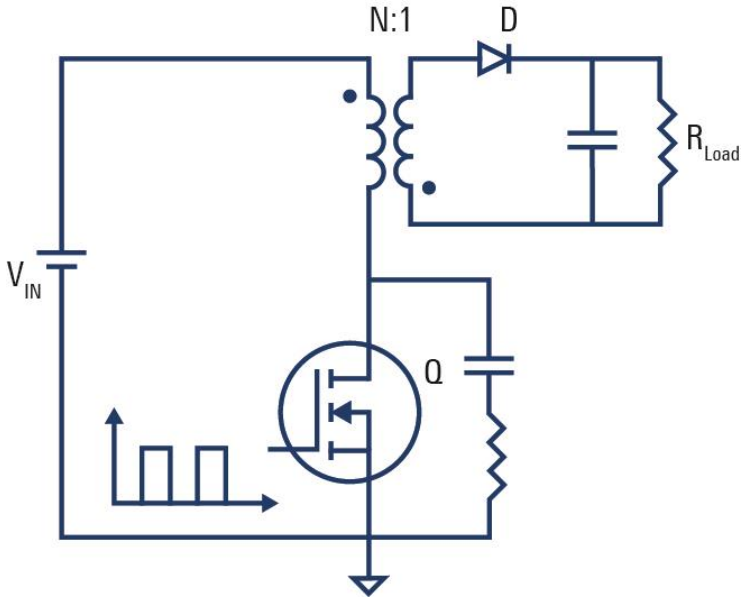

Figure 10 Primary RC-Damping

3.1.2.1 Design Considerations

The solution is to damp the oscillations and dissipate the energy into heat. The most effective way to do is to add an RC-Circuit in parallel to the low side MOSFET to damp the resonance at the oscillation frequency F_O.

3.1.2.2 Calculation of the damping circuit components

To effectively damp the oscillations, the resistance of the damping circuit can be calculated as follows:

$$R_{SNB} = \frac{1}{2*\zeta} * \sqrt{\frac{L_{Lk}}{C_{Lk}}} \quad (7)$$

In case, the damping factor zeta is set to 1, the damping in the system is called critically damped. This critical damping definition is the border between the overdamped and underdamped cases. This is exactly what the snubber resistor should provide [[1.

The definition of the damping capacitor is defined as follows:

$$C_{SNB} = \frac{1}{2*\pi*R_{SNB}*F_O} \quad (8)$$

Based on these definitions, the values of the leakage inductance and parasitic capacitance can be obtained by performing an in-circuit measurement.

3.1.2.3 In-Circuit measurement approach

While the primary leakage inductance can be measured with an LCR-Meter independent of the converter, the parasitic capacitance of the switch node is often difficult to obtain, because it consists of the output capacitance and in addition all parasitic created by the printed circuit board. Furthermore, the output capacitance of the MOSFET C_{OSS} is not linear with the drain-to-source voltage, and therefore the measurement with an LCR-Meter like the R&S®HM8118 does not provide proper values. Therefore, the user should rather follow an in-circuit measurement approach where the values are obtained during the operation of the converter.

First thing to do is to measure the frequency F_O of the oscillation during normal operation. It is important that the resonance circuit is not influenced by the attached probe as far as possible. The measurement of the frequency may be a challenge, as the probe will affect the high frequency ringing signal, due to the probe input capacitance. Therefore, it is crucial to use a probe with lowest input capacitance to obtain the most accurate measurement. For the same reason, the basic probing rules and recommendations should be considered.

Next step is to add an additional test capacitor to obtain half of the oscillation frequency which is named F_1. With the two measured frequencies and the known test capacitor, the parasitic capacitance of the MOSFET can be calculated.

$$C_{LK} = \frac{C_{add}}{x^2 - 1} \tag{9}$$

With

$$x = \frac{F_O}{F_1} \tag{10}$$

Knowing the parasitic capacitance of the switch node, the primary leakage inductance can be calculated as follows:

$$F_O = \frac{1}{2 * \pi * \sqrt{L_{LK} * C_{LK}}} \tag{11}$$

With

$$L_{LK} = \frac{1}{(2 * \pi * F_O)^2 * C_{LK}} \tag{12}$$

For an effective damping, it is desirable to obtain a ringing frequency which is 10-times higher than the switching frequency of the converter. In this case, the snubber will only damp the desired ringing and does not produce large additional losses at lower frequencies e.g. at the switching frequency. If the oscillation frequency is closer to the switching frequency, higher losses within the damping circuit will affect system efficiency. If the losses are too high, the only solution is to redesign the transformer to reduce the primary leakage inductance, and thus the oscillation frequency will be higher. A proper RC-Snubber circuit requires a capacitor which provides good high frequency characteristics. A ceramic or a film capacitor offers low ESR at higher frequency. In this case, the capacitor provides an impedance curve which fits to the application.

The power dissipated into the damping network can be estimated from the snubber capacitance, the voltage across the capacitance and the switching frequency as follows:

$$P = C * V * f_{SW} \tag{13}$$

3.1.2.4 Simulation with an Additional RC-Damping Circuit

In the following simulation is based on the one presented in chapter 3.1.1.2.2. It can be clearly seen that the oscillation is damped very effectively. The oscillation is totally gone after few oscillations, while the energy is transferred to the output.

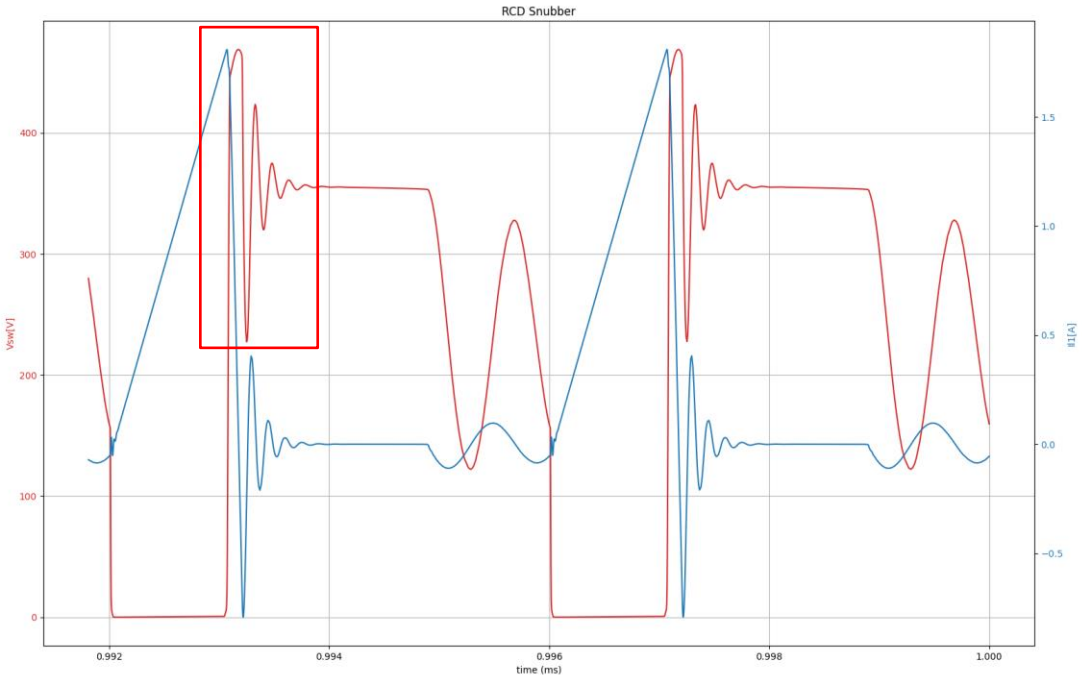

Figure 11 Simulation of RC-Damping (RCD-Snubber included)

Remark: No real measurement with the DUT was performed due to the fact that the measurement shown in chapter 3.1.1.3.2 showed no massive oscillation, like in the previous simulation. Therefore, a RC-Damping circuit was not necessary in the real design, which leads to a higher efficiency.

3.1.2.5 Conclusion

The design approach to damp the ringing after switch-off of the switching device shows that this is a very effective way to limit EMI in the design. A real measurement was not performed, because the oscillation visible in the simulation was not present in the real circuit. Nevertheless, the design technique followed by the validation process may be required in other designs.

3.1.3 Secondary RC-Damping Circuit

In many applications, in addition to the snubber on the primary side, also a RC-Damping circuit on the secondary side is required to protect the rectifier diode against any voltage stress, and it is sometimes required to pass the EMI final test. The ringing appears at the turn-off of the diode and may be severe. Especially a Schottky diode, which is often used to increase converter efficiency, is very sensitive against any overvoltage and must be well protected.

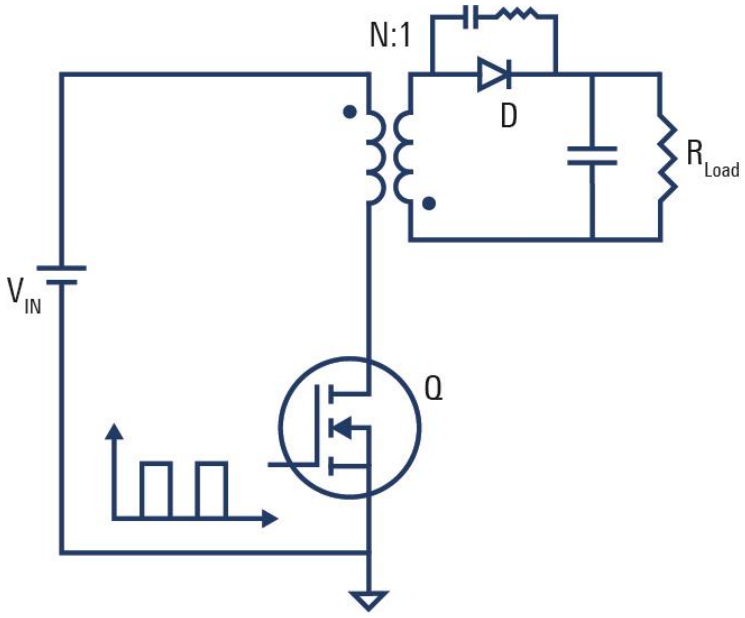

Figure 12 Secondary RC-Damping Circuit

3.1.3.1 Design Considerations

In general, the design needs a snubber because the secondary side leakage inductance forms a resonance circuit with the parasitic capacitance of the rectifier diode. The goal is to damp the ringing and dissipate the energy into heat. The most effective way to do is to add an RC-Circuit in parallel to the rectifier diode to damp the resonance at the oscillation frequency F_O.

3.1.3.1.1 Calculation of the snubber components

To effectively damp the oscillations, the resistance of the damping circuit can be calculated as follows:

$$R_{SNB} = \frac{1}{2*\zeta} * \sqrt{\frac{L_{Lk}}{C_{Lk}}} \quad (14)$$

In case, the damping factor zeta is set to 1, the damping in the system is called critically damped. This critical damping definition is the border between the overdamped and underdamped cases. This is exactly what the snubber resistor should provide [1].

The definition of the damping capacitor is defined as follows:

$$C_{SNB} = \frac{1}{2*\pi*R_{SNB}*F_O} \quad (15)$$

Based on these definitions, the values of the secondary leakage inductance and parasitic diode capacitance can be obtained by performing an in-circuit measurement.

3.1.3.1.2 In-Circuit measurement approach

While the secondary leakage inductance and the parasitic diode capacitance is difficult to measure with an LCR-Meter, the user should rather follow an in-circuit measurement approach.

First thing to do is to measure the frequency F_O of the oscillation during normal operation. It is important that the resonance circuit is not influenced by the attached probe, as far as possible. The measurement of the frequency may be a challenge as the probe will affect the high frequency ringing signal, due to the probe input capacitance. Therefore, it is crucial to use a probe with lowest input capacitance and high bandwidth to obtain the most accurate measurement. A suitable probe would be the R&S®RT-ZD10 which provides very low input capacitance, high bandwidth, and a sufficient voltage measurement range. The basic probing rules and recommendations should be followed, as always.

Next step is to add an additional test capacitor to obtain half of the oscillation frequency which is named F_1. With the two measured frequencies and the known test capacitor, the parasitic capacitance of the diode can be calculated.

$$C_{LK} = \frac{C_{add}}{x^2 - 1} \tag{16}$$

with

$$x = \frac{F_O}{F_1} \tag{17}$$

Knowing the parasitic capacitance of the rectifier diode, the secondary leakage inductance can be calculated as follows:

$$F_O = \frac{1}{2 * \pi * \sqrt{L_{LK} * C_{LK}}} \tag{18}$$

with

$$L_{LK} = \frac{1}{(2 * \pi * F_O)^2 * C_{LK}} \tag{19}$$

For an effective damping purpose, it is desirable to obtain a ringing frequency which is 10-times higher than the switching frequency of the converter. In this case, the snubber will only damp the desired ringing and does not produce large additional losses at lower frequencies e.g. at the switching frequency. If the oscillation frequency is closer to the switching frequency, higher losses within the damping circuit will affect system efficiency. If the losses are too high, the only solution is to redesign the transformer to reduce the primary leakage inductance and thus oscillation frequency will be higher. A proper RC-Snubber circuit requires a capacitor which provides good high frequency capability. A ceramic or a film capacitor offers low ESR at higher frequency. In this case, the capacitor provides an impedance curve which fits to the application.

The power dissipated into the damping network can be estimated from the snubber capacitance, the voltage across the capacitance and the switching frequency as follows:

$$P = C * U^2 * f_{SW} \tag{20}$$

ff

3.1.3.2 Simulation with a RC-Damping Circuit on the Secondary Side

3.1.3.2.1 Simulation without Snubber Circuit

The simulation of the flyback is used to demonstrate how effectively a snubber can reduce the massive oscillation. The first simulation shows the oscillation of the rectifier voltage during the switch-on of the main switch during turn-on cycle. The oscillation at the diode voltage show a peak to peak value of about 40V at 12 MHz. This will cause EMI problems and also damage the rectifier diode, if it is not designed for that maximum voltage.

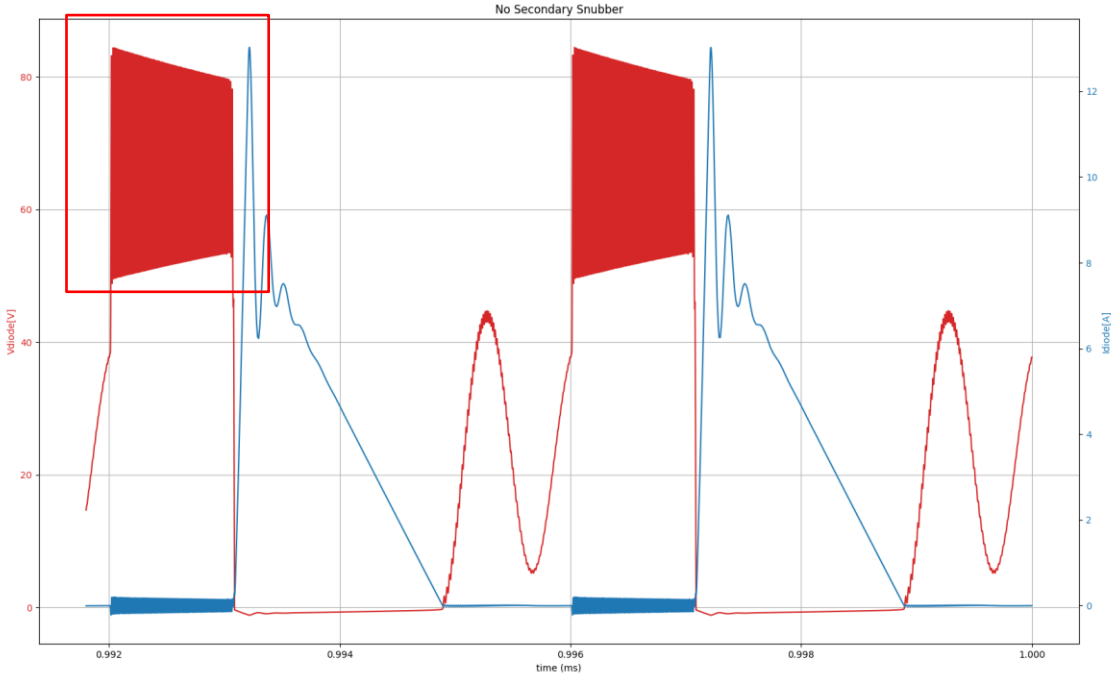

Figure 13 Simulation of secondary oscillation (RC-Damping not used)

Knowing from the simulation result above, a RC-Damping circuit is required. Therefore, the design approach adding a snubber, as discussed previously, was executed, and the result is shown in the next chapter.

3.1.3.2.2 Simulation with Snubber Circuit

The following simulation is based on the simulation presented in chapter 3.1.3.2.1. It can be clearly seen that the oscillation is damped very effectively. The oscillation is totally gone after few oscillations, during the phase when the energy is transferred to the output.

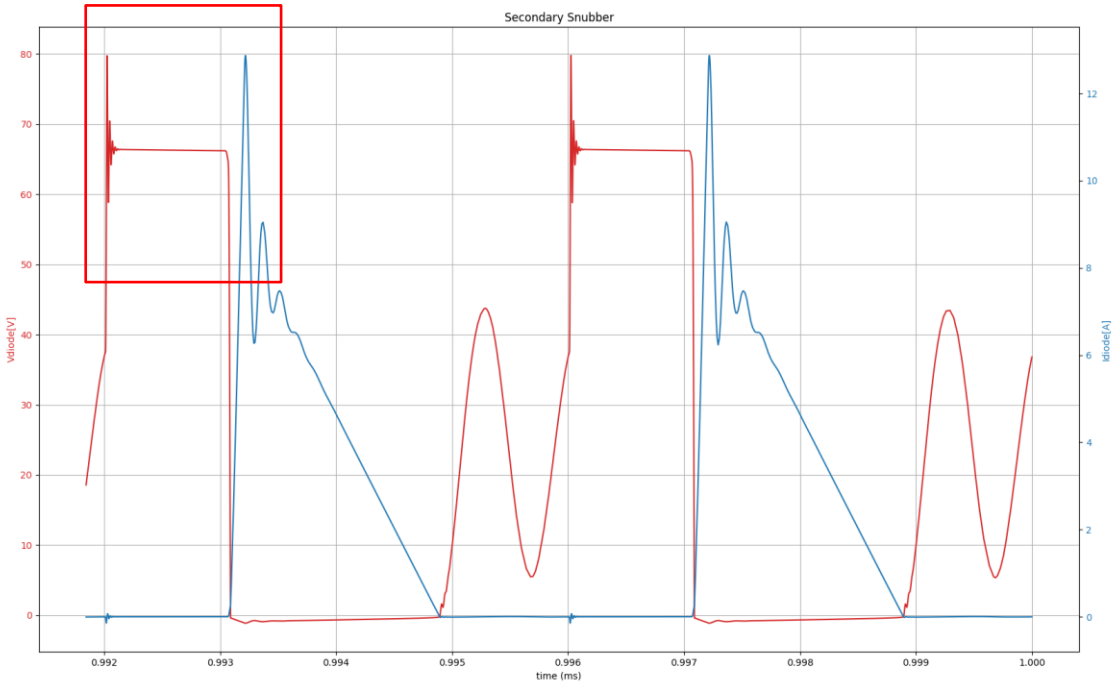

Figure 14 Simulation of Secondary Oscillation with RC-Damping

This simulation shows how effective a RC-damping circuit can be on the secondary rectifier. This method will be evaluated with a real measurement in the next chapter.

3.1.3.3 Measurement of RC-Damping Circuit on the Secondary Side

In this chapter, the previously described method was applied with the DUT. On the evaluation board, pads are provided to insert a RC-Damping circuit in parallel to the secondary rectifier, but initially no components were assembled. This is the starting point of this case study.

3.1.3.3.1 Measurement without Damping Circuit

The first measurement shows the starting point, where the voltage oscillation on channel 3 (orange) is measured over the rectifier diode with a proper differential probe, like the R&S RT-ZD10/RT-ZA15, after the main switch is turned on. This oscillation reaches its maximum value of 30V at the beginning, and lasts for more than 500ns, which will influence the EMI emissions. The frequency of this critical oscillation is in the range of 26 MHz. The maximum voltage of the diode is limited to 50V according to the datasheet. Therefore, enough safety margin regarding the maximum voltage is left in the system.

Figure 15 Rectifier Diode Oscillation

However, the EMI emissions are still one of the main focus in a converter, and cannot be neglected. Therefore, the RC-damping circuit is still required to reduce the emissions at this particular frequency. A more precise measurement was performed and is illustrated in Figure 16.

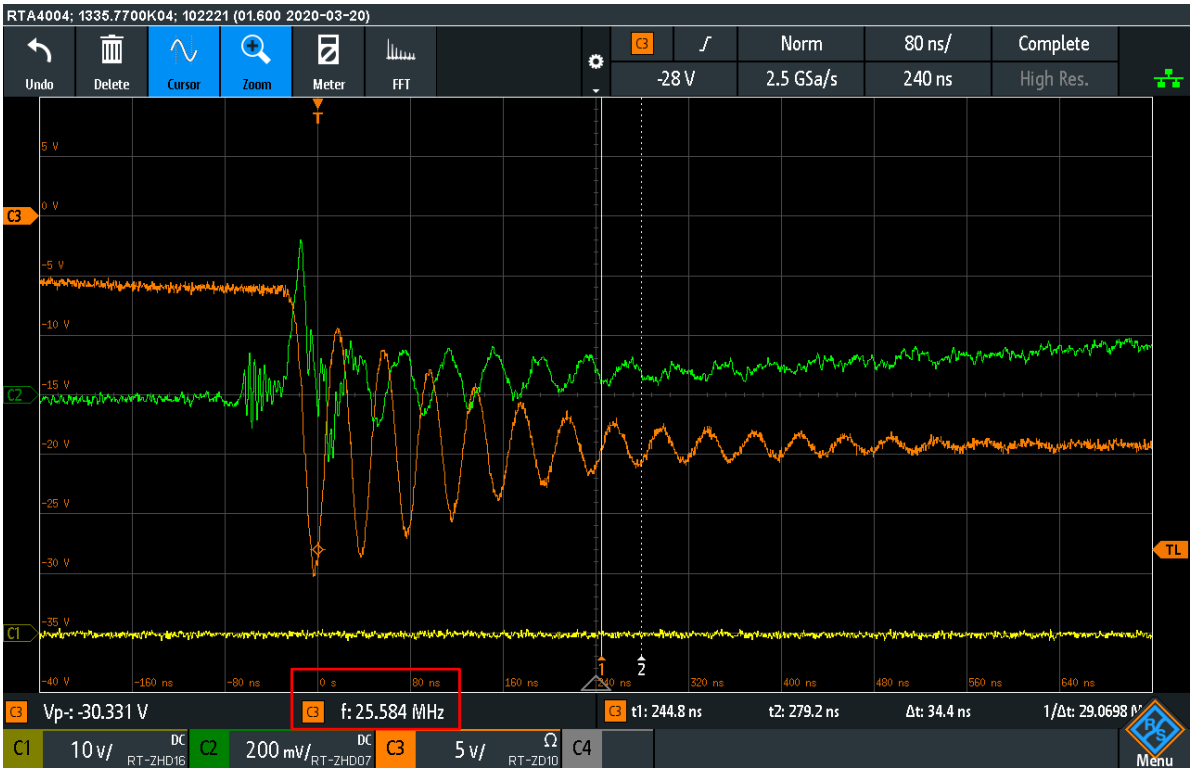

Figure 16 Rectifier Diode Oscillation (no additional capacitor)

As a result, the frequency reading is slightly shifted to 25,6 MHz, due to the optimized setting of the oscilloscope.

The next step was to add an additional capacitor (178 pF measured with the LCR bridge) to shift the oscillation frequency. This measurement result is shown in Figure 17.

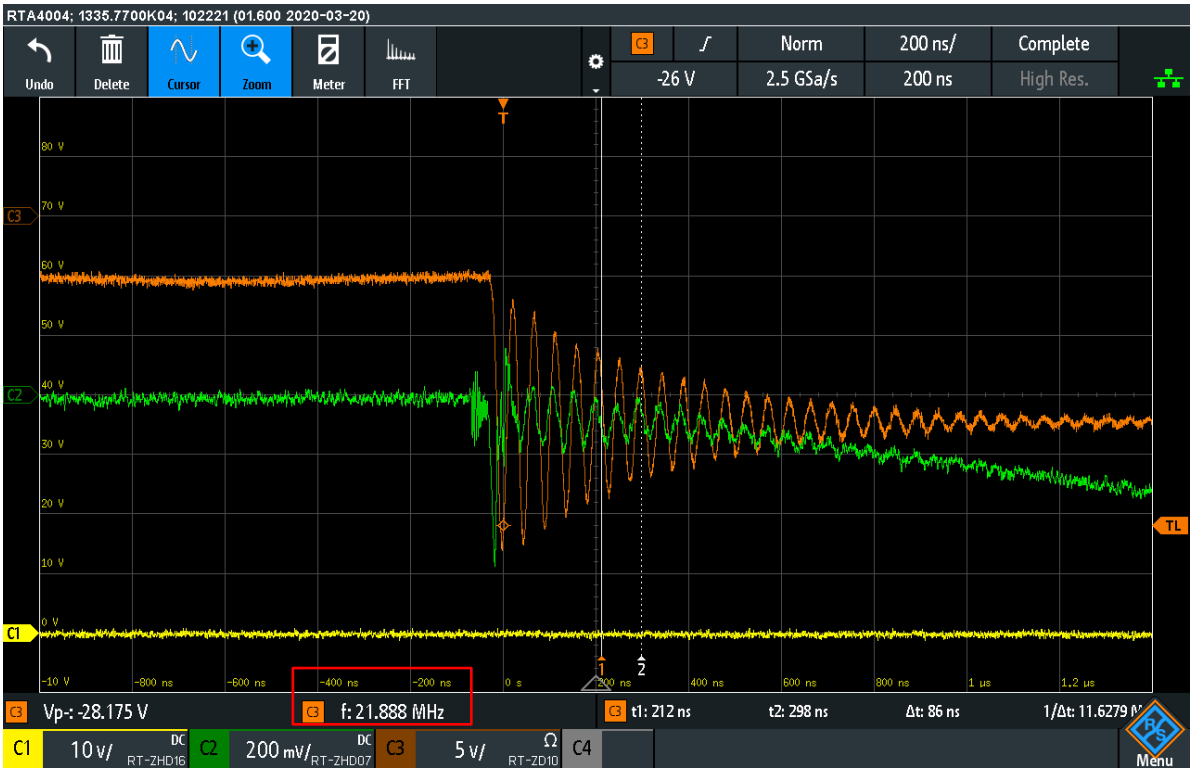

Figure 17 Rectifier Oscillation with additional 178 pF (Measured with LCR meter) capacitor

The frequency changes, caused by the additional capacitor, to about 21.9 MHz. With equations 16 and 17, the leakage capacitance was calculated and is equal to

C_{Lks} = 471 pF

This leakage capacitance is very close to the value within the datasheet. With this leakage capacitance value, and by using the equation 18 and 19, the secondary leakage inductance can be calculated and is equal to

L_{Lks} = 81 nH

Now, with C_{Lks} and L_{Lks} known, and by using the equations 14 and 15, the selected values are the following:

R_{SNB} = 35 Ω with a Damping factor of 0,19.

By using equation 15, the required capacitor would be C_{SNB} = 178 pF.

The damping factor was selected in a manner that the efficiency of the converter reaches still reasonable values, and the EMI emissions are decreased to fulfil the limits. The measurement including the RC-Damping circuit is illustrated in the next chapter.

3.1.3.3.2 Measurement with Damping Circuit

The measurement illustrated in Figure 18 shows a reasonable damping effect due to the RC damping network, compared with the measurement shown in Figure 16.

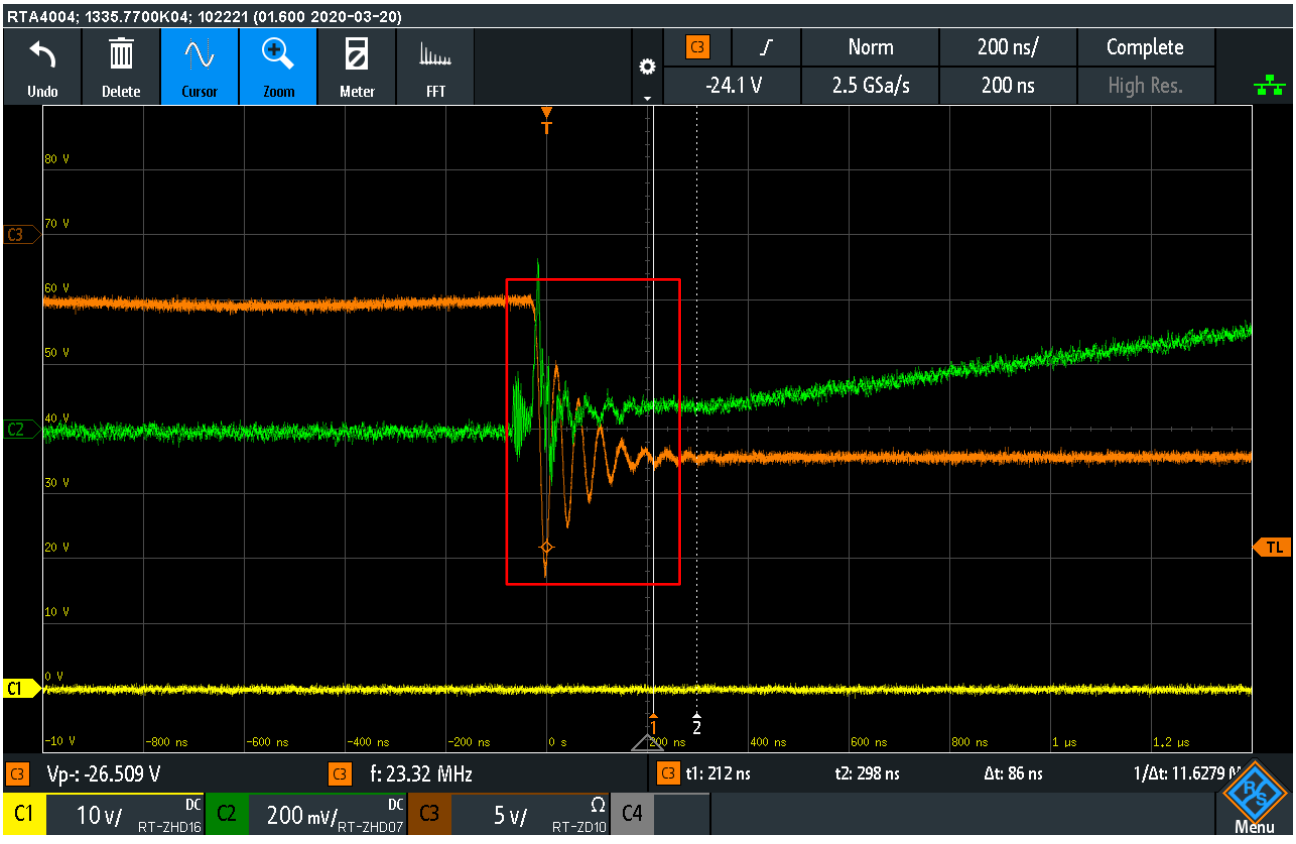

Figure 18 Rectifier Oscillation with the calculated RC damping network

3.1.3.3.3 Conclusion

The usage of a RC-damping circuit applied to the secondary rectifier, and its mandatory validation process with proper measurement tools, is essential in flyback converters to obtain a reliable design, as overvoltage is harmful for all semiconductor components and increases the MTBF rate. Of course, this used RC damping design example is a dissipative snubber solution and thus the energy is wasted into heat. The RC damping design is always a tradeoff between the maximum allowable voltage of the switching device, the EMI emissions the design can tolerate, and the dissipated energy caused by the RC damping circuit. However, a validation process performed with an oscilloscope is mandatory, to ensure that all relevant design values under all circumstances do not exceed the device limits.

3.2 Active Snubber Circuits

The active clamp snubber circuit belongs to the non-dissipative snubber group. The active clamp snubber circuit replaces the common RCD-snubber circuit by using an additional high side switch (Q2) and clamp capacitor (C_{clamp}). These two components offer the designer a more efficient way of converter operation. The basic circuit of the active clamp flyback is illustrated in Figure 19.

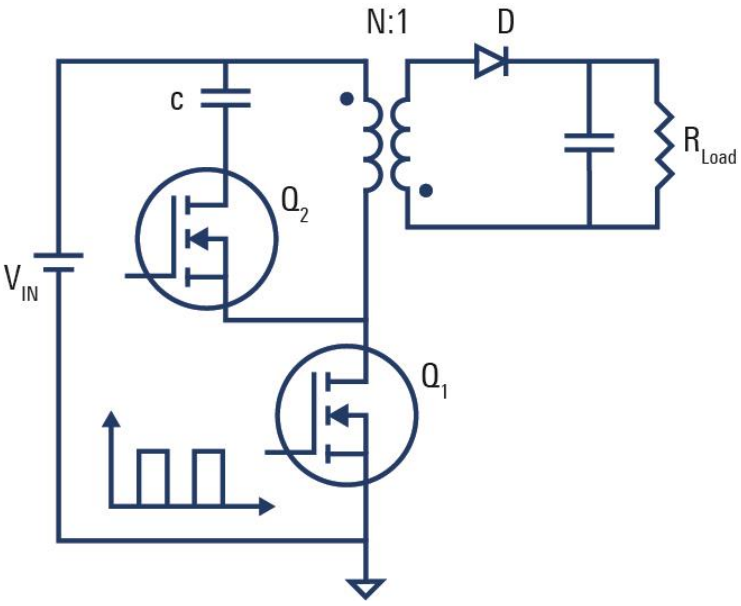

Figure 19 Active Clamp Structure

The new circuit provides a mechanism to store the energy of the leakage inductance which also protect the main switch from overvoltage. The fact, that the auxiliary switch (Q2) is able to conduct the clamp current in a bidirectional way, helps to transfer leakage energy back to the output through the transformer primary to secondary turns ratio. This happens during every switching cycle which reduces the losses tremendously compare to other passive clamping solutions used in state of the art flyback converters. This allows choosing a higher switching frequency for the design (>200kHz) to obtain a more compact design, while the efficiency can become very high. In addition to the benefits described previously, the principle also offers zero voltage switching of the low side switch, when a smart control method is used by the controller circuit.

3.2.1 Control of the Active Clamp Circuit

Unfortunately, all the benefits do not come for free and some drawbacks also exists in the active clamp solution. The control of the clamp switch requires an additional high side driver which causes higher cost in the bill of material. Furthermore, a smart and intelligent control algorithm has to be implemented in the controller to drive the switches at the correct timing. However, the controller offered by Texas Instruments [2] features these functionalities and, in addition, it ensures at high output power that the low side switch operates in zero voltage switching during the turn on condition of the main switch.

3.2.2 Working principle

The working principle of the active clamp flyback topology is illustrated in Figure 20 and is described below:

During turn-on period of the low side switch (1), energy is stored in the magnetizing inductance and in addition in the leakage inductance as described in chapter 2.2. During the switch off event of the main switch (2), the leakage energy is transferred through the body diode of the clamp switch into the clamp capacitor. Therefore, almost no peak on the switch node voltage is visible. Shortly after the conduction time of the body diode, the clamp switch is turned on by the controller (U_{GH}) and the leakage inductance can resonate with the clamp capacitor (3). While the clamp switch is in on state, the leakage energy and the magnetizing energy is transferred to the secondary side of the transformer and through the rectifier diode to the output.

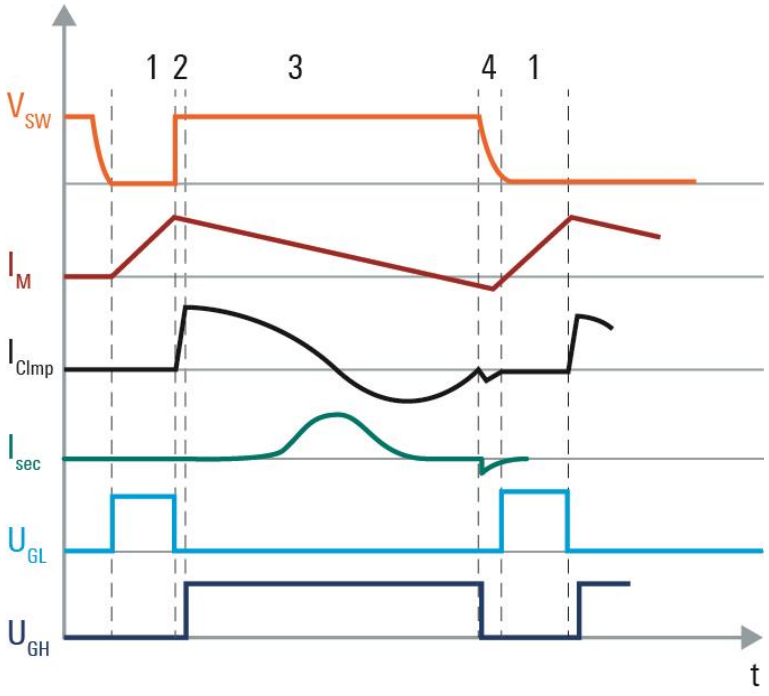

Figure 20 Active Clamp Waveforms (AAM)

Just before the energy within the resonance circuit becomes zero, the clamping switch is turned off and the charge present in the output capacitance of the low side switch is removed by the negative current (4). This ensures zero voltage switching of the low side switch during the next switch on event (1). Thereby clamping and switching losses are reduced to a minimum. However, in reality the converter does not always operate in this highly efficient mode and proper validation methods have to be applied to ensure proper operation over all circumstances e.g. at light load conditions where the high side switch is disabled (no active clamping)

3.2.3 Design Consideration

Beside the main principle of an active clamp flyback circuit, most of the calculation are in relation to the controller working principle. Therefore, the major equations to select the proper components are defined within in the datasheet of the controller supplier [2]. For example. the calculation of RMS current of the clamp switch needs to be done to estimate that the MOSFET operates in a valid operation range. Furthermore. the calculation of the clamp capacitor is critical and needs to be done according to the datasheet [2].

3.2.4 Active Clamp Case Study

Remark: The used DUT for all measurements within this chapter was the evaluation module provided by Texas Instruments UCC28780EVM-021 [3].

As the active clamp flyback topology offers more converter efficiency due to its additional clamping switch and therefore a passive snubber is not required anymore, several measurements are still required to validate the converter design properly. In the next chapters, few examples are presented which are the most important validation methods and have mainly the focus on the switch node voltage like in the previous passive snubber methods. Before the designer can start the validation process, it is very important to get sufficient knowledge about the controller functionalities. The best method to gain knowledge is to study the datasheet of the controller. However, this document should rather explain the reader with the most important measurement methods of a flyback converter and not explain the controller modes in details. Therefore, the next paragraphs are just a very short explanation of the main controller modes to present sufficient knowledge to understand the background of the performed measurements.

The complex controller provides several different operation modes to obtain always the best and most efficient way to convert the input power to the output power over the whole operating range. Therefore, the controller itself features the following operation modes:

► Adaptive Amplitude Modulation (AAM)

This mode is used at higher load where the output level ranges approximately from 2,25 A down to 1,5 A to reach highest efficiency. In this mode, the controller operates always in the transition mode or boundary conduction mode and the duty cycle is adopted accordingly with peak primary current mode control. Therefore, the clamping MOSFET operates in each turn off period of the low side switch to ensure the active clamping. As described previously, this ensures that the leakage energy is reused on the secondary side. In addition, this ensures also a zero-voltage operation of the low side switch during turn-on. This mode is the most efficient mode and the waveforms are illustrated in detail in Figure 20.

► Adaptive Burst Mode (ABM)

It is used from the medium load region down to the light load region where the output current level ranges approximately from 1,5 A down to 0,18 A. In this output current level range, the converter operates in a more efficient way compared to the previous mode. In this mode, the controller provides a burst mode operation. This means that the controller generates burst packages where the converter operates in the active clamp mode (AAM) within the bursts and stops operation between each burst period. The number of burst cycles varies while the output current changes. In this mode the ZVS mode is not performed at the first cycle of a burst package and hard switching will occur.

► Low Power Mode (LPM)

It is used in the light load region and ranges approximately from 0,18 A down to 0,08 A. During this mode, the high side switch is disabled and the active clamping principle is not applied at all. Therefore, the ZVS condition will never occur and the design has to be validated that the voltage at the switch node does not exceed the break down voltage of the low side switch. This can happen if to many switching cycles in this mode occur and the resistor connected in parallel to the clamp capacitor does not provide a suitable impedance to discharge the clamp capacitor. In this case, the switch node voltage will be higher and is only limited by the clamp capacitor and the discharge resistor.

► Standby Power Mode (SPM)

The standby power mode is entered at an output current lower than 0,08 A in order to minimize standby power. In this mode, only two switching cycles are used as applied in the low power mode, but the time between the two pulses are extended to obtain a lower burst frequency. Of course, in this mode the high side switch is still disabled including the driver to save energy.

3.2.4.1 Validation of Adaptive Amplitude Modulation

As described previously, in the AAM the active clamp function is always activated. In this case the, the low-side switch should be well protected against any voltage spike due to the clamp capacitor. Of course, the maximum voltage depends also on the correct calculation of the clamp capacitor. However, the clamp capacitor was calculated according to the datasheet of the controller and the maximum drain source voltage should not exceed approximately the input peak voltage plus the reflected voltage which is 105 V in this used design.

The measurement illustrated in Figure 21 show the AAM Mode (@ 80% load, V_{in} = 90V RMS).

Channel 1 = V_{ds}

Channel 2 = $I_{Primary}$

Channel 3 = PWM_H

Channel 4 = PWM_L

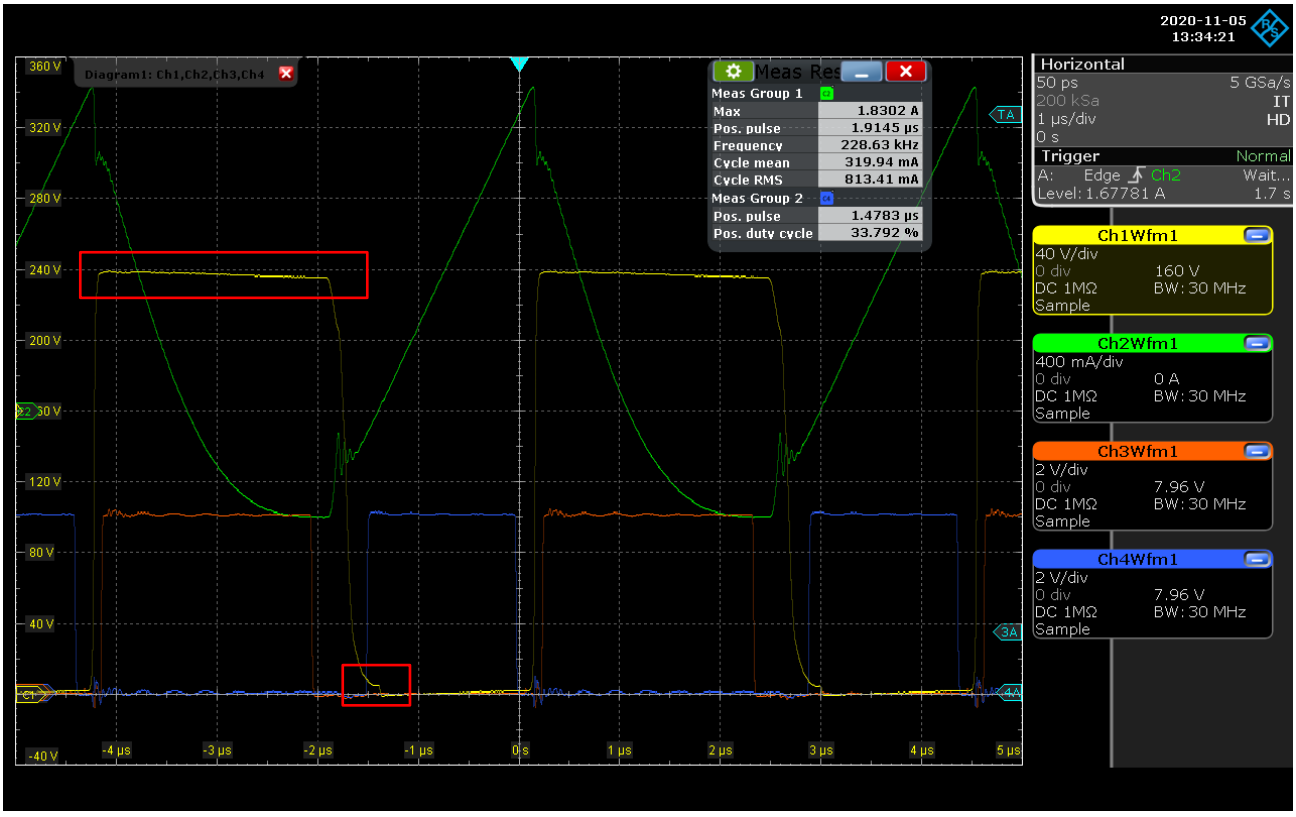

Figure 21 AAM Waveforms

The voltage at the switch node voltage is pretty flat because the high side switch conducts and absorbs the energy into the clamp capacitor. This means the maximum voltage at switch node does not exceed the break down voltage of the MOSFET because the clamp capacitor limits the voltage very effective. This is also true if the input voltage would be increased to the maximum allowable level of 240V RMS. This would lead to a maximum voltage of 450V at the switch node. Furthermore, the switch node voltage decreases due to the energy transfer during the turn- on period of the clamp switch (refer to red box in the left upper corner). The measured current in the primary inductance is the combination of the clamping current and the magnetizing current. The control signal for the high-side is active during off time and the low-side switch control signal is active during on-time respectively. It also remarkable that the ZVS condition is always ensured. This is clearly visible because the low side control signal is activated after the drain source reaches a voltage level below 10V (refer to the small red box).

3.2.4.2 Validation of AAM Mode Transition into ABM Mode

It is very important to understand that the zero-voltage condition is verified over all working points as long as the controller operates in the AAM. As described above, the complex controller provides several different operation methods to obtain always the best and most efficient way to convert the input power to the output power. However, the use of different operation modes also means that there are transition areas where the controller will leave a certain mode and will enter the next operation mode. In the measurement illustrated in Figure 22, a decreasing output current from a high level to a lower level caused the controller to change the mode from AAM into ABM. The measurement result is illustrated in Figure 22.

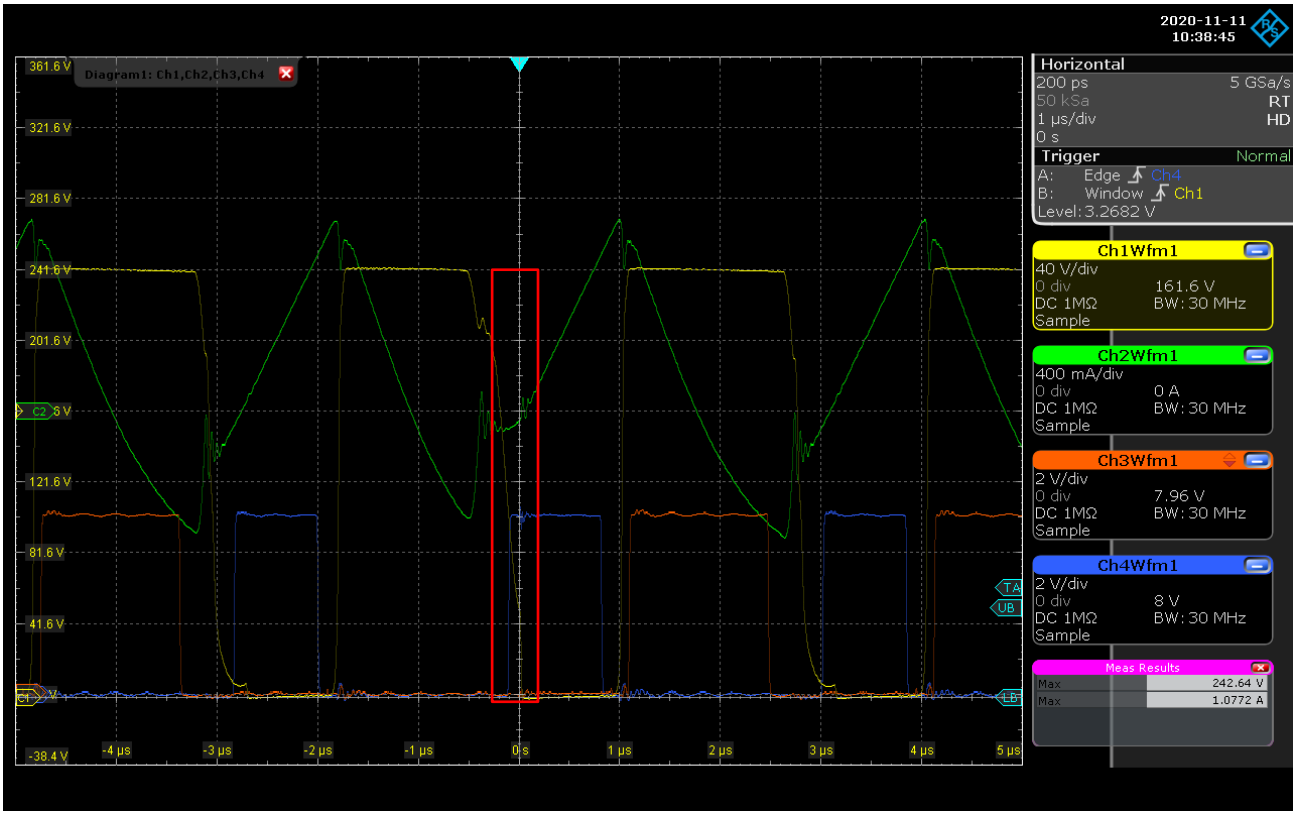

Figure 22 Transition from AAM to ABM (ZVS condition not always fulfilled)

Due to the fact that the ABM operated in burst mode, there is always at least a short period (at least one switching cycle) where the converter is not working in ZVS condition because of this mode transition. This event is very hard to capture with an analog trigger because it requires in the trigger function high sensitivity and also a possibility to define a complex A/B/R Trigger sequence. In this case, the A-Trigger was set to the positive edge of the low side control signal and continued a window trigger for the B-Trigger with very low hysteresis to capture the missing ZVS condition (red box). However, this missing ZVS condition only happens at the beginning of each burst package. Therefore, this is a regular behavior according to the datasheet. The hard-switching event causes higher switching losses and needs to be validated in further steps.

3.2.4.3 Validation of the Low Power Mode (LPM)

3.2.4.3.1 Working Principle

It is very important to validate this operation mode because the active clamp function is deactivated completely and there is a risk of an increasing switch voltage at switch-off of the low side switch. The leakage energy is not transferred back to the secondary side in this mode but it is charged into the clamp capacitor and discharged by a passive parallel resistor. However, the energy needs to be discharged to limit the maximum voltage at the switch node. Therefore, a parallel resistor also called bleed resistor needs to be placed to discharge the clamp capacitor.

The sequence which needs to be verified by a measurement is illustrated in Figure 23

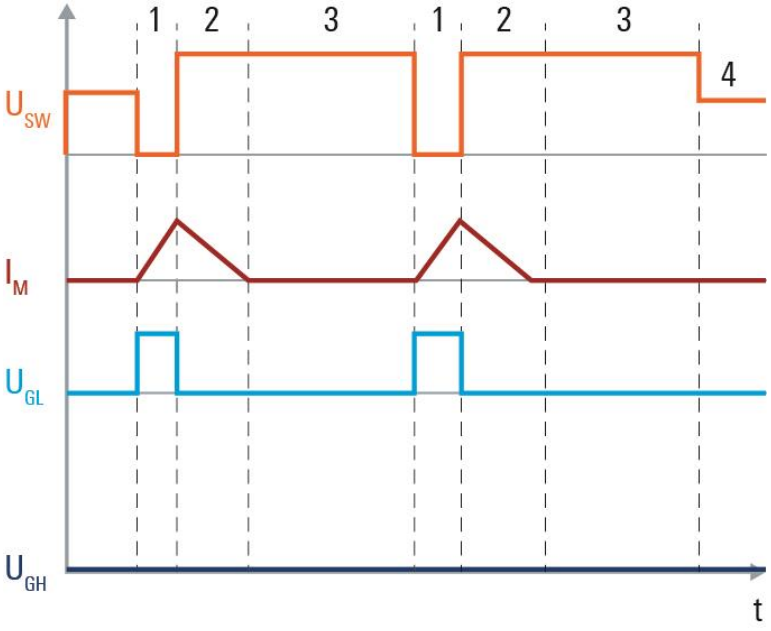

Figure 23 LPM Waveforms

The sequence illustrates that the high side switch (U_{GH}) does not switch at all within this operation mode. However, the sequence of the LPM mode starts with activating the main switch (1). After the current level has reached the desired peak level, the low-side switch will be switched-off. Now the energy within the magnetizing inductance can be transferred to the output (2). Now, the controller measures the primary current via an auxiliary winding until it detects a zero-current condition (3). If the zero current detection condition is fulfilled, the second switching event will start. In this mode, two switching events are executed before a delay of 40us is inserted before the next sequence with two cycles will appear.

3.2.4.3.2 Measurement Results

As describe previously, it is very important to validate the maximum peak voltage at the switch node for the two executed switch-on cycles. The measurement illustrated in Figure 24 show clearly that the maximum voltage at the switch node is limited to approximately 430V (red box). This measurement was performed at an input voltage of 220V RMS. As mentioned previously, the flyback voltage is around 105V and therefore the expected voltage without leakage energy contribution would be approximately 438V. However, this indicates that there is no reasonable influence of the leakage energy which could result in a higher switch node voltage. It is important to validate this condition under all circumstances which means the output current need to be changed while a complex trigger will catch any overvoltage event easily with lowest effort.

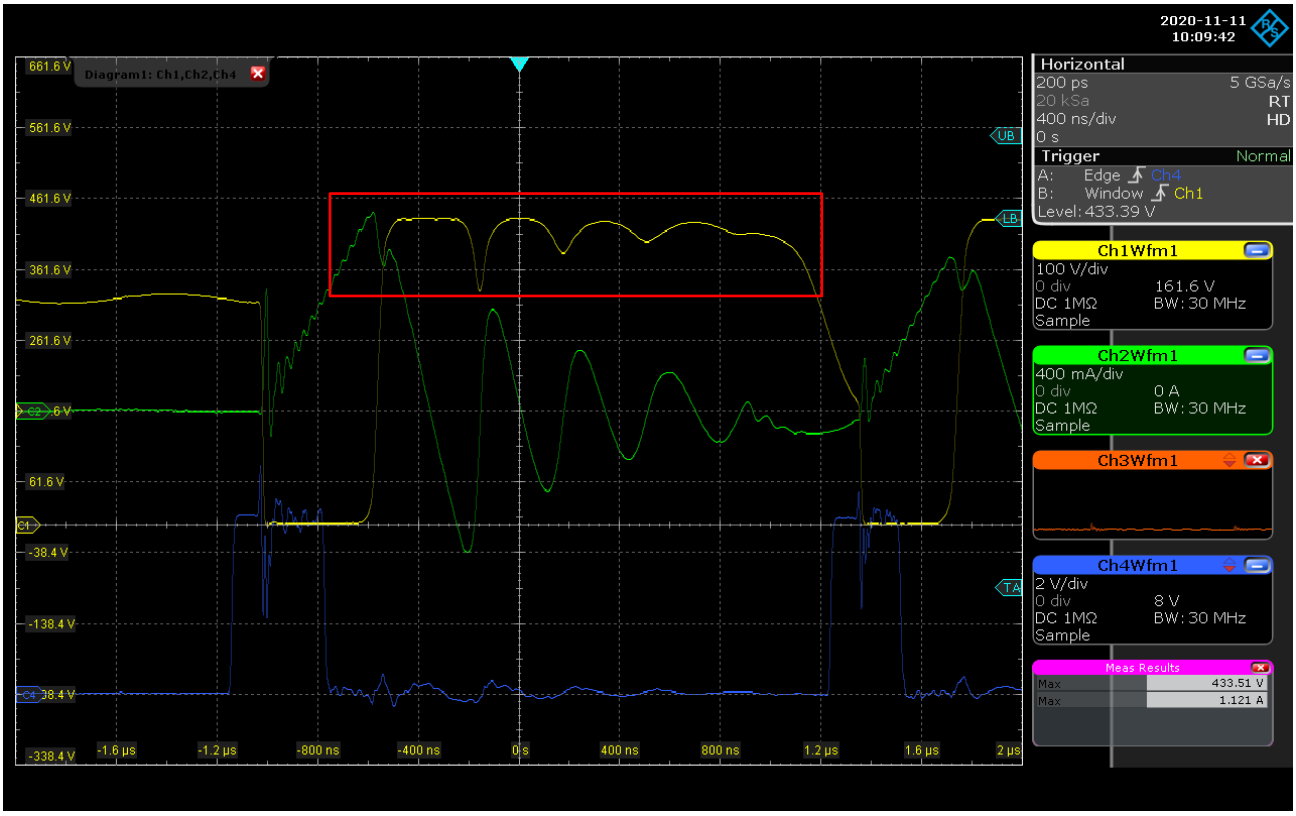

Figure 24 Low Power Mode Measurement @ Iout = 100mA

Again, a complex trigger definition (A/B/R Trigger) was used to catch the worst-case condition. In the measurement example above, the measurement system detected the maximum switch node voltage at 100mA output current. Of course, also the input voltage has to be considered to validate the maximum switch node voltage.

4 Conclusion

A state of the art flyback topology is a commonplace circuit and used in industries like consumer or industrial whenever an AC-to-DC conversion is required and needs to be performed at lower power level and the design needs to be optimized regarding overall system costs. Nevertheless, even the standard flyback is known as a simple topology, the converter still requires smart and intelligent validation methods to overcome the anomalies caused by unavoidable parasitic components.

Meanwhile, most of the parasitic components of a standard flyback converter are well understood by the power design community and are showcased in this document by a performed simulation. However, the simulation as always requires good knowledge about all parasitic to obtain reliable simulation results which are close to the real values. Therefore, a simulation may provide good and fast results initially at the beginning of the design phase, but these simulation results must be validated by real measurements in most cases. A combination is the best approach to reach enough confidence to release a reliable product to the market.

The standard flyback converter consists of a key component, the transformer. This part is the main root cause of the high voltage spikes or oscillations which can be controlled but not eliminated. Therefore, the goal of each standard flyback design is to control the voltage spikes and oscillation in a way that no other parts like the main switching semiconductor MOSFET will fail. Furthermore, the voltage spikes and oscillations may have negative effects on the EMI emissions and also these emissions need to be controlled. The snubber circuits are the state-of-the-art solution to overcome these negative effects present in flyback converters. Of course, many solutions exist to apply a snubber network to the converter. The most common solutions like the RCD dissipative snubber are presented within this document. However, it is mandatory that each snubber technique whether it is a dissipative or non-dissipative needs to be validated in the real design by proper and suitable measurements. The main tool which supports the validation procedure is the oscilloscope in combination with suitable probes.

Nowadays, semiconductor manufacturers have further developed new controllers to extend the standard flyback converter to obtain higher efficiency. However, this new controller utilizes an additional switch in combination with a complex control method to reuse the leakage energy which is wasted in previous standard flyback designs by the snubber circuits. Even a snubber is not required anymore in this new design, the validation method becomes even more important because of the complexity and of the variety of operation modes. Especially, a tool like an oscilloscope including a digital trigger may be very beneficial to catch the different operation conditions of such a complex system like an active clamp flyback converter. In this case, the designer is able to find any critical conditions within the converter operations.

In addition to the time domain validation method, an LCR measurement may support the designer to estimate real values like the leakage inductance of the transformer. Nevertheless, in some cases, an in-circuit measurement approach also can support the designer to obtain real values of parasitic components like the parasitic capacitance of the rectifier diode in combination with some math to optimize RC-Damping circuits.

5 Literature

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6 Ordering Information

Designation	Type	Order No.
NGL202 Power Supply	R&S®NGL202	3638.3376.03
Oscilloscope, 4 channels	R&S®RTA4004	1335.7700P64
Oscilloscope, 4 channels with digital trigger capabilities	R&S®RTO2064	1329.7002.64
LCR Bridge	R&S®HM8118 LCR Bridge	3593.0539.02
High Voltage Differential Probe	R&S®RT-ZHD07	1800.2307.02
Current Probe	R&S®R&S®RT-ZC20B	1409.8233.02
Differential Voltage Probe	R&S®R&S®R&S®RT-ZD10	1410.4715.02

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1SL363 | Version 0e | 06.2021
Application Note | Verification Methods Of Snubber Circuits in Flyback Converters
Data without tolerance limits is not binding | Subject to change