Interface Control Document

R&S®SMW-K506

ARB descriptor word (ADW) and control descriptor word (CDW)

Products:

► R&S®SMW200A

R&S® Munich | ICD | Version 1.1 | 04.2024

https://www.rohde-schwarz.com/appnote/1GP134

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Version	Date	Author	Comments
1.1	02.04.2024	R&S Munich	► Additional information on network interface properties
1.0	04.05.2022	R&S Munich	► First version

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1 Overview

1.1 Document Scope

The present R&S®SMW-K506 Interface Control Document contains information on

- the R&S descriptor word format, including ARB descriptor words and control descriptor words in deterministic and instant mode
- Timing requirements and limitations of the interface
- Properties of the network interface (Connector designation: HS DIGIQ).

It is intended for use by customers using descriptor words to control the R&S®SMW200A in real-time. The interface control document specifies the interface between the customer's hardware used for provision of descriptor words and the R&S®SMW200A HS DIGIQ interface. Additional information on descriptor word processing inside the R&S®SMW200A is provided.

Agile Sequencing (R&S®SMW-K506) is supported for SMW FW version 5.00.166.20 and higher.

1.2 Document Overview

The present document is organized as follows:

- Chapter 1 is this introduction which provides the scope of the document and further reference and introduces a list of abbreviations and definitions
- Chapter 2 provides the R&S descriptor word structure, including ARB descriptor words and control descriptor words in deterministic and instant mode
- Chapter 3 provides timing requirements for ADW and CDW streaming
- Chapter 4 provides information on the network interface

1.3 Further/Reference Documents

[1] "R&S®SMW-K501/-K502/-K503/-K504/-K315 Extended and Real Time Sequencing, Pulse-on-Pulse Simulation User Manual," Rohde & Schwarz.

[2] "R&S®SMW200A Vector Signal Generator User Manual," Rohde & Schwarz.

[3] "Generation of Radar Signals in a Hardware in the Loop (HIL) Environment," Rohde & Schwarz, Application Note.

1.4 Abbreviations and Definitions

The abbreviation “SMW” is used in this document for the Rohde & Schwarz vector signal generator R&S®SMW200A.

The SMW is a general-purpose vector signal generator with outstanding RF performance. It is capable of generating signals for all main communication, radio and avionic standards and of simulating GNSS signals. Equipped with one or more processing/coder boards, the SMW can be turned into a fully-fledged radar simulator for reliable and flexible testing of receivers.

Further abbreviations:

ADW	ARB Descriptor Word
CDW	Control Descriptor Word

Table 1: Abbreviations

2 R&S Descriptor Word Structure

2.1 General Descriptor Word Format Specification

2.1.1 General Descriptor Word Content

The SMW provides a dedicated interface to receive and process R&S Descriptor Words. R&S ARB Descriptor Words (ADW) can be used to replay pre-calculated and pre-stored waveform segments. R&S Control Descriptor Words (CDW) can be used to change RF frequency or level.

Descriptor Word Type	**Purpose**
ADW	Replay pre-calculated waveform (ARB) segments
CDW	Control RF parameters

Table 2: General Descriptor Word Data Content

Descriptor words are transmitted as sequence of bytes. For all descriptor words, their type is determined by flags in the header. The descriptor word size and content depend on the type.

2.1.2 Times

All times are given as number of clock cycles of the internal 2.4 GHz clock signal.

2.1.3 Bit and Byte Ordering Criteria

All data values are encoded using the following bit and byte ordering criteria:

- ► For numbering, the most significant bit/byte is numbered as bit/byte 0
- ► For bit/byte ordering, the most significant bit/byte is transmitted first (big-endian)

2.1.4 Reserved and Spare Bits

Reserved and spare bits may be used for evolution, and defined in future updates of this ICD. In order to assure compatibility with future updates, these bits should be set to 0. The same applies for stuffing bits.

2.2 ARB Descriptor Word (ADW)

Each ARB descriptor word consists of header, flags, body and payload. The SMW provides two operating modes for ADW streaming: deterministic and instant mode.

The structure for ADWs is the same for both modes. It is highlighted if ADW parameters are only evaluated in one of two operating modes. The difference between deterministic and instant mode is described in Section 3.1.

In this section all ADW components are introduced. The ARB descriptor word format is defined.

2.2.1 ARB Descriptor Word Data Content

The header and flags section of each ADW contain information about the content (structure) of the ADW. Information about the RF characteristics of the desired signal are given in the body section. The payload section addresses a pre-calculated ARB segment. The extension section can be used to play back multiple, identical segments by means of a single ADW (bursts).

2.2.1.1 Header

The ADW header section contains flags which define the content of the ADW.

ADW header			**56 Bit**
Parameter	**Data type**	**Description**	**Size**
RSVD	-	Reserved for future use	52 Bit
SEG	Boolean	0 = not supported 1 = ARB segment	1 Bit
USE_EXTENSION	Boolean	0 = ADW extension block is not used 1 = ADW extension block is used	1 Bit
RSVD	-	Reserved for future use	2 Bit

Table 3: ADW Header Structure

2.2.1.2 Flags

The ADW flags section contains information about the xDW type, interrupt mode and marker settings.

ADW flags			**8 Bit**
Parameter	**Data type**	**Description**	**Size**
CTRL	Boolean	Indicates whether the descriptor word is an ADW or a CDW 0 = ADW 1 = CDW	1 Bit

SEG_INTERRUPT	Boolean	Indicates whether the addressed segment can be interrupted by a subsequent segment or is played until the last sample. 0 = Played until last sample of segment 1 = Can be interrupted by subsequent ADW If the burst extension is used, the flag is valid for all repetitions of the segment.	1 Bit
RSVD	-	Reserved for future use	1 Bit
IGNORE_ADW	Boolean	ADW is ignored (no signal output)	1 Bit
M4	Boolean	Reserved	1 Bit
M3	Boolean	Set Marker 3	1 Bit
M2	Boolean	Set Marker 2	1 Bit
M1	Boolean	Set Marker 1	1 Bit

Table 4: ADW Flags Structure

2.2.1.3 Body

The ADW body section contains offset values for frequency, level and phase relative to the instrument RF settings.

ADW body			**64 Bits**
Parameter	**Data type**	**Description**	**Size**
FREQ_OFFSET	int	Frequency offset added to instrument RF frequency. -1 GHz <= frequency_offset <= 1 GHz FREQ_OFFSET = (frequency_offset / 2.4e9) * 2^{32}	32 Bit
LEVEL_OFFSET	unsigned int	Level offset subtracted from instrument RF level. level_offset >= 0 dB LEVEL_OFFSET = $10^{(-level\_offset / 20)} * 2^{15}$	16 Bit
PHASE_OFFSET	unsigned int	Phase offset 0° <= phase_offset < 360° PHASE_OFFSET = phase_offset/360° * 2^{16}	16 Bit

Table 5: ADW Body Structure

2.2.1.4 Payload

The payload section contains the segment index of a pre-calculated waveform.

ADW payload			**80 Bit**
Parameter	**Data type**	**Description**	**Size**
SEGMENT	unsigned int	Index of the pre-calculated waveform, which was loaded into the SMW memory in advance	24 Bit
RSVD	-	Reserved for future use	56 Bit

Table 6: ADW Payload Structure

2.2.1.5 Extension

The 6 Byte extension is evaluated if the USE_EXTENSION bit in the header is set to 1. If USE_EXTENSION=0, all extension fields should be filled with zeros.

Extension fields [USE_EXTENSION=1]			**48 Bit**
Parameter	**Data type**	**Description**	**Size**
BURST_SRI	unsigned int	Segment repetition interval (SRI) from first sample to first sample BURST_SRI = (SRI in seconds) * 2.4e9	32 Bit
BURST_ADD_SEGMENTS	unsigned int	Number of repetitions in addition to the initial segment 0 = infinite repetitions (do not use with SEG_INTERRUPT = 0)	16 Bit

Table 7: ADW Extension Structure if USE_EXTENSION=1

Extension fields [USE_EXTENSION=0]			**48 Bit**
Parameter	**Data type**	**Description**	**Size**
STUFFING	-	Fill with 0	48 Bit

Table 8: ADW Extension structure if USE_EXTENSION=0

2.2.2 ARB Descriptor Word Bits Allocation

An ADW consists of header, flags, body, payload and extension. The extension content depends on the USE_EXTENSION flag in the header. **Error! Reference source not found.** shows the bit allocation for an ADW with extension, Table 9 shows the bit allocation for an ADW without extension.

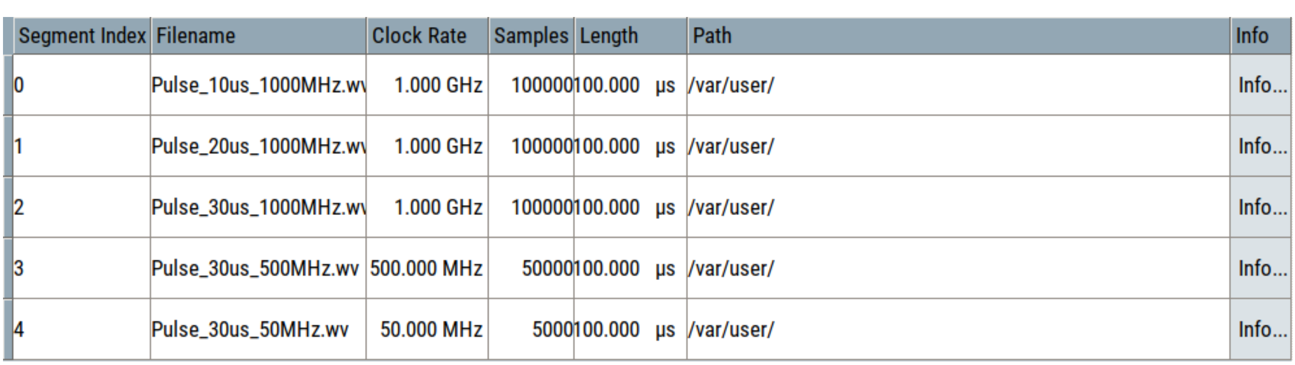
Header	**Flags**	**Body**	**Payload**	**Extension**	**Total (bits)**
56	8	64	80	48	256

Table 9: Bits allocation of ADW without extension

2.2.3 ARB segment streaming (rates and memory usage)

ARB segments have to be uploaded to the SMW before starting the simulation. This can be performed via the SMW GUI or remotely with SCPI commands.

A table showing all preloaded segments can be accessed via the SMW GUI.



Segment Index	Filename	Clock Rate	Samples	Length	Path	Info
0	Pulse_10us_1000MHz.wv	1.000 GHz	100000	100.000 µs	/var/user/	Info...
1	Pulse_20us_1000MHz.wv	1.000 GHz	100000	100.000 µs	/var/user/	Info...
2	Pulse_30us_1000MHz.wv	1.000 GHz	100000	100.000 µs	/var/user/	Info...
3	Pulse_30us_500MHz.wv	500.000 MHz	50000	100.000 µs	/var/user/	Info...
4	Pulse_30us_50MHz.wv	50.000 MHz	5000	100.000 µs	/var/user/	Info...

Figure 1: Pre-calculated segment table view in the SMW200A GUI

Each individual waveform is assigned a segment index (first column) which is used inside the ADW (SEGMENT in ADW payload) to address the respective waveform segment.

All waveforms appended to this list are internally resampled to a common clock rate. A container file is automatically created, which is downloaded to the memory of the coder board. After this, the SMW is ready to receive ADWs with a segment index to select and play a waveform.

In order to reach high ADW streaming rates with ARB segments, the SMW firmware up-samples the user waveforms before processing them in hardware to minimize the hardware resampling delay. This in turn leads to a higher memory usage.

The desired ARB sample rate can be selected in the SMW200A GUI:

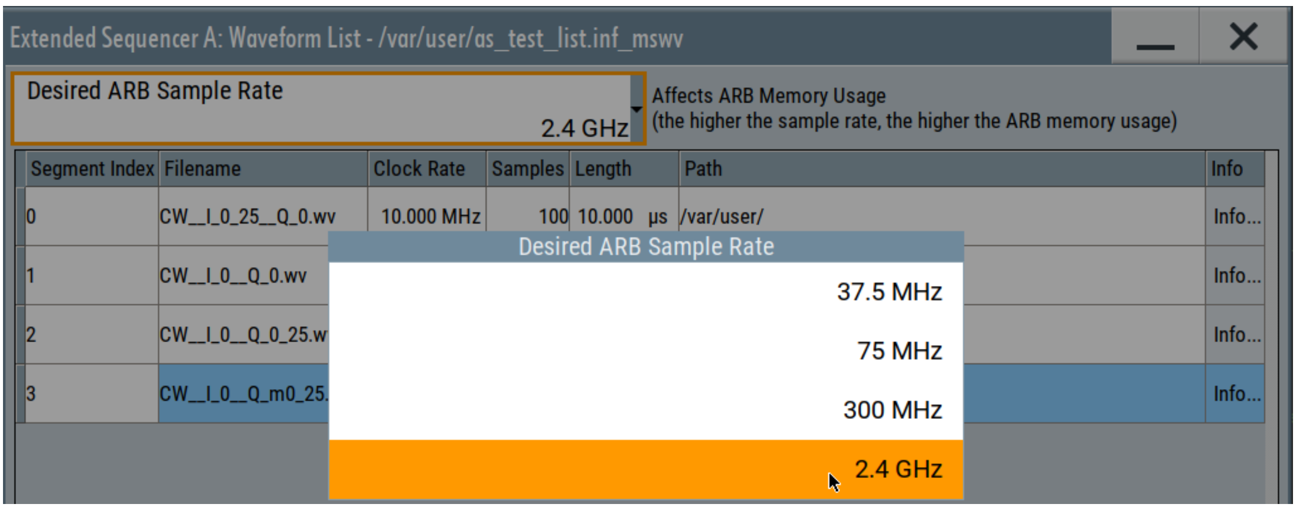


Figure 2: Selection of desired ARB Sample Rate in SMW200A GUI

The selected sample rate determines the waveform clock rate after resampling and consequently the memory usage. The following table provides an overview about desired ARB segment sample rate, waveform clock rate, minimum segment length and as an example minimum memory usage for 1000 segments with a lengths of 100 µs each.

Desired ARB Sample Rate	**Waveform Clock Rate**	**Minimum segment length**[1]	**Minimum Memory Usage (1000 segments; 100 µs per segment)**[2]
37.5 MHz	max(37.5 MHz, highest clock rate of loaded segments)	27.3 µs	15 MByte
75 MHz	max(75 MHz, highest clock rate of loaded segments)	13.7 µs	30 MByte
300 MHz	max(300 MHz, highest clock rate of loaded segments)	3.41 µs	120 MByte
2.4 GHz	2.4 GHz	427 ns	960 Mbyte

Table 10: Overview about relation of max. ARB sample rate, waveform clock rate, min. segment length and memory usage

The 24 Bit SEGMENT field inside the R&S ADW theoretically allows to address 2^{24} = 16.777.216 individual waveforms. The maximum number of segments with minimum segment size is 2 million.[2]

[1] Minimum RAM granularity = 1024 Samples
[2] Max. Memory size = 2 GSamples (requires SMW-K515)

2.3 Control Descriptor Word (CDW)

By setting the CTRL flag in the xDW flags section, the user can issue commands such as changing the instrument RF frequency and/or amplitude of the signal generator directly from the descriptor word, where otherwise a SCPI command would have been necessary.

As with ADWs, the content and layout of CDWs is the same for both deterministic and instant mode. The difference in timing is described in Section **Error! Reference source not found.**.

2.3.1 Control Descriptor Word Data Content

A CDW consists of header, flags and body. The header and flags of each CDW specify the command type. Information about the instrument RF settings are given in the body section.

2.3.1.1 Header

The CDW header section contains flags which define the command type.

CDW header			**56 Bit**
Parameter	**Data type**	**Description**	**Size**
RSVD	-	Reserved for future use	52 Bit
PATH	Boolean	Specifies RF path which is affected by CDW 0 = Path A 1 = Path B	1 Bit
CMD	unsigned int	Specifies command type 0 = Frequency change 1 = Amplitude change 2 = Frequency and amplitude change	3 Bit

Table 11: CDW Header Structure

2.3.1.2 Flags

The CDW flags section contains information about the xDW type.

CDW flags			**8 Bit**
Parameter	**Data type**	**Description**	**Size**
CTRL	Boolean	Indicates whether descriptor word is an ADW or a CDW 0 = ADW 1 = CDW	1 Bit
RSVD	-	Reserved for future use	7 Bit

Table 12: CDW Flag Structure

2.3.1.3 Body

The CDW body section contains values for instrument RF frequency and level.

<table>
<tr><th colspan="3">CDW body</th><th>64 Bit</th></tr>
<tr><th>Parameter</th><th>Data type</th><th>Description</th><th>Size</th></tr>
<tr><td>FVAL</td><td>unsigned int</td><td>RF frequency setting of signal generator in Hz</td><td>40 Bit</td></tr>
<tr><td>LVAL</td><td>signed
fixed point
BCD</td><td>RF level setting of signal generator in dBm
<table>
<tr><th>Bit</th><th>0</th><th>1-7</th><th>8-11</th><th>12-15</th><th>16-23</th></tr>
<tr><td>Value</td><td>Sign
0=pos
1=neg</td><td>Integer
part</td><td>Tenth
part</td><td>Hundredth
part</td><td>Unused
(Set to 0)</td></tr>
</table></td><td>24 Bit</td></tr>
</table>

Table 13: CDW Body Structure

2.3.2 Control Descriptor Words Bits Allocation

The bit allocation of a CDW is shown in the following table.

Header	Flags	Body	Total (bits)
56	8	64	128

Table 14: Bits allocation of CDW

3 Timing requirements

3.1 ADW Processing

The SMW provides two modes for ADW streaming. The deterministic mode should be used if there are strict timing requirements for segment playback. If this is not required, instant mode can be used where segments are played back as soon as the ADW has been processed. The operating mode can be configured in the SMW GUI or via SCPI command (see R&S®SMW200A Manual).

Irrespective of the operating mode, the SMW features a receive buffer (FIFO) for 512 ADWs. ADWs are taken out of this FIFO at a maximum rate of 1ADW/µs or 1MADW/s (see Minimum ARB segment playback repetition interval in R&S®SMW200A datasheet). This has to be considered at the transmit side. The flow control is within the responsibility of the user.

For the following sections the convention is as follows:

- ADW #x addresses segment #x (referred to as current ADW and current segment)
- ADW #y addresses segment #y (referred to as next ADW and next segment)

3.1.1 Deterministic Mode Processing

In deterministic mode, once an ADW arrives at the HS DIGIQ interface, the data is unpacked and written into a buffer. When the ADW is taken from the FIFO, the addressed ARB segment is loaded and a ready-marker is provided at the configured global or local connector. The user can then trigger the playback of the next segment (see R&S®SMW200A Manual for Trigger/Marker configuration). After the segment was triggered, the next ADW in line is processed. This process is illustrated in Figure 4 and Figure 4.

SEG_INTERRUPT = 0

In case the SEG_INTERRUPT flag of the current ADW (ADW #x) was set to 0, the ready marker for the next ADW (ADW #y) is delayed until the current segment (segment #x) has been played until the last sample.

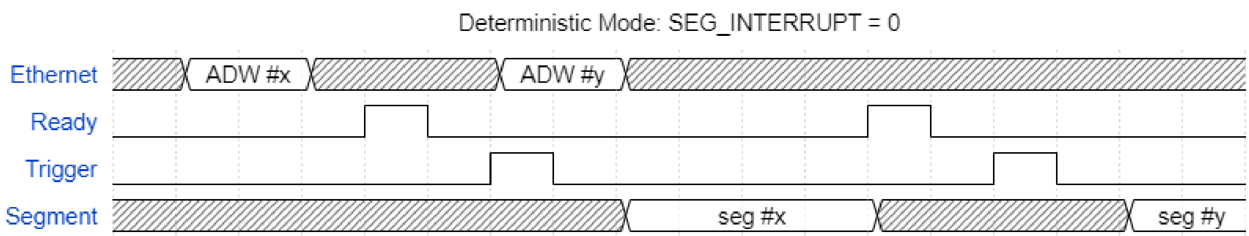


Figure 3: Timing diagram of segment playback in deterministic mode with SEG_INTERRUPT=0 in ADW #x

SEG_INTERRUPT = 1

In case the SEG_INTERRUPT flag of the current ADW (ADW #x) was set to 1, the ready marker for the next ADW (ADW #y) is provided as soon as the ADW was processed. Triggering the next segment (segment #y) immediately interrupts the current segment (segment #x).

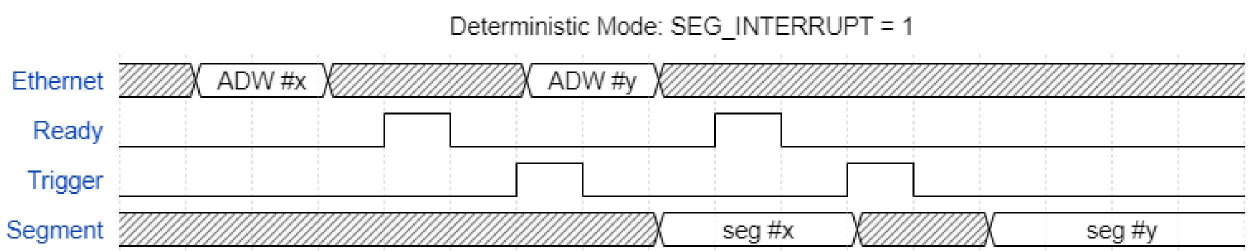


Figure 4: Timing diagram of segment playback in deterministic mode with SEG_INTERRUPT = 1 in ADW #x

The delay between the rising trigger edge and the segment appearing at the RF output is deterministic up to the jitter given in the R&S®SMW200A datasheet. This delay depends on the configured ARB sample rate and is also given in the R&S®SMW200A datasheet. The ARB sample rate can be configured on creation of an ARB segment list.

3.1.2 Instant Mode Processing

In instant mode, ARB segments are played back as soon as possible, without the need for an external trigger. In this mode, the delay between the arrival of the ADW at the HS DIGIQ interface at the SMW and the signal appearing at the RF output of the SMW is not deterministic.

SEG_INTERRUPT = 0

If the SEG_INTERRUPT flag is set to 0, the segment is always played back until the last sample. Playback is not interrupted by other successively arriving ADWs (See Figure 5).

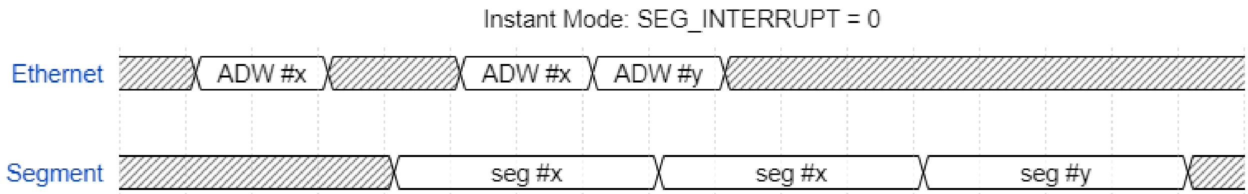


Figure 5: Timing diagram for segment playback in instant mode with SEG_INTERRUPT=0 in ADW #x

SEG_INTERRUPT = 1

If the SEG_INTERRUPT flag is set to 1, the playback of the currently played segment is interrupted to start the playback of the segment addressed by a successively arriving ADW as soon as possible (see Figure 6).

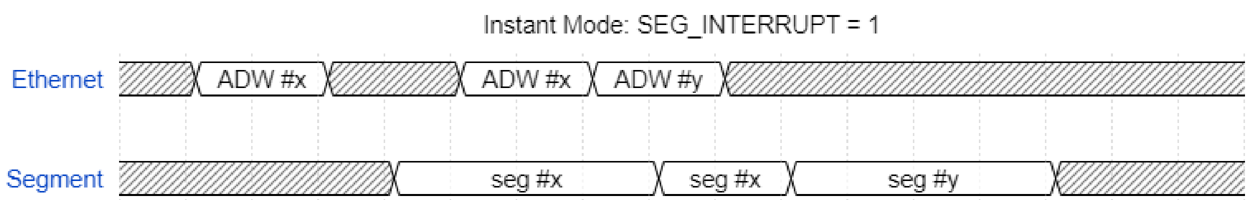


Figure 6: Timing diagram for segment playback in instant mode with SEG_INTERRUPT=1 in ADW #x

4 Network Interface Properties

Connector designation	HS DIGIQ
Mechanical connector	QSFP+ / QSFP 28
Mandatory adapter	40G QSFP+ to 10G SFP+ adapter converter module
Supported data rates	10 Gbit/s
Supported network protocols	UDP over Ethernet

Table 15: Network interface properties

The figure below illustrates the connection between the SMW200A HS DIGIQ interface and a PC with a 10G SFP+ ethernet network interface.

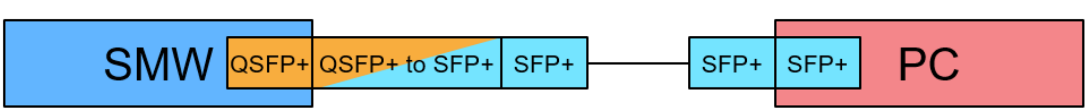


Figure 7: Connection between the SMW200A HS DIGIQ interface and a PC with a 10G SFP+ ethernet network interface

Note: ADW/CDW streaming is only supported for point-to-point connections between a user equipment's network interface and the SMW200A HS DIGIQ interface. Routing via hubs, switches or routers is not supported!

Sending ADWs via UDP to the SMW, it must be considered that the sender application is responsible for fragmenting the ADW data into UDP datagrams of an appropriate size. It is highly recommended to limit the datagram size to a maximum of 512 bytes.

To improve real-time capability, the Address Resolution Protocol (ARP) table of the sender should be up-to-date before starting to send UDP datagrams. Otherwise, the first datagram will be possibly sent delayed, since the sender has to send an ARP request and wait for the response to update his ARP table before. This can be done by sending empty UDP datagrams to the SMW interface. The procedure has to be repeated depending on the ARP table timeout of the sender.

5 Appendix

A Examples

A.1 ADW with Extension

Parameter	Parameter Value	Meaning	Binary Data
ADW Header			
RSVD	0	-	0x00000000000004
RSVD	0	-	
USE_EXTENSION	1	True	
RSVD	0	-	
ADW Flags			
CTRL	0	False	0x01
SEG_INTERRUPT	0	False	
RSVD	0	-	
IGNORE_ADW	0	False	
M4	0	-	
M3	0	Marker 3 off	
M2	0	Marker 2 off	
M1	1	Marker 1 on	
ADW Body			
FRQ	-14660155	-125 MHz	0xf2aaaaaa5a9e5555
LEV	23198	3 dB	
PHS	21845	120°	
ADW Payload			
SEGMENT	2	Waveform #2	0x000002000000000000000
RSVD	0	-	
ADW Extension			
BURST_SRI	192000	80 µs	0x0002ee000009
BURST_ADD_SEGMENTS	9	9	

ADW: 0x00000000 0x00000401 0xf2aaaaaa 0x5a9e5555 0x00000200 0x00000000 0x00000002 0xee000009

A.2 ADW without Extension

Parameter	Parameter Value	Meaning	Binary Data
ADW Header			
RSVD	0	-	0x00000000000000
RSVD	0	-	
USE_EXTENSION	0	False	
RSVD	0	-	
ADW Flags			
CTRL	0	False	0x41
SEG_INTERRUPT	1	True	
RSVD	0	-	
IGNORE_ADW	0	False	
M4	0	-	
M3	0	Marker 3 off	
M2	0	Marker 2 off	
M1	1	Marker 1 on	
ADW Body			
FRQ	29320310	250 MHz	0xcaaaaaaa40261555
LEV	16423	6 dB	
PHS	1820	10°	
ADW Payload			
SEGMENT	100	Waveform #100	0x00006400000000000000
RSVD	0	-	
ADW Extension			
STUFFING	0	-	0x000000000000
STUFFING	0	-	

ADW: 0x00000000 0x00000041 0xcaaaaaaa 0x40261555 0x00006400 0x00000000 0x00000000 0x00000000

A.3 CDW

Parameter	Parameter Value	Meaning	Binary Data
ADW Header			
RSVD	0	-	0x0000000000000a
PATH	1	Path B	
CMD	2	Frequency and amplitude change	
ADW Flags			
CTRL	1	True	0x80
RSVD	0	-	
ADW Body			
FVAL	10900000000	10.9 GHz	0x0289b0cd008d0000
LVAL	-7536640	-13 dBm	

CDW: 0x00000000 0x00000a80 0x0289b0cd 0x008d0000

Rohde & Schwarz

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