R&S®CMW500 Digital IQ with CADENCE Emulator Application Note

Products:

- | R&S[®]CMW500
- | R&S[®]EX-IQ-BOX | R&S[®]EXBOX-Z3
- | R&S[®]FSQ
- | R&S[®]FSV

This application note explains how to bring a CADENCE system which is attached to an R&S[®]EX-IQ-BOX into service for the first time.

The first part of the document shows how to setup an LTE Demo without using a UE design. This setup uses the R&S[®]CMW500 as the downlink transmitter. The emulator receives the downlink via an R&S[®]EX-IQ-BOX and passes it to an R&S spectrum analyzer (R&S[®]FSx) via a second R&S[®]EX-IQ-BOX.

The second part describes the real wiring using up- and downlink. This will only work if a UE design is available on the emulator.



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The following abbreviations are used throughout this manual:

R&S[®]EX-IQ-BOX is abbreviated as R&S EX-IQ-BOX, R&S[®]EXBOX-Z3 is abbreviated as R&S EXBOX-Z3, R&S[®]CMW500 is abbreviated as R&S CMW500, R&S[®]FSQ is abbreviated as R&S FSQ and R&S[®]FSV is abbreviated as R&S FSV.

1 Hardware Setup for LTE Demo

1.1 Schematic Setup



Figure 1: Setup Diagram

1.2 Hardware Requirements for Demo

Amount	Unit	Hardware Key					
R&S CMV	R&S CMW500 minimum configuration						
1	R&S CMW-B300A Signaling Unit Wideband (SUW)	1202.6304.02					
1	R&S CMW-B510A Digital IQ Board	1202.8007.02					
Adapter							
2	R&S EX-IQ-BOX	1409.5505K04/.02					
2	R&S EXBOX-Z3 CADENCE PALLADIUM Breakout 1417.3566.02 Board						
1	CADENCE HDDC Breakout Board SCSI V	39BRSA					
1	Cadence Palladium Emulator						
R&S FSQ	or R&S FSV						
1	R&S FSQ-B17 Digital Baseband Interface	1163.0063.02					
Cabeling							
2	R&S SMU-Z6 LVDS cable for connecting digital baseband interfaces	1415.0201.02					
1	BNC cable						
1	BNC cable (<= 1m)						
1	BNC T adapter						
2	USB cable						
2	SCSI II to SCSY V cable						

1.3 Cabeling of All Units

External PC	R&S CMW500	R&S EX-IQ-BOX I	R&S EX-IQ-BOX II	CADENCE HDDC Breakout Board SCSI V	R&S FSQ/ R&S FSV
From/ To	From	From/To	From/To	From/To	From/To
	DIGIQ OUT2	DIG IQ IN 1			
USB		USB			
USB			USB		
	REF OUT	REF IN			
		REF IN split with BNC T adapter (short cable)	REF IN		
		SCSI II		SCSI IV J1 (lower left)	
			SCSI II	SCSI IV J2	
				(lower right)	
			DIG IQ IN 2		DIG IQ IN

1.4 Software Requirements

Software Requirements						
R&S CMW500 (installation via R&S Version Manager, SW to be retrieved on http://extranet.rohde-schwarz.com)						
Basic	R&S CMW-BASE	Standard CMW500 Protocol HW and SW Configuration				
LTE	R&S CMW-KF500	LTE Example Scenarios				
WCDMA	R&S CMW-KF400	WCDMA Example Scenarios				
R&S EX-IQ-BOX						
	R&S DiglConf	Digital Interface Configurator for the R&S EX-IQ-BOX, to be installed on an external PC				
R&S FSQ or R&S FSV						
LTE	R&S FSQ-K100	Analysis of EUTRA/LTE FDD downlink signals				
	R&S FSQ-K101	Analysis of EUTRA/LTE FDD uplink signals				
	R&S FSQ-K102	Analysis of EUTRA/LTE downlink MIMO signals				

2 Running an Application

2.1 Example LTE

2.1.1 Instructions for LTE Example

CADENCE delayBox box setting in terminalAssign_R_S_Ch*_new.qel files

```
delayBox -add {after_CLK_IN_P_20 4 Ch1_CLK_IN_P}
delayBox -add {long_after_CLK_IN_P_80 8 Ch1_CLK_IN_P}
```

Use default Power Values LVCMOS33_8 (3.3V, 8 mA) Please contact CADENCE for the complete Tar ball settings

Note: Do all settings in the following order: 1, 2, 3...6

- 1. Start R&S CMW500 including R&S CMW500 Base Software and PT Server
- 2. R&S DiglConf
 - Start the R&S DiglConf program on R&S CMW500.
 - Change Number of Ex-IQ-Boxes to "2" in the select box.

a. R&S EX-IQ-BOX I

- I. Select R&S EX-IQ-BOX 1 Choose the correct serial number
- II. Select "config..." \rightarrow "Interface Type: user defined ..."
- III. Set To Default Preset all parameters and switching states.
- IV. Logic Type:
- LVTTL Transmitter

SDR

16 Bit

LSB

LSB

Parallel

- V. Direction:
- VI. Protocol \rightarrow Format:
- VII. Protocol \rightarrow Data Rate:
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data → Word Size:
- X. Data \rightarrow Word Aligment:
- XI. Data \rightarrow Bit Order:
- XII. Data → Numeric Format: 2's Complement
- XIII. Clock \rightarrow Clock rate:
- (For example 1.522 MHz)

Refer to Figure 2: Palladium: Logic Analyzer.

(read out from CADENCE system)

- XIV. Clock \rightarrow Clock Source:
- XV. Clock \rightarrow Clock Phase: 180 deg
- XVI. Switch "State" to "ON"
- XVII. Refer to Figure 3: LTE: R&S DigIConf: Setup of the R&S EX-IQ-BOX I (Transmitter).

External

b. R&S EX-IQ-BOX II

- I. Select R&S EX-IQ-BOX 2 Choose the correct serial number
- II. Select "config..." \rightarrow "Interface Type: user defined ..."
 - Preset all parameters and switching states.
- III. Set To DefaultIV. Logic Type:
- V. Direction:
- LVTTL Receiver Parallel

16 Bit

LSB

LSB

- VI. Protocol \rightarrow Format:
- VII. Protocol → Data Rate: SDR
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data \rightarrow Word Size:
- X. Data \rightarrow Word Aligment:
- XI. Data \rightarrow Bit Order:
- XII. Data \rightarrow Numeric Format: 2's Complement
- XIII. Clock \rightarrow Clock rate:
- (read out from CADENCE system) (For example 1.522 MHz)

Refer to Figure 2: Palladium: Logic

Analyzer. External

- XIV. Clock \rightarrow Clock Source:
- XV. Clock \rightarrow Clock Phase: 180 deg
- XVI. Switch "State" to "ON"
- XVII. Refer to Figure 4: LTE: R&S DiglConf: Setup of R&S EX-IQ-BOX II (Receiver).

CMW500

3. Open Project Explorer and load a LTE sample scenario C:\Rohde-Schwarz\Scenarios\15.11\APPL\MLAPI\ LTE SAMPLE SCN\1.0\TestProjectLTE Sample Scn.tpd

Refer to Figure 5: LTE: Test Project with LLAPI test case "II_001" loaded within Project Explorer.

 Apply the RF/DIG IQ settings within the "System Configuration" dialog. To open the GUI, click the "Open System Configuration Dialog" button, see the following figure.



Apply the following settings:

- a. UE connected to: **DIGITAL IQ**
- b. Direction Settings: Downlink Only
- c. Dig IQ OUT 2:
- d. AUX A:
- e. AUX B:
- **Direction OFF** f. Click the "Save Changes" button Refer to Figure 6: LTE: System Configuration with applied DIGITAL IQ settings.

Direction OFF

Sample Rate: 7.68 Msps Enable Source: Digital IQ OUT

- 5. Start the test case within the Project Explorer. Follow the instructions until the MMI Comand Dialog: "5 MHz Cell is setup, Press Send to finish scenario" Refer to Figure 7: MMI Command Dialog message.
- 6. R&S FSQ/R&S FSV settings

Note: EUTRA/LTE Downlink PC Software for the Signal Analyzer R&S FSQ must be installed and licensed on an external PC/laptop. With R&S FSV this is not necessary.

- a. Start R&S FSQ/R&S FSV
- b. After booting up Signal Analyzer software, press "PRESET"
- c. (Start EUTRA/LTE Downlink PC Software on external PC/Laptop) for **R&S FSQ**
- d. Apply "General Settings":
 - I. Duplexing:
 - II. Link Direction:
 - III. Source:
- FDD Downlink
- **Digital IQ**
- IV. VISA RSC:
- IP Address of your R&S FSQ
- V. Refer to Figure 7: MMI Command Dialog message.
- e. Apply "Advanced Settings":
 - I. Source Sampling Rate: 7.68 MHz
 - II. Full Scale Level: 223mV
 - III. Refer to Figure 8, Figure 9 and Figure 10.

Result on R&S FSx

Refer to Figure 12: EUTRA/LTE Downlink PC Software: Results.

Result on CADENCE

Refer to Figure 13 and Figure 14.

Screenshots for LTE Example

 Palladium: Logic Analyzer [/exp 	ort/home/demo/wireless/PRO	_SOLUTION/2010_1X_loopba	ck_lower/dieter.sess = 🗖 🛪
<u>F</u> ile <u>E</u> dit			<u>H</u> elp
💽 🗮 🔡 🔳 🏦			💥 🕒
Setup Control Clock Set/Force	e SDL Probe Memory	RTL/Gate InfiniTrace Asse	rtions
	Runtime Clock	Config	
Clock Configuration			
Clock Name: CLK	Frequency:	- 100.000 MHz 🗸 De	elay: 🛛 cycle 🗸
Clocks Oversampling Ratio:			
Clock Display			
QTFCLK is 100.000000 MHz (actual	is 1.522000 MHz)	Current Clocks O	versampling Ratio: 1
Clock Name	100 000	1 522000	0 Delay
fastest_clock	100.000	1.522000	0
Save Import			

Figure 2: Palladium: Logic Analyzer

Protocol VData VClock VTrigger VTest	
Protoco	Parallel
Data Pata	
Interleaving	
Protocol Data Clock Trigger Test	
Clock Settings	Reference Clock
Clock Rate 1.522 000 000 MHz	Source REF IN
Clock Source External (User Interface)	Freq. Counter 10 MHz
Clock Phase 180 deg	Frequency
Clock Skew 0.00 ns 🗾	
Clock In Skew 0.00 ns 💌	
R&S IQ Data R&S	Clock
Instrument EX-IQ-B	OX Data DUT
Reference Clock	
/Protocol VData VClock VTrigger VTest \	
Signal Type	
Word Size	16 Bit 🗾
Word Alignment	LSB
Bit Order	LSB
User Interface Bits	Alignment
	x x x x x M
Numeric Format	2's Complement 💌
Charles Concerned and the sales Train	
State On Logic Typ	
Direction	Transmitter

Figure 3: LTE: R&S DiglConf: Setup of the R&S EX-IQ-BOX I (Transmitter)

/Protocol V Data V Clock V Trigger V Test	[
Format	Parallel 🗾
Data Rate	SDR 💽
Interleaving	Not Interleaved
/ Protocol ViDatai V Clock V Trigger V Test V	
Signal Type	
Word Alignment	
Dia Orden	
User Interface Bits Alignment	
D 1 2 3 4 5 6 7 8 9 10 11 12 13 L x x x x x x x x x x x x x x x	14 15 16 17 × M
Numeric Format	2's Complement 💌
Protocol Data Clock Trigger Test	
Clock Settings	nce Clock
Clock Rate 1.522 000 000 MHz Source REF	IN 💌
Clock Source External (User Interface) Freq. Counter 10 M	1Hz
Clock Phase 180 deg	quency
Clock Skew 0.00 ns I Ext. Clock	U Hz 💌
Clock In Skew 0.00 ns	
R&S IQ Data R&S Clock Instrument REF OUT Defenses Clock	
State On Logic Type LVTTL	•
Direction	•

Figure 4: LTE: R&S DiglConf: Setup of R&S EX-IQ-BOX II (Receiver)

Project Explorer CMW - TestProjectLTE_Sample_Scn.tpd [C:Rohde-Sch	warz'Scenarios'16.11'APPL'MLAPVLTE_SAMPLE_SC	Htts.0]		808
Iestivojecu.i E_sampie_sch/pd	N		11.1	
E Ty Test Project Description	Extension cosist	-	Yalue	(Y)
	Extension script			
E-Est Sequences	Execution relations	1		
E E Tests	Seecles		⊻	
lest Lases	Timeout [s]	0		
- V II 001 Cell Setup	Test sute reference	LTE Tests_TestSu	te	<u>v</u>
 II ml_001 Cell Setup 	Test case reference	L001 Cel Setup		2
II wi_002 EPS Bearer Setup	Comment			
 Imi_003 MT call with data generator 				
- D mi_004 multi Cell scenario				
Image:				
Image:	_			
I mi 007a Handover - Same cell	×			
J	1			
opening plugin-jar (projectexplorer_base.jar) 19 plugin(s) loaded 0 type(s) loaded				
0 editor(s) loaded				
1 setup pane(s) loaded				
26 SOAP service(s) loaded				
initializing plugin				
Loading TestReports				
O reports loaded				
loading document [C:\Rohde-Schwarz\Scemarios\15.11\APPL\ML	API\LTE_SAMPLE_SCM\1.0\TestFrojectLTE_S	ample_Scn.tpd]		
loading template [C:\Rohde-Schwarz\MCT\template\TestProjec	tDescription_V4.1.dtd]	the lot from the first had t		
loading external reference [C:\Rohde-Schwarz\Scenarios\15.	11\APPL\NLAPI\tsitetopology\ite.top]	rcerte_oampre_oun.couj		
loading external reference [C:\Robde-Schwarz\NCT\LRS\Logic	alResourceSetup.irs]			
creating structure tree				
loading finished				
e Hesseges				
Project Explorer ready		Туре	Lower Imit Up	per init

Figure 5: LTE: Test Project with LLAPI test case "II_001" loaded within Project Explorer

UE Connected To	Configuration	on Files							
DIGITAL IQ	✓ digIQ								1
			Configuration	is applicable for a	il test	cases			
Connector Settings	Signal Routing Se	lected To	est Cases General Se	ettings			202332	20220	21
IQ Board 1									
DIG IQ IN / OUT 1			FDIG IQ OUT 2			LAUX A			
Direction	OFF		Direction	OUT	1.00	Direction	OFF	~	
RAT(s)	LTE		RAT(s)	LTE		Function	None		
Monitor Source	NONE		Monitor Source	NONE		Clock Freq. [MHz]	100.0	2.1.1.2.2.E	
Sample Rate	3.84 Msps		Sample Rate	7.68 Msps	~		0100010	0.000.0	
Start Source	Auto Internal	V	Start Source	Auto Internal	· · · · ·	AUX B			
Enable Source	Auto Internal	· · · · ·	Enable Source	Digital IQ OUT	~	Direction	OFF	~	
Additional Filter	None	~	Additional Filter	None	~	Function	None	×	
Connected Device			Connected Device			Clock Freq. [MHz]		80.020-	
DIG IQ IN / OUT 3-			DIG IQ OUT 4			Direction Settings			
Direction	OFF	101213	Direction	OFF	100	Downlink Only			
RAT(s)			RAT(s)			1			
Monitor Source	NONE		Monitor Source	NONE	~				
Sample Rate	100.0 Msps	· · ·	Sample Rate	100.0 Msps	v				
Start Source	Auto Internal		Start Source	Auto Internal	Y				
Enable Source	Auto Internal		Enable Source	Auto Internal	~				
Additional Filter	1.	10101	Additional Effer		(747)	distances in the second state	12 - 12 - 12 - 12 - 12 - 12 - 12 - 12 -	en play we will have	1

Figure 6: LTE: System Configuration with applied DIGITAL IQ settings

😼 MMI Commai	nd Dialog	8
Request		
5 MHz Cell is setu	p, press Send to finish scenario.	
<		>
	Copy To Clipboard	
Confirm		
Please e	enter MMI command response or error string	
\r\nOK\r\n		
<		>
	Result Flag	
	Send	

Figure 7: MMI Command Dialog message

eneral	Settir	ngs	*# ## ##			×
Seneral	Setting	S Advance	ed Settings			
Signal	Char	acteristics		Result Settings		
Stand	dard	 	3GPP LTE 💌	EVM Unit	%	•
Duple	exing		FDD 💌	Bit Stream Format	Symbols	•
Link I	Directio	on	Downlink 💌	Subframe Selection	-ALL	-
Frequ	Jency		1 GHz	Antenna Selection	Antenna 1	-
Input						
Source	ce		Digital IQ 💌			
Level	Settir	ngs	Master Analyzer 💌			
Auto	Level					
Refe	rence l	_evel (RF)	-30.00 dBm			
Atten	uation	(RF)	10 dB 💌			
Refe	rence l	_evel (BB)	0 dBm 💌			
Trigge	r Set	tings				
Trigg	er Moo	le	Free Run 💌			
Trigg	er Offs	et	0.00			
мімо	Analy	vzer Confia	uration			
200	Nr	State	VISA RSC	Antenna Assignment		
•	1	Master	TCPIP::FSQ8-200427	Antenna 1 (2, 3, 4)		
	2			Antenna 2		
	3			Antenna 3		
	4			Antenna 4		

Figure 8: LTE EUTRA/LTE Downlink PC Software: General Settings

eneral Settings		
eneral Settings Advanced S	ittings	
IQ Settings		
Swap IQ		
Baseband Settings		
Input High Impedance		
Input Balanced		
Input Lowpass		
Input Dithering		
Input Settings Advanced		
Auto Level Track Time	100 ms	
Digital IQ Settings		
Source Sampling Rate	7.68 MHz	
Full Scale Level	223 mV	

Figure 9: LTE EUTRA/LTE Downlink PC Software: Advanced Settings

nodulation Settings					
wnlink Demodulation Setting	ps Downlink Sig	nal Characteristics Down	link Advanced Signa	al Characteristics	
Physical Settings					
hannel Bandwidth	5 MHz	Sampling Rate	7.68 MHz	Occupied BW	4.515 MHz
lumber of Resource Blocks		25 FFT Size	512	Occupied Carriers	301
lyclic Prefix	Auto	▼ 2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.2.			
DD UL/DL Allocations	Conf. 0	TDD Allocations			
Physical Layer Cell Iden	tity				
Cell Identity Group	Auto	▼ Identity	Auto 💌		
MIMO Configuration —					· · · · · · · · · · · · · · · · · · ·
Configuration	1 Tx Antenna	 Antenna Selection 	Antenna 1 📃 💌		
Subframe Configuration					
Configurable Subframes	10	ID Code Mod	Ulation Enhar	nced Number of	Offset Power
Selected Subframe 0	-	Word Word	Settu	ngs HB	RB (dB)
Used Allocations	0				
	· & & & & & & & & & & & & & & & & & & &				

Figure 10: EUTRA/LTE Downlink PC Software: Downlink Signal Characteristics

Demodulation Settings						
Downlink Demodulation Settings Downlink Signal Characteristics Downlink Advanced Signal Characteristics						
Synchronization Signal S	ettings					_
P-/S-SYNC Repetition Period	10 Slots 💽	P-SYNC Rel. Power	0.00 dB	P-/S-SYNC Sequence	P:Internal S:Inter	mal
		S-SYNC Rel. Power	0.00 dB			
Reference Signal Structu	ıre —					
PRS Initialization	36.211 v8.3.0 💌	Rel. Power	0.00 dB	Pseudo-Rand. Seq. R_p	ors Internal	
Subcarrier Offset	Auto 💌					
Misc Settings						
PRB Symbol Offset	2					
PBCH Length	4 Symbols 💌	PBCH Sym. Offset	7			
PCFICH Present	~					
PHICH Number of Groups	0	PHICH Duration	Normal 💌	PHICH Rel. Power	0.00 d	В
PDCCH Present						
Fast Forward (N_c)	1600					

Figure 10: EUTRA/LTE Downlink PC Software: Downlink Advanced Signal Characteristics



Figure 12: EUTRA/LTE Downlink PC Software: Results



Figure 13: Palladium Waveform of I/Q with LTE traffic



Figure 14: Palladium Waveform of I/Q with LTE traffic

3 Hardware Setup for Real Simulation

3.1 Schematic Setup



Figure 14: Setup Diagram

3.2 Hardware Requirements for Real Simulation

Amount	Unit	Hardware Key		
R&S®CMW500 minimum configuration				
1	R&S CMW-B300A Signaling Unit Wideband (SUW)	1202.6304.02		
1	R&S CMW-B510A Digital IQ Board	1202.8007.02		
Adapter				
2	R&S EX-IQ-BOX	1409.5505K04/.02		
2	R&S EXBOX-Z3 CADENCE PALLADIUM Breakout Board	1417.3566.02		
1	CADENCE HDDC Breakout Board SCSI V	39BRSA		
1	Cadence Palladium Emulator			
Cabeling				
2	R&S SMU-Z6 LVDS cable for connecting digital baseband interfaces	1415.0201.02		
1	BNC cable			
1	BNC cable (<= 1m)			
1	BNC T adapter			
2	USB cable			
2	SCSI II to SCSY V cable			

External PC	R&S CMW500	R&S EX-IQ-BOX I	R&S EX-IQ-BOX II	CADENCE HDDC Breakout Board SCSI V
From/ To	From	From/To	From/To	From/To
	DIGIQ OUT2	DIG IQ IN 1		
USB		USB		
USB			USB	
	REF OUT	REF IN		
		REF IN split with BNC T adapter (short cable)	REF IN	
		SCSI II		SCSI IV J1 (lower left)
			SCSI II	SCSI IV J2
				(lower right)
	DIG IQ IN/OUT 1		DIG IQ OUT 2	

3.3 Cabeling of all Units

3.4 Software Requirements

Software Requirements				
R&S CMW500 (installable via R&S Version	Manager, SW to I	be retrieved on http://extranet.rohde-schwarz.com)		
Basic	R&S CMW-BASE	Standard R&S CMW500 Protocol Tester HW and SW Configuration		
LTE	R&S CMW-KF500	LTE Example Scenarios		
WCDMA	R&S CMW-KF400	WCDMA Example Scenarios		
Ex IQ Box				
	R&S DiglConf	Digital Interface Configurator for the R&S EX-IQ-BOX, to be installed on an external PC		

3.5 Example LTE

3.5.1 Instructions for LTE Example

Note: Do all settings in the following order: 1, 2, 3...6

- 1. Start R&S CMW500 including R&S CMW500 Base Software and PT Server
- 2. R&S DiglConf
 - Start the R&S DiglConf program
 - Afterwards change Number of Ex-IQ-Boxes to "2" in the select box

a. R&S EX-IQ-BOX I

- I. Select R&S EX-IQ-BOX 1 Choose the correct serial number
- II. Select "config..." \rightarrow "Interface Type: user defined ..."
- III. Set To Default
- Preset all parameters and switching states. LVTTL

Transmitter

LSB

LSB

- IV. Logic Type: V. Direction:
- VI. Protocol \rightarrow Format:
 - Parallel
- VII. Protocol \rightarrow Data Rate: SDR
- VIII. Protocol \rightarrow Interleaving: Not Interleaved 16 Bit
- IX. Data \rightarrow Word Size:
- X. Data \rightarrow Word Aligment:
- XI. Data \rightarrow Bit Order:
- XII. Data \rightarrow Numeric Format: 2's Complement
 - XIII. Clock \rightarrow Clock rate: (read out from CADENCE system)
 - (For example 1.522 MHz)

Refer to Figure 2: Palladium: Logic

- Analyzer. External
- XIV. Clock \rightarrow Clock Source:
- XV. Clock \rightarrow Clock Phase:
- XVI. Switch "State" to "ON"
- XVII. Refer to Figure 3: LTE: R&S DigIConf: Setup of the R&S EX-IQ-BOX I (Transmitter).

180 deg

b. EX-IQ-BOX II

I. Select R&S EX-IQ-BOX 1 Choose the correct serial number

LVTTL

Receiver

Parallel

SDR

16 Bit

LSB

LSB

- II. Select "config..." \rightarrow "Interface Type: user defined ..."
 - Preset all parameters and switching states.
- III. Set To DefaultIV. Logic Type:
- V. Direction:
- VI. Protocol \rightarrow Format:
- VII. Protocol → Data Rate:
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data \rightarrow Word Size:
- X. Data \rightarrow Word Aligment:
- XI. Data \rightarrow Bit Order:
- XII. Data → Numeric Format: 2's Complement
- XIII. Clock \rightarrow Clock rate:
- (read out from CADENCE system) (For example 1.522 MHz)
- Refer to Figure 2: Palladium: Logic

Analyzer. External

- XIV. Clock \rightarrow Clock Source:
- XV. Clock \rightarrow Clock Phase: 180 deg
- XVI. Switch "State" to "ON"
- XVII. Refer to Figure 4: LTE: R&S DigIConf: Setup of R&S EX-IQ-BOX II (Receiver).

R&S CMW500

- 3. Open Project Explorer and load an UL + DL LTE sample scenario C:\Rohde-Schwarz\Scenarios\15.11\APPL\MLAPI\ LTE_SAMPLE_SCN\1.0\TestProjectLTE_Sample_Scn.tpd For example, load test case "ml_002".
- 4. Apply the RF/DIG IQ settings within the "System Configuration" dialog
 - a. UE connected to: DIGITAL IQ
 - b. Direction Settings:

-	J	
c.	Dig IQ OUT 2:	Sample Rate: 7.68 Msps
		Enable Source: Digital IQ OUT
d.	Dig IQ IN/OUT 1:	Sample Rate: 7.68 Msps
		Enable Source: Auto Internal
e.	AUX A:	Direction OFF
f.	AUX B:	Direction OFF

- g. Click the "Save Changes" button B Refer to Figure 6: LTE: System Configuration with applied DIGITAL IQ settings.
- Start the test case within Project Explorer. For example, start test case "ml_002" (real UL is needed)

4 Troubleshooting

4.1 Testing the HW

4.1.1 Instructions to Test the HW Setup

R&S DiglConf

- Start the R&S DiglConf program. 1.
- 2. Change Number of Ex-IQ-Boxes to "2" in the select box.

a. R&S EX-IQ-BOX I

I. Select R&S EX-IQ-BOX 1 Choose the correct serial number

LSB

LSB

180 deg

20 kHz

Sine

"ON"

- II. Select "config..." \rightarrow "Interface Type: user defined ..."
- III. Set To Default
- Preset all parameters and switching states. LVTTL
- IV. Logic Type: V. Direction: Transmitter
- VI. Protocol \rightarrow Format:
- Parallel VII. Protocol \rightarrow Data Rate: SDR
- VIII. Protocol \rightarrow Interleaving: Not Interleaved 16 Bit
- IX. Data \rightarrow Word Size:
- X. Data \rightarrow Word Alignent:
- XI. Data \rightarrow Bit Order:
- XII. Data \rightarrow Numeric Format: 2's Complement
- XIII. Clock \rightarrow Clock rate: (read out from CADENCE system)
 - (For example 1.522 MHz)
- XIV. Clock \rightarrow Clock Source: External
- XV. Clock \rightarrow Clock Phase:
- XVI. Test \rightarrow Test Signal:
- XVII. Test \rightarrow Fequency:
- XVIII. Test \rightarrow Amplitude: 0 dBFS
- XIX. Test \rightarrow TX Test:
- XX. Switch "State" to "ON"
- XXI. Refer to Figure 15: R&S EX-IQ-BOX transmitter settings.

b. R&S EX-IQ-BOX II

I. Select R&S EX-IQ-BOX 2 Choose the correct serial number

On

16 Bit

LSB

(read out from CADENCE system)

- II. Start Transient Recorder 1...
- III. Data Source: DIG IQ OUT 2
- IV. Smart Graphic: On
- V. Display Type: I/Q
- VI. State:
- VII. Select "config..." \rightarrow "Interface Type: user defined ..."
- VIII. Logic Type: LVTTL IX. Direction: Receiver
- X. Protocol \rightarrow Format: Parallel
- XI. Protocol \rightarrow Data Rate:
- SDR XII. Protocol \rightarrow Interleaving: Not Interleaved
- XIII. Data \rightarrow Word Size:
- XIV. Data \rightarrow Word Alignment: LSB
- XV. Data \rightarrow Bit Order:
- XVI. Data \rightarrow Numeric Format: 2's Complement
- XVII. Clock \rightarrow Clock rate:
- (For example 1.522 MHz) XVIII. Clock \rightarrow Clock Source: External
- XIX. Clock \rightarrow Clock Phase: 180 deg
- XX. Switch "State" to "ON"

3. EX-IQ-BOX II Transient Recorder 1... Refer to Figure 17: .

Result on R&S EX IQ BOX II

If you can see the Sine in the Transient Recorder, the HW setup is OK. If there is a spike, the HW setup is faulty.

Result on CADENCE

Sine wave sampled with the interface CLK without spikes.

Protocol VData VClock VTrigger VTest	
Tx Test	On
Test Signal	Sine 💌
Sine Signal Settings	
Frequency	20.000 kHz 💌
Amplitude	0.00 dBFS 💌

Figure 15: R&S EX-IQ-BOX transmitter settings



Figure 17: R&S EX-IQ-BOX receiver Transient Recorder



Figure 17: Palladium Waveform of I/Q with sine wave

About Rohde & Schwarz

Rohde & Schwarz is an independent group of companies specializing in electronics. It is a leading supplier of solutions in the fields of test and measurement, broadcasting, radiomonitoring and radiolocation, as well as secure communications. Established more than 75 years ago, Rohde & Schwarz has a global presence and a dedicated service network in over 70 countries. Company headquarters are in Munich, Germany.

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- Energy-efficient products
- Continuous improvement in environmental sustainability
- ISO 14001-certified environmental management system



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