

R&S®CMW500 Digital IQ with CADENCE Emulator

Application Note

Products:

- | R&S®CMW500
- | R&S®EX-IQ-BOX | R&S®EXBOX-Z3
- | R&S®FSQ
- | R&S®FSV

This application note explains how to bring a CADENCE system which is attached to an R&S®EX-IQ-BOX into service for the first time.

The first part of the document shows how to setup an LTE Demo without using a UE design. This setup uses the R&S®CMW500 as the downlink transmitter. The emulator receives the downlink via an R&S®EX-IQ-BOX and passes it to an R&S spectrum analyzer (R&S®FSx) via a second R&S®EX-IQ-BOX.

The second part describes the real wiring using up- and downlink. This will only work if a UE design is available on the emulator.

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The following abbreviations are used throughout this manual:

R&S[®]EX-IQ-BOX is abbreviated as R&S EX-IQ-BOX, R&S[®]EXBOX-Z3 is abbreviated as R&S EXBOX-Z3, R&S[®]CMW500 is abbreviated as R&S CMW500, R&S[®]FSQ is abbreviated as R&S FSQ and R&S[®]FSV is abbreviated as R&S FSV.

1 Hardware Setup for LTE Demo

1.1 Schematic Setup

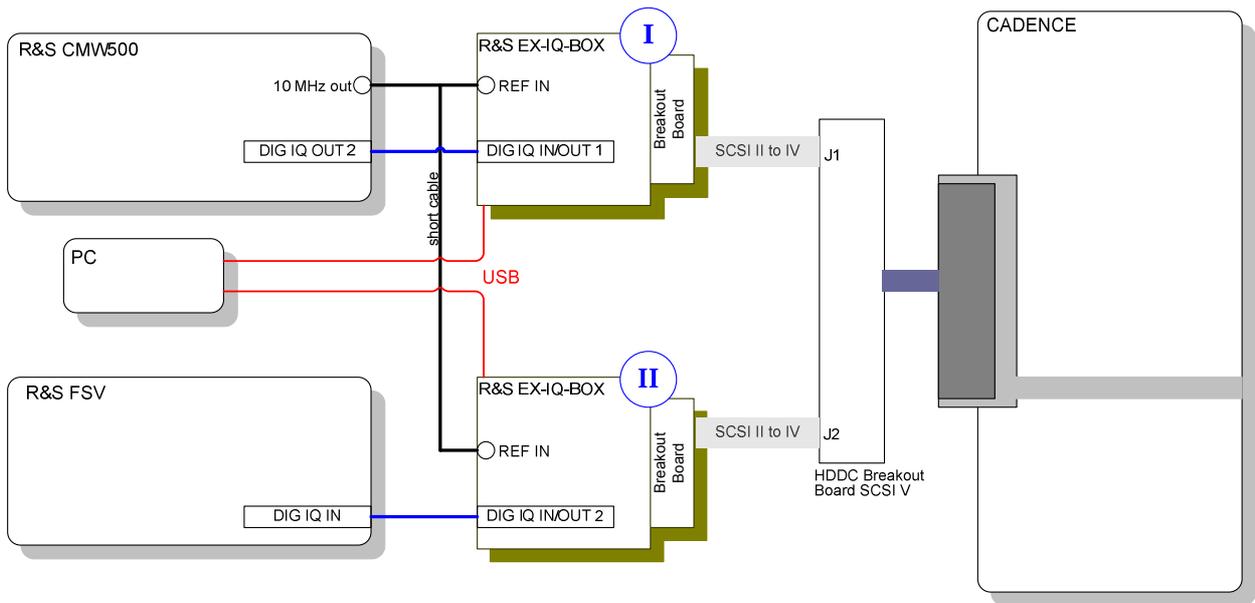


Figure 1: Setup Diagram

1.2 Hardware Requirements for Demo

Amount	Unit	Hardware Key
R&S CMW500 minimum configuration		
1	R&S CMW-B300A Signaling Unit Wideband (SUW)	1202.6304.02
1	R&S CMW-B510A Digital IQ Board	1202.8007.02
Adapter		
2	R&S EX-IQ-BOX	1409.5505K04/.02
2	R&S EXBOX-Z3 CADENCE PALLADIUM Breakout Board	1417.3566.02
1	CADENCE HDDC Breakout Board SCSI V	39BRSA
1	Cadence Palladium Emulator	
R&S FSQ or R&S FSV		
1	R&S FSQ-B17 Digital Baseband Interface	1163.0063.02
Cabeling		
2	R&S SMU-Z6 LVDS cable for connecting digital baseband interfaces	1415.0201.02
1	BNC cable	
1	BNC cable (<= 1m)	
1	BNC T adapter	
2	USB cable	
2	SCSI II to SCSI V cable	

1.3 Cabeling of All Units

External PC	R&S CMW500	R&S EX-IQ-BOX I	R&S EX-IQ-BOX II	CADENCE HDDC Breakout Board SCSI V	R&S FSQ/ R&S FSV
From.../ To...	From...	From.../To...	From.../To...	From.../To...	From.../To...
	DIGIQ OUT2	DIG IQ IN 1			
USB		USB			
USB			USB		
	REF OUT	REF IN			
		REF IN split with BNC T adapter (short cable)	REF IN		
		SCSI II		SCSI IV J1 (lower left)	
			SCSI II	SCSI IV J2 (lower right)	
			DIG IQ IN 2		DIG IQ IN

1.4 Software Requirements

Software Requirements		
R&S CMW500 (installation via R&S Version Manager, SW to be retrieved on http://extranet.rohde-schwarz.com)		
Basic	R&S CMW-BASE	Standard CMW500 Protocol HW and SW Configuration
LTE	R&S CMW-KF500	LTE Example Scenarios
WCDMA	R&S CMW-KF400	WCDMA Example Scenarios
R&S EX-IQ-BOX		
	R&S DigIConf	Digital Interface Configurator for the R&S EX-IQ-BOX, to be installed on an external PC
R&S FSQ or R&S FSV		
LTE	R&S FSQ-K100	Analysis of EUTRA/LTE FDD downlink signals
	R&S FSQ-K101	Analysis of EUTRA/LTE FDD uplink signals
	R&S FSQ-K102	Analysis of EUTRA/LTE downlink MIMO signals

2 Running an Application

2.1 Example LTE

2.1.1 Instructions for LTE Example

CADENCE delayBox box setting in terminalAssign_R_S_Ch*_new.qel files

```
-----
delayBox -add {after_CLK_IN_P_20 4 Ch1_CLK_IN_P}
delayBox -add {long_after_CLK_IN_P_80 8 Ch1_CLK_IN_P}
-----
```

Use default Power Values LVCMOS33_8 (3.3V, 8 mA)
Please contact CADENCE for the complete Tar ball settings

Note: Do all settings in the following order: 1, 2, 3...6

1. Start R&S CMW500 including R&S CMW500 Base Software and PT Server
2. R&S DigiConf
 - Start the R&S DigiConf program on R&S CMW500.
 - Change Number of Ex-IQ-Boxes to “2” in the select box.

a. R&S EX-IQ-BOX I

- I. Select R&S EX-IQ-BOX 1 Choose the correct serial number
- II. Select “config...” → “Interface Type: user defined ...”
- III. Set To Default Preset all parameters and switching states.
- IV. Logic Type: LVTTTL
- V. Direction: Transmitter
- VI. Protocol → Format: Parallel
- VII. Protocol → Data Rate: SDR
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data → Word Size: 16 Bit
- X. Data → Word Aligment: LSB
- XI. Data → Bit Order: LSB
- XII. Data → Numeric Format: 2’s Complement
- XIII. Clock → Clock rate: (read out from CADENCE system)
(For example 1.522 MHz)
Refer to [Figure 2: Palladium: Logic Analyzer](#).
- XIV. Clock → Clock Source: External
- XV. Clock → Clock Phase: 180 deg
- XVI. Switch “State” to “ON”
- XVII. Refer to [Figure 3: LTE: R&S DigiConf: Setup of the R&S EX-IQ-BOX I \(Transmitter\)](#).

b. R&S EX-IQ-BOX II

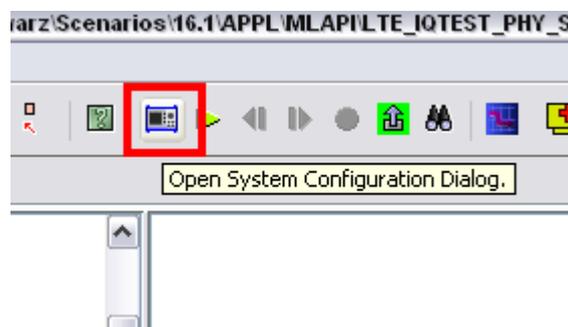
- I. Select R&S EX-IQ-BOX 2 Choose the correct serial number
- II. Select "config..." → "Interface Type: user defined ..."
- III. Set To Default Preset all parameters and switching states.
- IV. Logic Type: LVTTL
- V. Direction: Receiver
- VI. Protocol → Format: Parallel
- VII. Protocol → Data Rate: SDR
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data → Word Size: 16 Bit
- X. Data → Word Aligment: LSB
- XI. Data → Bit Order: LSB
- XII. Data → Numeric Format: 2's Complement
- XIII. Clock → Clock rate: (read out from CADENCE system)
(For example 1.522 MHz)
Refer to [Figure 2: Palladium: Logic Analyzer](#).
- XIV. Clock → Clock Source: External
- XV. Clock → Clock Phase: 180 deg
- XVI. Switch "State" to "ON"
- XVII. Refer to [Figure 4: LTE: R&S DigiConf: Setup of R&S EX-IQ-BOX II \(Receiver\)](#).

CMW500

3. Open Project Explorer and load a LTE sample scenario
C:\Rohde-Schwarz\Scenarios\15.11\APPL\MLAPI\
LTE_SAMPLE_SCN\1.0\TestProjectLTE_Sample_Scn.tpd

Refer to [Figure 5: LTE: Test Project with LLAPI test case "ll_001" loaded within Project Explorer](#).

4. Apply the RF/DIG IQ settings within the "System Configuration" dialog.
To open the GUI, click the "Open System Configuration Dialog" button, see the following figure.



Apply the following settings:

- a. UE connected to: DIGITAL IQ
- b. Direction Settings: Downlink Only
- c. Dig IQ OUT 2: Sample Rate: 7.68 Msps
Enable Source: Digital IQ OUT
- d. AUX A: Direction OFF
- e. AUX B: Direction OFF
- f. Click the "Save Changes" button 
Refer to [Figure 6: LTE: System Configuration with applied DIGITAL IQ settings](#).

5. Start the test case within the Project Explorer.
Follow the instructions until the MMI Command Dialog:
"5 MHz Cell is setup, Press Send to finish scenario"
Refer to [Figure 7: MMI Command Dialog message](#).

6. R&S FSQ/R&S FSV settings

Note: EUTRA/LTE Downlink PC Software for the Signal Analyzer R&S FSQ must be installed and licensed on an external PC/laptop.
With R&S FSV this is not necessary.

- a. Start R&S FSQ/R&S FSV
- b. After booting up Signal Analyzer software, press "PRESET"
- c. (Start EUTRA/LTE Downlink PC Software on external PC/Laptop) for R&S FSQ
- d. Apply "General Settings":
 - I. Duplexing: FDD
 - II. Link Direction: Downlink
 - III. Source: Digital IQ
 - IV. VISA RSC: IP Address of your R&S FSQ
 - V. Refer to [Figure 7: MMI Command Dialog message](#).
- e. Apply "Advanced Settings":
 - I. Source Sampling Rate: 7.68 MHz
 - II. Full Scale Level: 223mV
 - III. Refer to [Figure 8](#), [Figure 9](#) and [Figure 10](#).

Result on R&S FSx

Refer to [Figure 12: EUTRA/LTE Downlink PC Software: Results](#).

Result on CADENCE

Refer to [Figure 13](#) and [Figure 14](#).

Screenshots for LTE Example

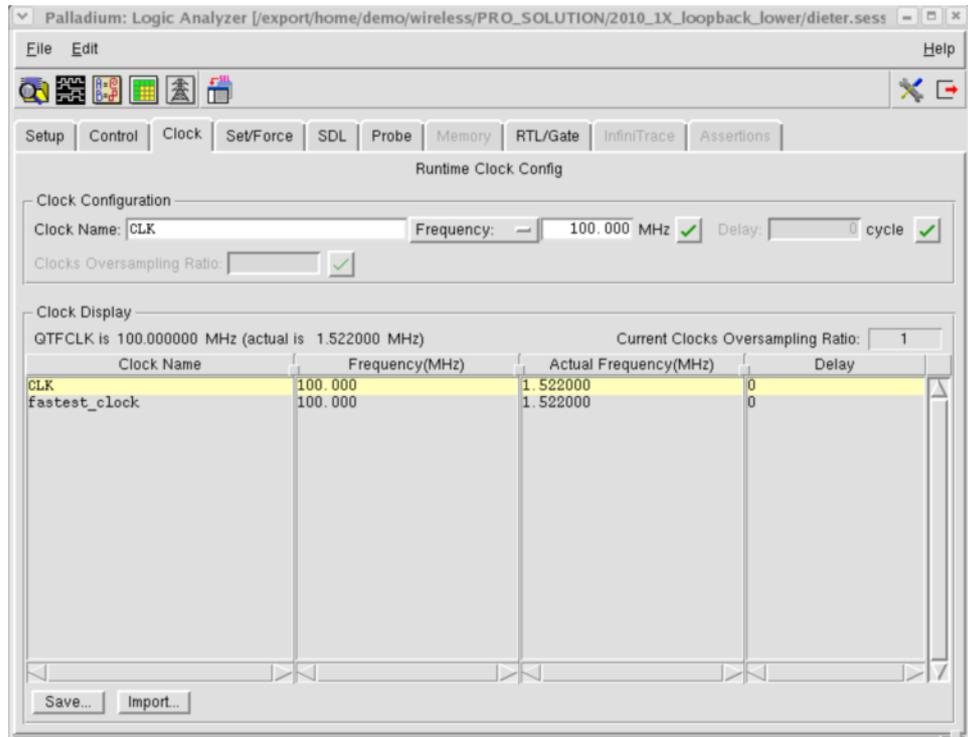


Figure 2: Palladium: Logic Analyzer

The screenshot displays the R&S DigiConf software interface, divided into three main sections: Protocol, Clock, and Data.

Protocol Tab: Shows settings for Format (Parallel), Data Rate (SDR), and Interleaving (Not Interleaved).

Clock Tab: Contains Clock Settings and Reference Clock sections.

- Clock Settings:** Clock Rate (1.522 000 000 MHz), Clock Source (External (User Interface)), Clock Phase (180 deg), Clock Skew (0.00 ns), and Clock In Skew (0.00 ns).
- Reference Clock:** Source (REF IN), Freq. Counter (10 MHz), and Ext. Clock (0 Hz).

 A block diagram below shows the signal flow: R&S Instrument REF OUT provides a Reference Clock to R&S EX-IQ-BOX REF IN. The EX-IQ-BOX outputs IQ Data to the Instrument and Clock Data to the DUT.

Data Tab: Configures signal parameters:

- Signal Type: IQ
- Word Size: 16 Bit
- Word Alignment: LSB
- Bit Order: LSB
- User Interface Bits Alignment: A table showing bit positions 0-17. Bits 1-14 are marked 'x', bit 15 is 'M', and bits 16-17 are '-'.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
L	x	x	x	x	x	x	x	x	x	x	x	x	x	x	M	-	-
- Numeric Format: 2's Complement

Bottom Section:

- State: On (highlighted)
- Logic Type: LVTTL
- Direction: Transmitter

Figure 3: LTE: R&S DigiConf: Setup of the R&S EX-IQ-BOX I (Transmitter)

The screenshot displays the R&S DigiConf configuration interface, divided into three main sections: Protocol, Data, and Clock.

Protocol Section:

- Format: Parallel
- Data Rate: SDR
- Interleaving: Not Interleaved

Data Section:

- Signal Type: IQ
- Word Size: 16 Bit
- Word Alignment: LSB
- Bit Order: LSB
- User Interface Bits Alignment: A table showing bit positions 0-17. Bits 1-14 are marked 'x', bit 15 is 'M', and bits 16-17 are '-'.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
L	x	x	x	x	x	x	x	x	x	x	x	x	x	x	M	-	-
- Numeric Format: 2's Complement

Clock Section:

- Clock Settings:**
 - Clock Rate: 1.522 000 000 MHz
 - Clock Source: External (User Interface)
 - Clock Phase: 180 deg
 - Clock Skew: 0.00 ns
 - Clock In Skew: 0.00 ns
- Reference Clock:**
 - Source: REF IN
 - Freq. Counter: 10 MHz
- Frequency:**
 - Ext. Clock: 0 Hz

Block Diagram:

```

    graph LR
      R_S_Instrument[R&S Instrument REF OUT] -- Reference Clock --> R_S_EX_IQ_BOX[R&S EX-IQ-BOX REF IN]
      R_S_Instrument -- IQ Data --> R_S_EX_IQ_BOX
      R_S_EX_IQ_BOX -- Clock Data --> DUT[DUT]
    
```

State and Logic Settings:

- State: On
- Logic Type: LVTTL
- Direction: Receiver

Figure 4: LTE: R&S DigiConf: Setup of R&S EX-IQ-BOX II (Receiver)

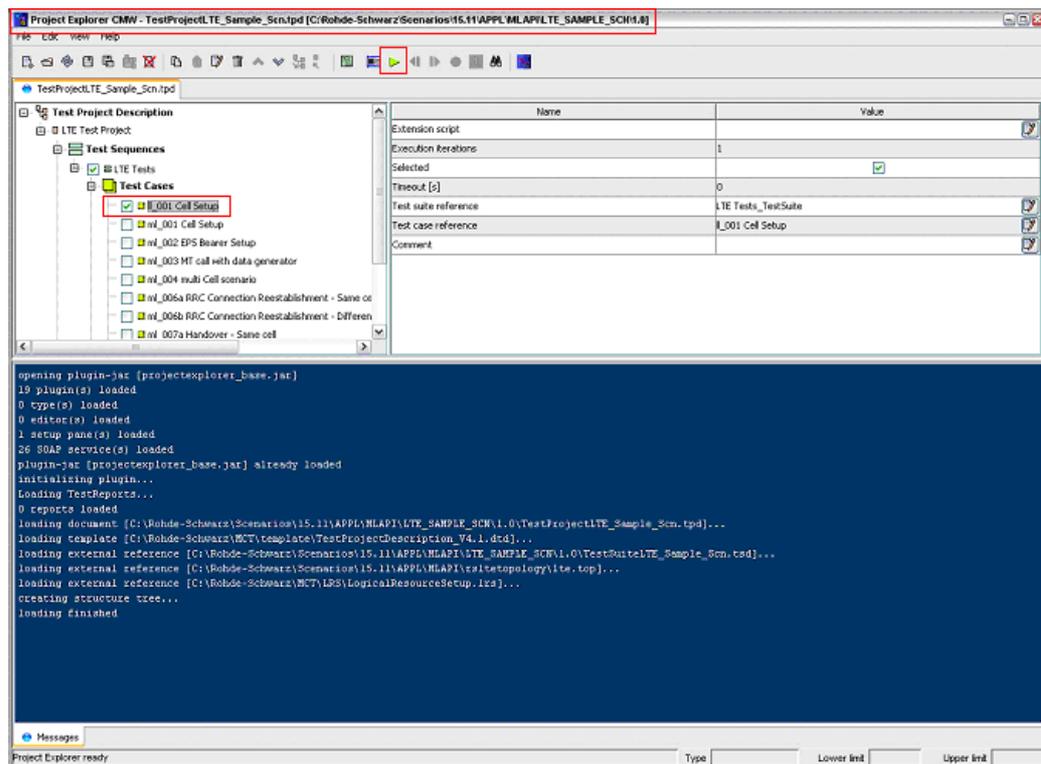


Figure 5: LTE: Test Project with LLAPI test case "II_001" loaded within Project Explorer

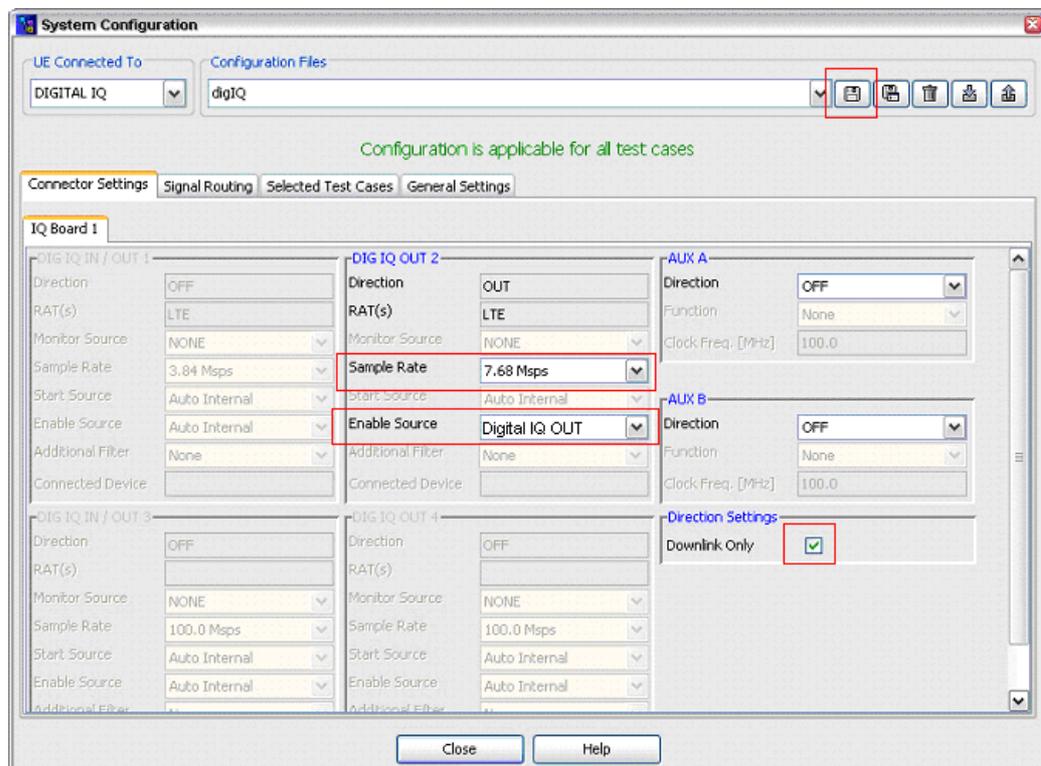


Figure 6: LTE: System Configuration with applied DIGITAL IQ settings

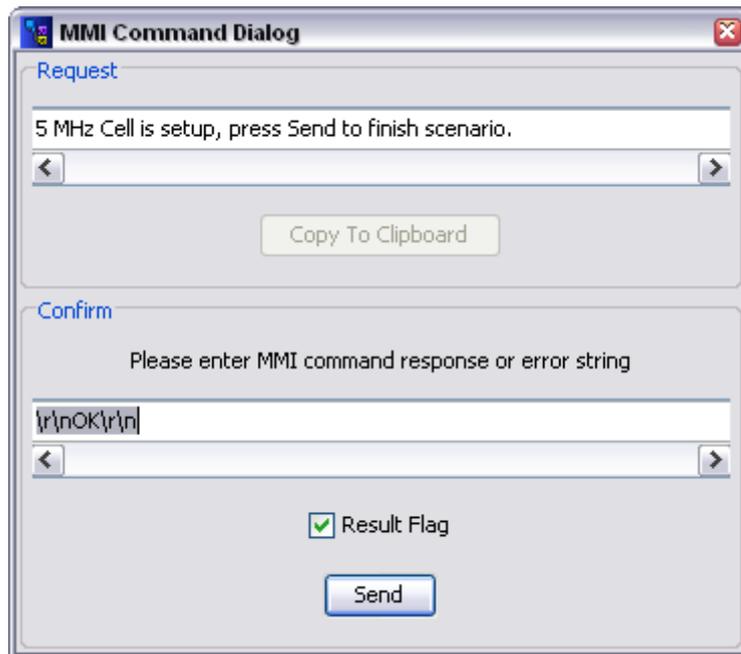


Figure 7: MMI Command Dialog message

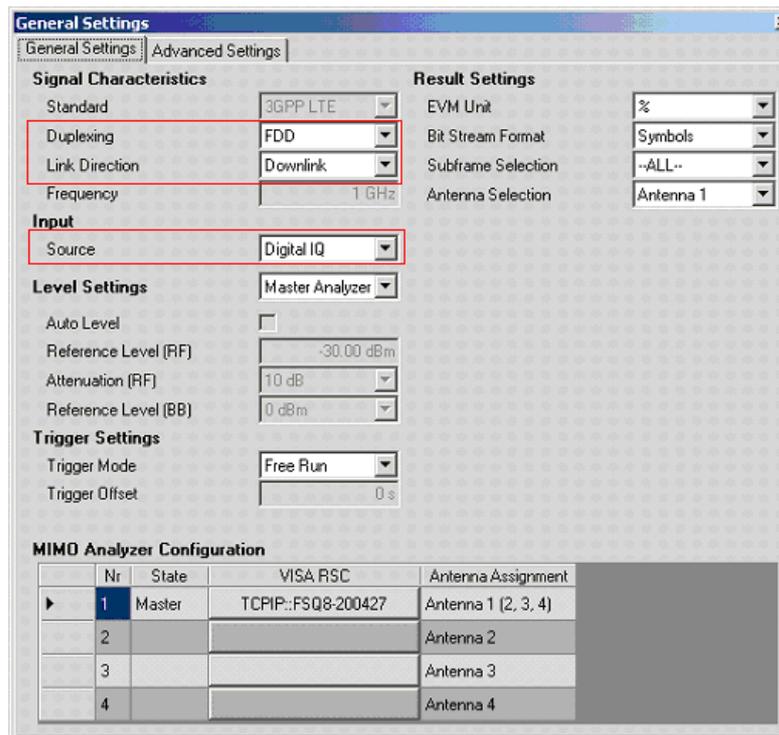


Figure 8: LTE EUTRA/LTE Downlink PC Software: General Settings

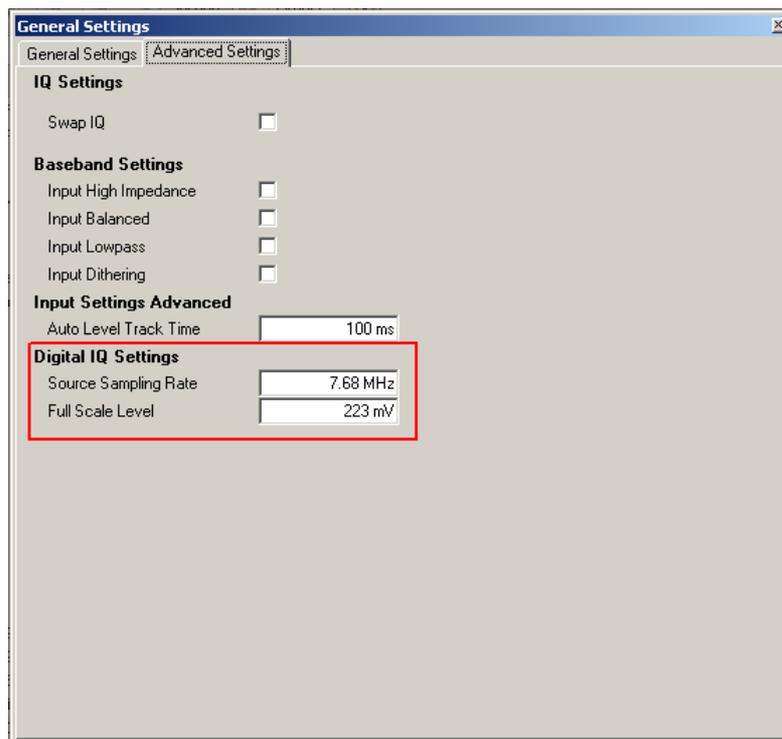


Figure 9: LTE EUTRA/LTE Downlink PC Software: Advanced Settings

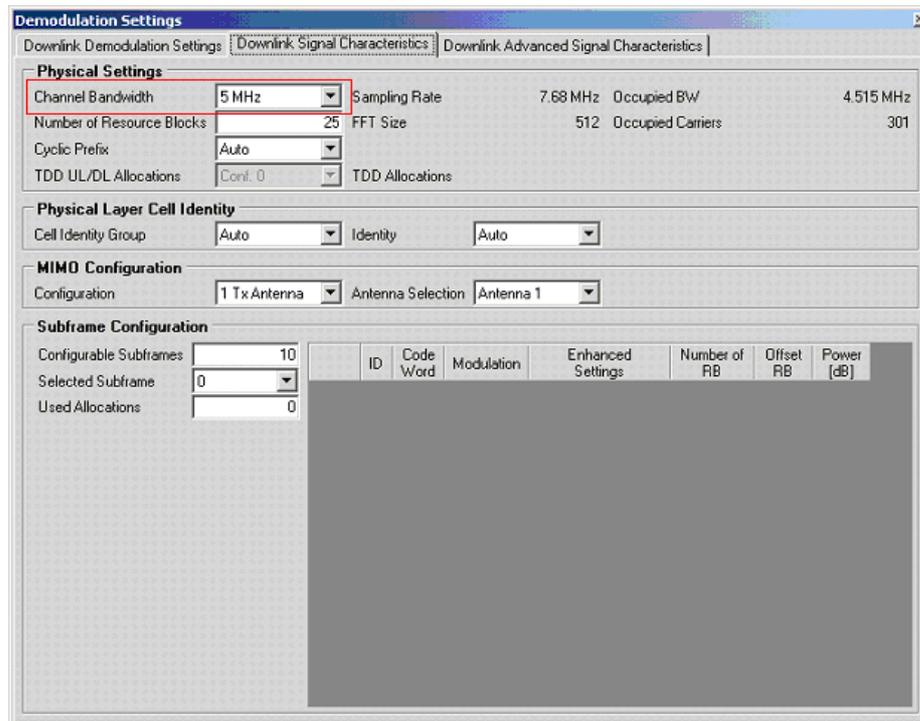


Figure 10: EUTRA/LTE Downlink PC Software: Downlink Signal Characteristics

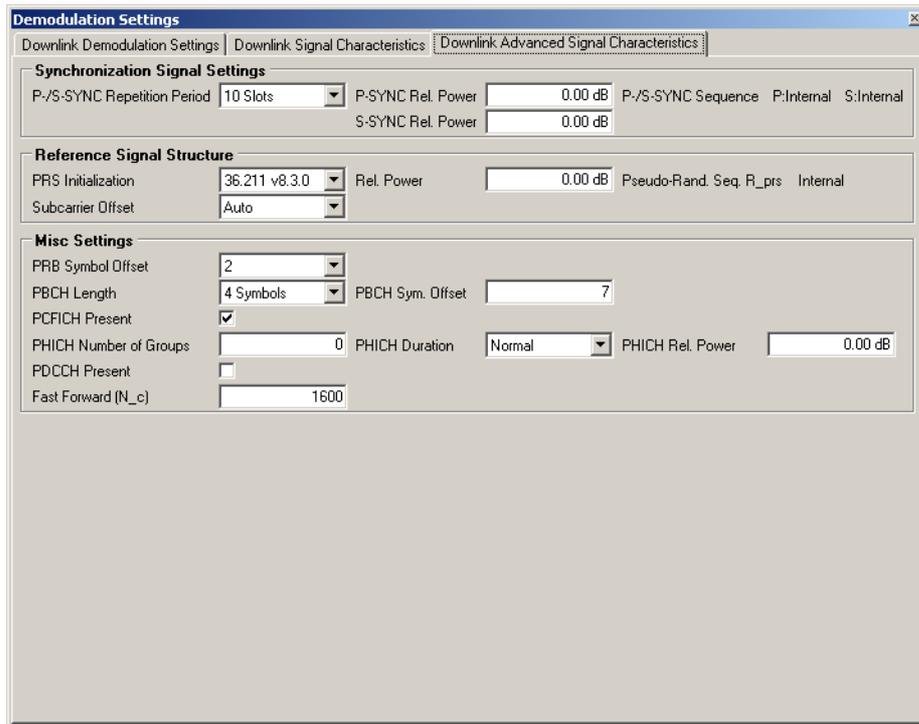


Figure 10: EUTRA/LTE Downlink PC Software: Downlink Advanced Signal Characteristics

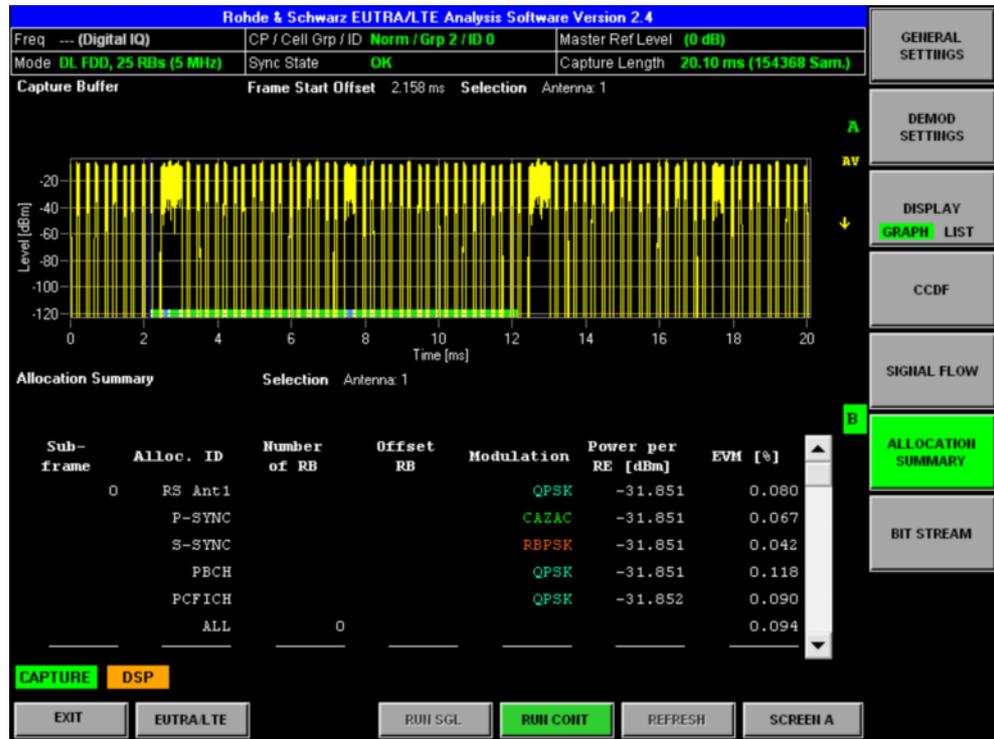


Figure 12: EUTRA/LTE Downlink PC Software: Results

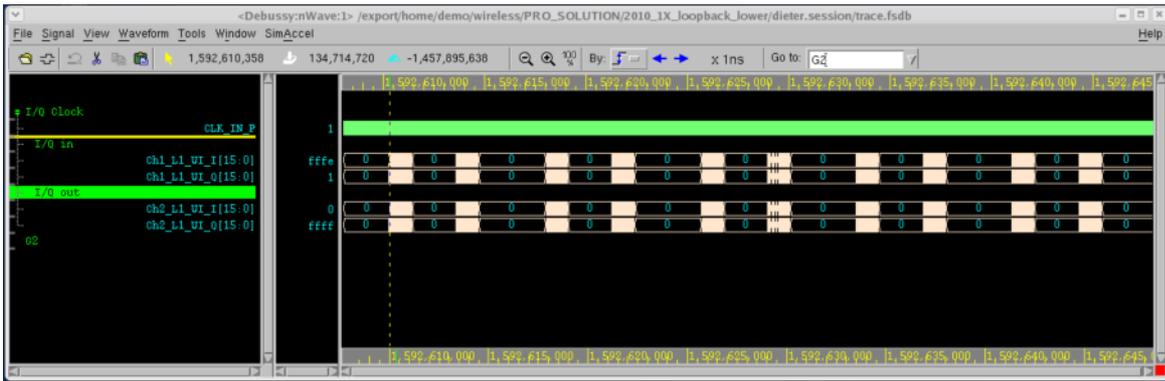


Figure 13: Palladium Waveform of I/Q with LTE traffic

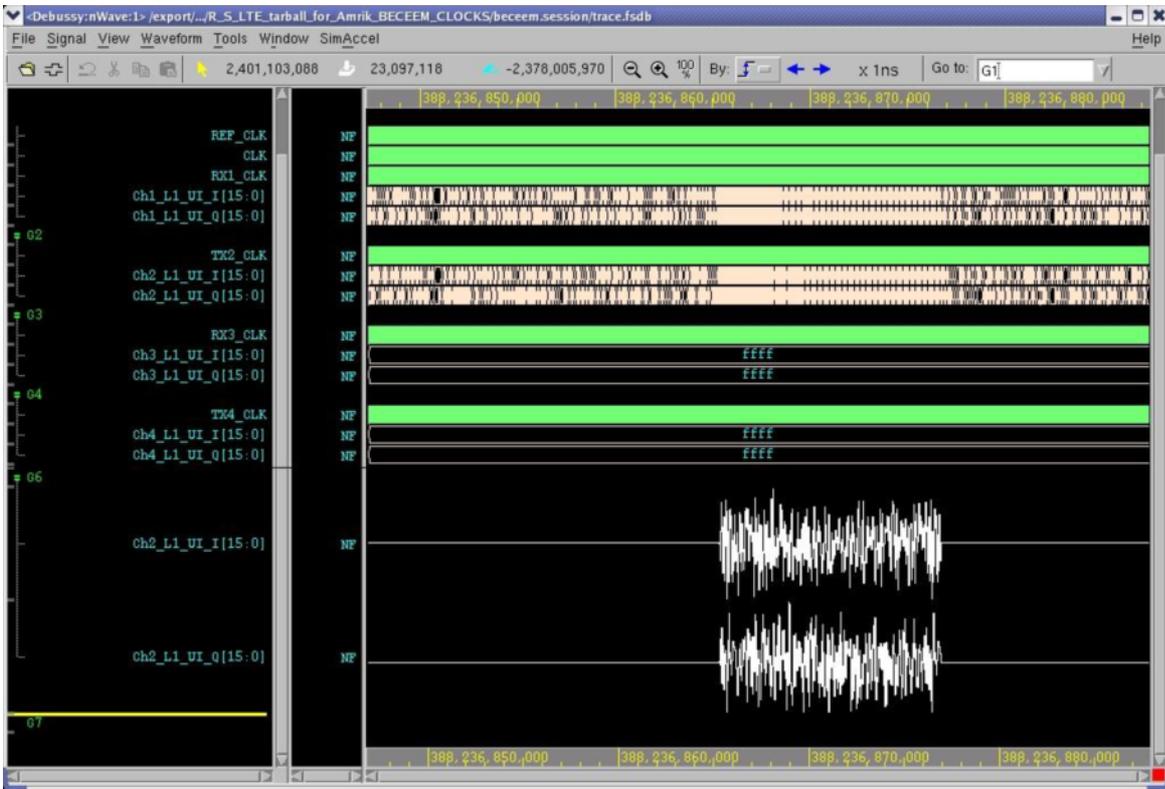


Figure 14: Palladium Waveform of I/Q with LTE traffic

3 Hardware Setup for Real Simulation

3.1 Schematic Setup

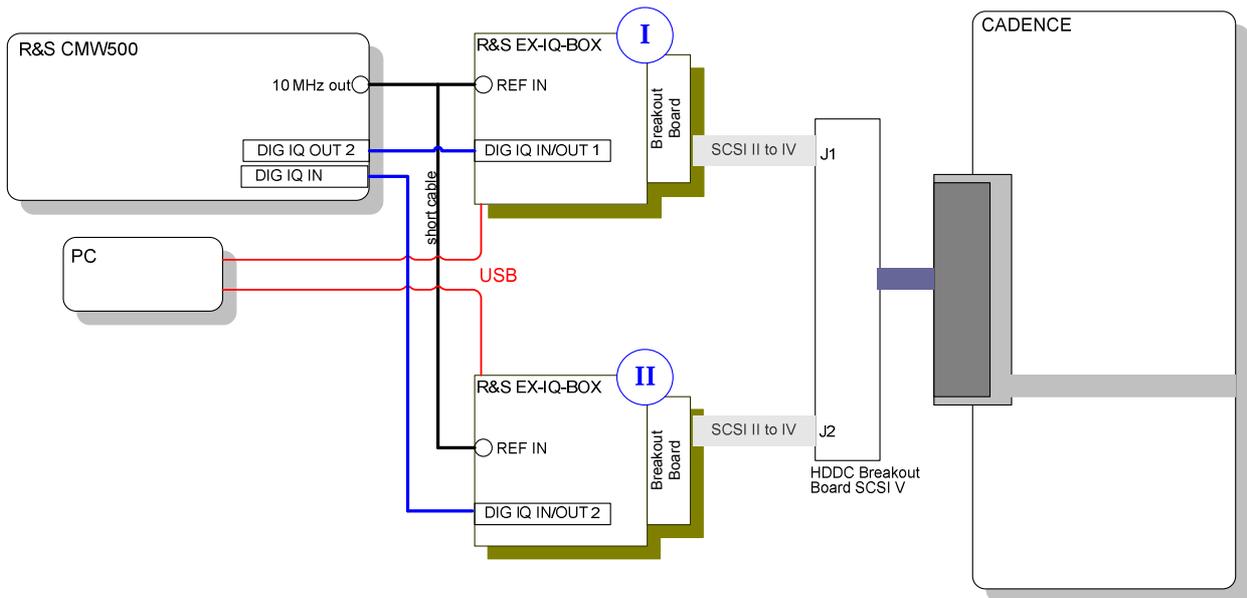


Figure 14: Setup Diagram

3.2 Hardware Requirements for Real Simulation

Amount	Unit	Hardware Key
R&S®CMW500 minimum configuration		
1	R&S CMW-B300A Signaling Unit Wideband (SUW)	1202.6304.02
1	R&S CMW-B510A Digital IQ Board	1202.8007.02
Adapter		
2	R&S EX-IQ-BOX	1409.5505K04/.02
2	R&S EXBOX-Z3 CADENCE PALLADIUM Breakout Board	1417.3566.02
1	CADENCE HDDC Breakout Board SCSI V	39BRSA
1	Cadence Palladium Emulator	
Cabeling		
2	R&S SMU-Z6 LVDS cable for connecting digital baseband interfaces	1415.0201.02
1	BNC cable	
1	BNC cable (<= 1m)	
1	BNC T adapter	
2	USB cable	
2	SCSI II to SCSI V cable	

3.3 Cabeling of all Units

External PC	R&S CMW500	R&S EX-IQ-BOX I	R&S EX-IQ-BOX II	CADENCE HDDC Breakout Board SCSI V
From.../To...	From...	From.../To...	From.../To...	From.../To...
	DIGIQ OUT2	DIG IQ IN 1		
USB		USB		
USB			USB	
	REF OUT	REF IN		
		REF IN split with BNC T adapter (short cable)	REF IN	
		SCSI II		SCSI IV J1 (lower left)
			SCSI II	SCSI IV J2 (lower right)
	DIG IQ IN/OUT 1		DIG IQ OUT 2	

3.4 Software Requirements

Software Requirements		
R&S CMW500 (installable via R&S Version Manager, SW to be retrieved on http://extranet.rohde-schwarz.com)		
Basic	R&S CMW-BASE	Standard R&S CMW500 Protocol Tester HW and SW Configuration
LTE	R&S CMW-KF500	LTE Example Scenarios
WCDMA	R&S CMW-KF400	WCDMA Example Scenarios
Ex IQ Box		
	R&S DigIConf	Digital Interface Configurator for the R&S EX-IQ-BOX, to be installed on an external PC

3.5 Example LTE

3.5.1 Instructions for LTE Example

Note: Do all settings in the following order: 1, 2, 3...6

1. Start R&S CMW500 including R&S CMW500 Base Software and PT Server
2. R&S DigIConf
 - Start the R&S DigIConf program
 - Afterwards change Number of Ex-IQ-Boxes to “2” in the select box

a. R&S EX-IQ-BOX I

- I. Select R&S EX-IQ-BOX 1 Choose the correct serial number
- II. Select “config...” → “Interface Type: user defined ...”
- III. Set To Default Preset all parameters and switching states.
- IV. Logic Type: LVTTTL
- V. Direction: Transmitter
- VI. Protocol → Format: Parallel
- VII. Protocol → Data Rate: SDR
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data → Word Size: 16 Bit
- X. Data → Word Aligment: LSB
- XI. Data → Bit Order: LSB
- XII. Data → Numeric Format: 2’s Complement
- XIII. Clock → Clock rate: (read out from CADENCE system)
(For example 1.522 MHz)
Refer to [Figure 2: Palladium: Logic Analyzer](#).
- XIV. Clock → Clock Source: External
- XV. Clock → Clock Phase: 180 deg
- XVI. Switch “State” to “ON”
- XVII. Refer to [Figure 3: LTE: R&S DigIConf: Setup of the R&S EX-IQ-BOX I \(Transmitter\)](#).

b. EX-IQ-BOX II

- I. Select R&S EX-IQ-BOX 1 Choose the correct serial number
- II. Select "config..." → "Interface Type: user defined ..."
- III. Set To Default Preset all parameters and switching states.
- IV. Logic Type: LVTTL
- V. Direction: Receiver
- VI. Protocol → Format: Parallel
- VII. Protocol → Data Rate: SDR
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data → Word Size: 16 Bit
- X. Data → Word Aligment: LSB
- XI. Data → Bit Order: LSB
- XII. Data → Numeric Format: 2's Complement
- XIII. Clock → Clock rate: (read out from CADENCE system)
(For example 1.522 MHz)
Refer to [Figure 2: Palladium: Logic Analyzer](#).
- XIV. Clock → Clock Source: External
- XV. Clock → Clock Phase: 180 deg
- XVI. Switch "State" to "ON"
- XVII. Refer to [Figure 4: LTE: R&S DigiConf: Setup of R&S EX-IQ-BOX II \(Receiver\)](#).

R&S CMW500

3. Open Project Explorer and load an UL + DL LTE sample scenario
C:\Rohde-Schwarz\Scenarios\15.11\APPL\MLAPI\
LTE_SAMPLE_SCN\1.0\TestProjectLTE_Sample_Scn.tpd
For example, load test case "ml_002".
4. Apply the RF/DIG IQ settings within the "System Configuration" dialog
 - a. UE connected to: DIGITAL IQ
 - b. Direction Settings: ---
 - c. Dig IQ OUT 2: Sample Rate: 7.68 Msps
Enable Source: Digital IQ OUT
 - d. Dig IQ IN/OUT 1: Sample Rate: 7.68 Msps
Enable Source: Auto Internal
 - e. AUX A: Direction OFF
 - f. AUX B: Direction OFF
 - g. Click the "Save Changes" button 
Refer to [Figure 6: LTE: System Configuration with applied DIGITAL IQ settings](#).
5. Start the test case within Project Explorer.
For example, start test case "ml_002" (real UL is needed)

4 Troubleshooting

4.1 Testing the HW

4.1.1 Instructions to Test the HW Setup

R&S DigIConf

1. Start the R&S DigIConf program.
2. Change Number of Ex-IQ-Boxes to "2" in the select box.

a. R&S EX-IQ-BOX I

- I. Select R&S EX-IQ-BOX 1 Choose the correct serial number
- II. Select "config..." → "Interface Type: user defined ..."
- III. Set To Default Preset all parameters and switching states.
- IV. Logic Type: LVTTTL
- V. Direction: Transmitter
- VI. Protocol → Format: Parallel
- VII. Protocol → Data Rate: SDR
- VIII. Protocol → Interleaving: Not Interleaved
- IX. Data → Word Size: 16 Bit
- X. Data → Word Aligment: LSB
- XI. Data → Bit Order: LSB
- XII. Data → Numeric Format: 2's Complement
- XIII. Clock → Clock rate: (read out from CADENCE system)
(For example 1.522 MHz)
- XIV. Clock → Clock Source: External
- XV. Clock → Clock Phase: 180 deg
- XVI. Test → Test Signal: Sine
- XVII. Test → Fequency: 20 kHz
- XVIII. Test → Amplitude: 0 dBFS
- XIX. Test → TX Test: "ON"
- XX. Switch "State" to "ON"
- XXI. Refer to [Figure 15: R&S EX-IQ-BOX transmitter settings](#).

b. R&S EX-IQ-BOX II

- I. Select R&S EX-IQ-BOX 2 Choose the correct serial number
- II. Start Transient Recorder 1...
- III. Data Source: DIG IQ OUT 2
- IV. Smart Graphic: On
- V. Display Type: I/Q
- VI. State: On
- VII. Select "config..." → "Interface Type: user defined ..."
- VIII. Logic Type: LVTTTL
- IX. Direction: Receiver
- X. Protocol → Format: Parallel
- XI. Protocol → Data Rate: SDR
- XII. Protocol → Interleaving: Not Interleaved
- XIII. Data → Word Size: 16 Bit
- XIV. Data → Word Aligment: LSB
- XV. Data → Bit Order: LSB
- XVI. Data → Numeric Format: 2's Complement
- XVII. Clock → Clock rate: (read out from CADENCE system)
(For example 1.522 MHz)
- XVIII. Clock → Clock Source: External
- XIX. Clock → Clock Phase: 180 deg
- XX. Switch "State" to "ON"

- EX-IQ-BOX II Transient Recorder 1...
Refer to [Figure 17](#): .

Result on R&S EX IQ BOX II

If you can see the Sine in the Transient Recorder, the HW setup is OK.
If there is a spike, the HW setup is faulty.

Result on CADENCE

Sine wave sampled with the interface CLK without spikes.

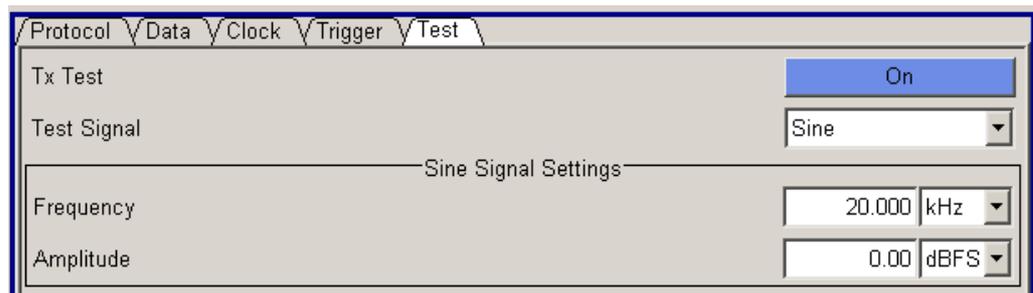


Figure 15: R&S EX-IQ-BOX transmitter settings

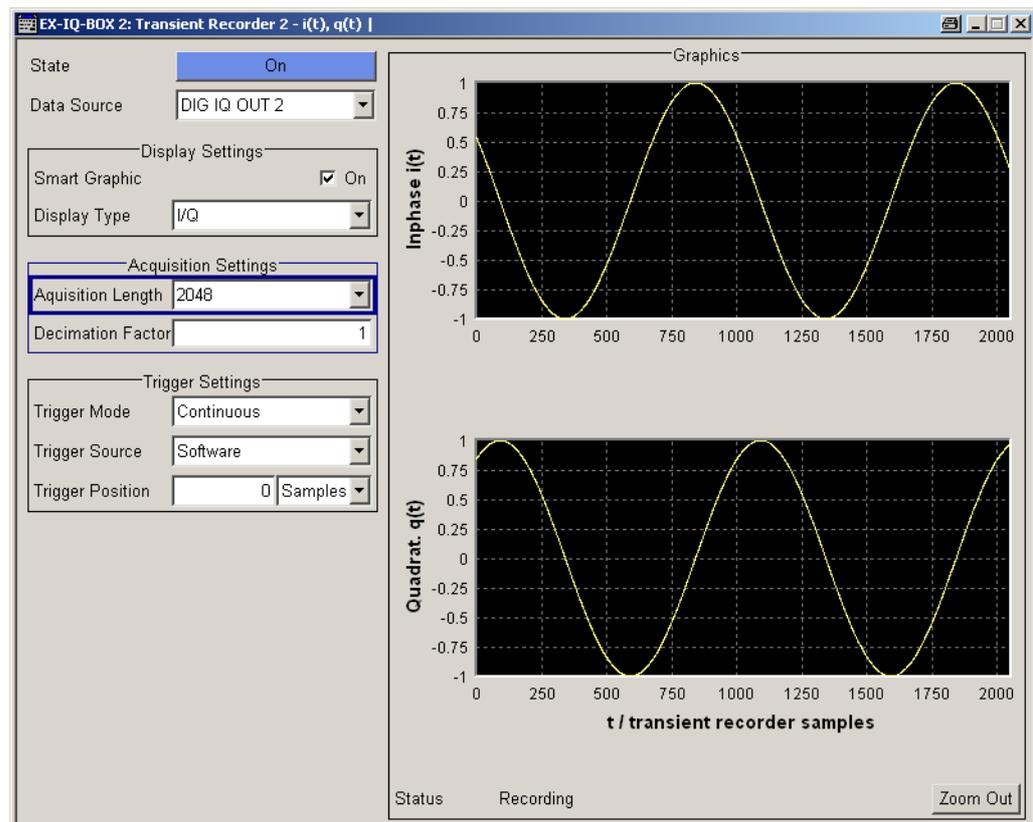


Figure 17: R&S EX-IQ-BOX receiver Transient Recorder

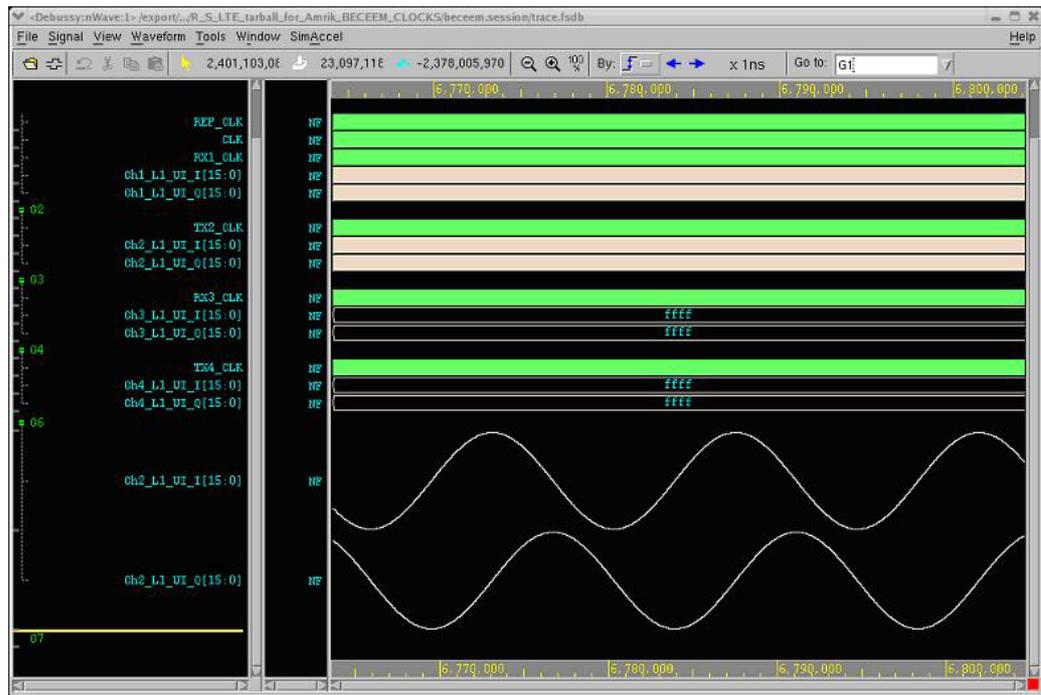


Figure 17: Palladium Waveform of I/Q with sine wave

About Rohde & Schwarz

Rohde & Schwarz is an independent group of companies specializing in electronics. It is a leading supplier of solutions in the fields of test and measurement, broadcasting, radiomonitoring and radiolocation, as well as secure communications. Established more than 75 years ago, Rohde & Schwarz has a global presence and a dedicated service network in over 70 countries. Company headquarters are in Munich, Germany.

Environmental commitment

- Energy-efficient products
- Continuous improvement in environmental sustainability
- ISO 14001-certified environmental management system



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